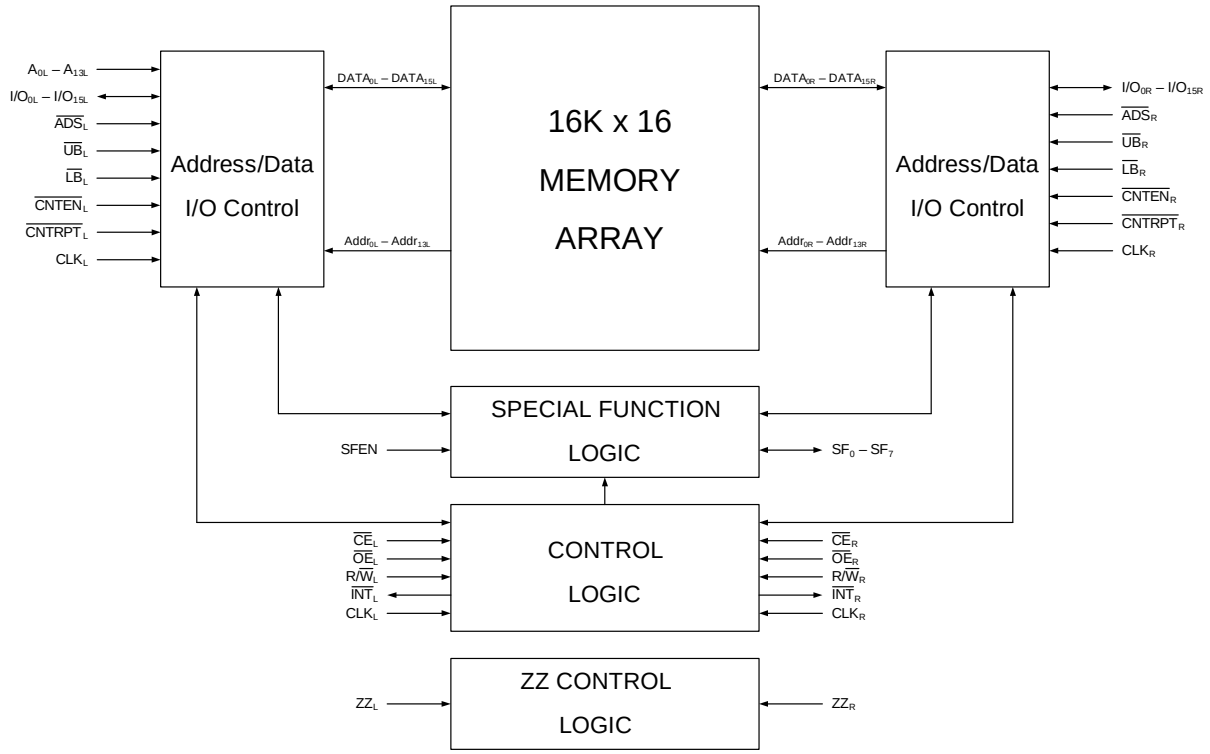
MOBILE MULTIMEDIA INTERFACE (M^2I) VERY LOW POWER 1.8V 16K X 16 SYNCHRONOUS DUAL-PORT STATIC RAM

Final Datasheet
IDT70P9268L

Features

- **True Dual-Ported Memory Cells**
  - Allows simultaneous access of the same memory location
- **High per-port throughput performance**
  - *Industrial: 800 Mbps*
- **Low-Power Operation**
  - *Active: 15 mA (typ.)*
  - *Standby: 2 uA (typ.)*
- **Multiplexed address and data I/Os**
- **Counter enable and repeat features**
- **Full synchronous operation on both ports**
- **Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility**
- **LVTTL-compatible, single 1.8V (+/- 100mV) power supply**
- **Industrial temperature range (-40C to +85C)**
- **Available in a 100-ball fpBGA (fine pitch BGA)**
- **Green parts available, see ordering information**

Block Diagram



NOTES:

1. This block diagram depicts operation with the address and data signals mux'd on the right port but not on the left port. If each port is set to operate with the address and data signals mux'd, then both sides of the block diagram will be the same as the right port pictured above.

Device Description

Designed primarily for use as a high-speed, low-power inter-connect in multi-processor wireless handsets, the IDT70P9268 or Mobile Multimedia Interconnect (M^2I) provides many advantages over embedded serial interfaces, asynchronous memories, and other legacy solutions to inter-processor communication.

Performance

The M^2I supports unparalleled data throughput rates of up to 900 Mbps per port. This is achieved through the implementation of a synchronous architecture which allows the device to support much shorter cycle times (20 ns compared to 55 ns for most low-power asynchronous memories). Additionally, the adoption of a synchronous architecture allows the M^2I to support on-chip counter functionality which helps to eliminate the inefficiencies associated with asynchronous implementations of the address-data-multiplex (ADM) interface. Asynchronous ADM (address-data multiplex) interfaces require the assertion of an external address on one cycle followed by the associated data on the subsequent cycle. This results in an access scheme that imparts a 50% inefficiency into a system already limited by slow cycle times. The M^2I's counter functionality allows a single external address to be asserted on one cycle followed by data being burst into or out of the device on every subsequent cycle. This, when combined with the dramatically improved cycle time, translates to roughly six times greater throughput per-port when compared with asynchronous ADM devices.

Power Consumption

In portable applications, power consumption is of vital concern. This is why the M^2I includes several features targeted at reducing the power consumption of the device itself and the system as a whole. First, the M^2I was designed to consume 40% less operating current than low-power asynchronous memories (15 mA compared to 25 mA). When combined with it's superior performance and counter functionality, which allow it to complete media transfers in fewer cycles, this enables the M^2I to consume nearly 90% less energy than asynchronous memories during transfers of a given file size. Second, the M^2I features port-specific chip-enable and sleep mode pins which allow the two ports of the M^2I to be powered down into standby mode independently of one another. When combined with the M^2I's interrupt flag functionality, this allows the processor subsystems to communicate with one another and to shut off whole portions of the handset which are not in use, dramatically reducing the power consumption of the system.

Flexibility

To help meet the ever changing requirements of wireless handsets, the M^2I has been designed to provide a great deal of flexibility. The M^2I has the ability to support both ADM and traditional SRAM interfaces, allowing it to seamlessly interface with both current and legacy processors. Additionally, the M^2I helps to free up GPIO pins on the processors, allowing designers to include differentiating functionality that helps set their product apart from the competition. By supporting the ADM interface, the M^2I consumes nearly 50% fewer pins per-port than non-multiplexed solutions. The M^2I also frees up additional GPIO pins on the processors by including 8 dynamically programmable GPIO extender pins. These pins allow the processors to offload the need to monitor or control simple, binary state devices (e.g. switches, LED drivers, etc.) to the M^2I and allow the processors to use their GPIO pins for more value added functions.

Pin Configuration

IDT70P9268
BY100
100-BALL fpBGA

A1 V_{SS}	A2 I/O_{0R}	A3 V_{DD}	A4 I/O_{4R}	A5 I/O_{7R}	A6 V_{DD}	A7 I/O_{10R}	A8 V_{DD}	A9 I/O_{15R}	A10 SFEN
B1 $R/\overline{W}_R$	B2 CLK_R	B3 I/O_{1R}	B4 V_{SS}	B5 I/O_{5R}	B6 V_{SS}	B7 I/O_{11R}	B8 V_{SS}	B9 I/O_{14R}	B10 $\overline{OE}_R$
C1 ADS_R	C2 $CNTEN_R$	C3 $CNTRPT_R$	C4 I/O_{2R}	C5 I/O_{6R}	C6 I/O_{8R}	C7 I/O_{12R}	C8 ZZ_R	C9 SF_7	C10 V_{SS}
D1 $\overline{CE}_R$	D2 $\overline{INT}_R$	D3 $\overline{UB}_R$	D4 $\overline{LB}_R$	D5 I/O_{3R}	D6 I/O_{9R}	D7 I/O_{13R}	D8 SF_6	D9 SF_5	D10 SF_4
E1 $\overline{INT}_L$	E2 V_{SS}	E3 V_{DD}	E4 $\overline{UB}_L$	E5 $CNTRPT_L$	E6 SF_0	E7 $MSEL^{(2)}$	E8 V_{DD}	E9 V_{SS}	E10 V_{DD}
F1 $\overline{CE}_L$	F2 $\overline{LB}_L$	F3 $CNTEN_L$	F4 CLK_L	F5 V_{SS}	F6 $A_{13L}^{(3)}$	F7 SF_2	F8 V_{SS}	F9 V_{SS}	F10 SF_1
G1 ADS_L	G2 $A_{0L}^{(3)}$	G3 $A_{3L}^{(3)}$	G4 V_{DD}	G5 I/O_{8L}	G6 I/O_{12L}	G7 $A_{7L}^{(3)}$	G8 ZZ_L	G9 $\overline{OE}_L$	G10 SF_3
H1 $R/\overline{W}_L$	H2 $A_{2L}^{(3)}$	H3 I/O_{0L}	H4 V_{SS}	H5 I/O_{4L}	H6 I/O_{11L}	H7 I/O_{13L}	H8 $A_{9L}^{(3)}$	H9 $A_{12L}^{(3)}$	H10 NC
J1 $A_{1L}^{(3)}$	J2 $A_{5L}^{(3)}$	J3 I/O_{1L}	J4 I/O_{6L}	J5 I/O_{7L}	J6 I/O_{9L}	J7 V_{DD}	J8 I/O_{15L}	J9 $A_{10L}^{(3)}$	J10 $A_{11L}^{(3)}$
K1 $A_{4L}^{(3)}$	K2 $A_{6L}^{(3)}$	K3 I/O_{2L}	K4 I/O_{3L}	K5 I/O_{5L}	K6 V_{DD}	K7 I/O_{10L}	K8 V_{SS}	K9 I/O_{14L}	K10 $A_{8L}^{(3)}$

NOTES:
1. The device setup shown above features multiplexed address and data signals on the right port and non-multiplexed address and data signals on the left port.
2. For multiplexed address and data signal operation on the left port, this pin should be set to V_{DD}. For non-multiplexed address and data signal operation on the left port, this pin should be set to V_{SS}.
3. For multiplexed address and data signal operation on the left port, these pins should be set to V_{SS}.

Pin Names (70P9268)

Left Port	Right Port	Names
CE_L	CE_R	Chip Enable (Input)
R/W_L	R/W_R	Read/Write Enable (Input)
OE_L	OE_R	Output Enable (Input)
$A_{0L} – A_{15L}$	N/A	Address (Input)
$I/O_{0L} – I/O_{15L}$	N/A	Data (Input/Output)
N/A	$I/O+A_{0R} – I/O+A_{15R}$	Multiplexed Address and Data (Input/Output)
CLK_L	CLK_R	Clock (Input)
UB_L	UB_R	Upper Byte Enable (Input)
LB_L	LB_R	Lower Byte Enable (Input)
ADS_L	ADS_R	Address Strobe Enable (Input)
$CNTEN_L$	$CNTEN_R$	Counter Enable (Input)
$CNTRPT_L$	$CNTRPT_R$	Counter Repeat (Input)
INT_L	INT_R	Interrupt Flag (Output)
ZZ_L	ZZ_R	Sleep Mode Enable (Input)
SFEN		Special Function Enable (Input)
SF_{0-7}		Special Function I/O (Input/Output)
M_{SEL}		Left Port Mode Select
V_{DD}		Power (1.8V)
V_{SS}		Ground (0V)

NOTES:
1. The device setup shown above features multiplexed address and data signals on both ports.
2. For non-multiplexed address and data signal operation on the left port, set pin E7 = Vss.

Truth Table I - Read/Write and Enable Control (Multiplexed Port)

OE	CLK	CE	UB	LB	R/W	ADS	ZZ	Upper Byte	Lower Byte	Cycle	Address	Mode
X	↑	H	X	X	X	X	L	High Z	High Z	X	X	Deslected
X	↑	L	H	H	X	X	L	High Z	High Z	X	X	Both bytes deselected
X	↑	L	L	H	L	L	L	--	--	N	A_N	Write to Upper Byte
X	↑	X	X	X	L	H	L	D_{IN}	High Z	N+1	--	
X	↑	L	H	L	L	L	L	--	--	N	A_N	Write to Lower Byte
X	↑	X	X	X	L	H	L	High Z	D_{IN}	N+1	--	
X	↑	L	L	L	L	L	L	--	--	N	A_N	Write to Both Bytes
X	↑	X	X	X	L	H	L	D_{IN}	D_{IN}	N+1	--	
H	↑	L	L	H	H	L	L	--	--	N	A_N	Read Upper Byte Only
L	↑	X	X	X	H	H	L	D_{OUT}	High Z	N+2	--	
H	↑	L	H	L	H	L	L	--	--	N	A_N	Read Lower Byte Only
L	↑	X	X	X	H	H	L	High Z	D_{OUT}	N+2	--	
H	↑	L	L	L	H	L	L	--	--	N	A_N	Read Both Bytes
L	↑	X	X	X	H	H	L	D_{OUT}	D_{OUT}	N+2	--	
H	↑	L	L	L	X	H	L	High Z	High Z	X	X	Outputs Disabled
X	X	X	X	X	X	X	H	High Z	High Z	X	X	Sleep Mode – Power down

Truth Table II - Read/Write and Enable Control (Non-Multiplexed Port)

OE	CLK	CE	UB	LB	R/W	ZZ	Upper Byte I/O	Lower Byte I/O	Mode
X	↑	H	X	X	X	L	High Z	High Z	Deselected
X	↑	L	H	H	X	L	High Z	High Z	Both Bytes Deselected
X	↑	L	L	H	L	L	D_{IN}	High Z	Write To Upper Byte Only
X	↑	L	H	L	L	L	High Z	D_{IN}	Write to Lower Byte Only
X	↑	L	L	L	L	L	D_{IN}	D_{IN}	Write to Both Bytes
L	↑	L	L	H	H	L	D_{OUT}	High Z	Read Upper Byte Only
L	↑	L	H	L	H	L	High Z	D_{OUT}	Read Lower Byte Only
L	↑	L	L	L	H	L	D_{OUT}	D_{OUT}	Read Both Bytes
H	↑	L	L	L	X	L	High Z	High Z	Outputs Disabled
X	X	X	X	X	X	H	High Z	High Z	Sleep Mode – Power Down

Truth Table III - Address Counter Control

External Address	Previous Internal Address	Internal Address Used	CLK	ADS	CNTEN	CNTRPT	Mode
A_n	X	A_n	↑	L	X	H	External Address Used
X	A_n	A_{n+1}	↑	H	L	H	Counter Enabled – Internal Address Generation
X	A_{n+1}	A_{n+1}	↑	H	H	H	External Address Blocked – Counter Disabled (A_{n+1} reused)
X	X	A_n	↑	X	X	L	Counter Reset to Last External Address Loaded

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	VDD
Industrial	-40°C to +85°C	0V	1.8V +/- 100mV

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	1.2	--	V_{DD} + 0.2	V
V_{IL}	Input Low Voltage	-0.2	--	0.4	V

Absolute Maximum Ratings

Symbol	Rating	Industrial	Unit
V_{DD}	Voltage on Input, Output and I/O Terminals with Respect to V_{SS}	-0.5V to V_{DD} +0.3V	V
V_{TERM}	Terminal Voltage with Respect to GND	-0.5V to +2.9V	V
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
T_{JN}	Junction Temperature	+150	°C
I_{OUT}	DC Output Current	20	mA

Capacitance

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	VIN = 0V	9	PF
C_{OUT}	Output Capacitance	VOUT = 0V	11	PF

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 1.8V +/- 100mV)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{IN} = V_{SS} to V_{DD}	--	1	Ua
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}x = V_{IH}$ or $\overline{OE}x = V_{IH}$ or $V_{OUT} = V_{SS}$ to V_{DD}	--	1	UA
V_{OL}	Output Low Voltage	I_{OL} = 0.1mA, V_{DD} = Min	--	0.2	V
V_{OH}	Output High Voltage	I_{OH} = -0.1mA, V_{DD} = Min	V_{DD} – 0.2V	--	V
V_{OLSF}	Output Low Voltage	I_{OL} = 4mA, V_{DD} = Min	--	0.4	V

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 1.8V +/- 100mV)

Symbol	Parameter	Test Conditions	70P9268	
			Typ.	Max.
I_{DD}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$, Outputs Disabled, f = f_{MAX}(1)	15 mA	25 mA
I_{SB1}	Standby Current (Both Ports – TTL Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$, Outputs Disabled, f = f_{MAX}(1)	2 mA	4 mA
I_{SB2}	Standby Current (One Port – TTL Inputs)	$\overline{CE}_{"A"} = V_{IL}$ and $\overline{CE}_{"B"} = V_{IH}$, Active Port Outputs Disabled, f = f_{MAX}(1)	3 mA	5 mA
I_{SB3}	Full Standby Current (Both Ports CMOS Inputs)	Both Ports Outputs Disabled $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$, or $V_{IN} \leq 0.2V$, f = 0(2)	2 uA	8 uA
I_{SB4}	Full Standby Current (One Port – CMOS Inputs)	$\overline{CE}_{"A"} \leq 0.2V$ and $\overline{CE}_{"B"} \geq V_{DD} - 0.2V$, $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$, Active Port Outputs Disabled, f = f_{MAX}(1)	3 mA	5 mA
I_{ZZ}	Sleep Mode Current	ZZ_L and $ZZ_R > V_{DD} - 0.2V$	2 uA	8 uA

NOTES:

1. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 1.8V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

AC Test Conditions

Input Pulse Levels	V_{SS} to V_{DD}
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	V_{DD}/2
Output Reference Levels	V_{DD}/2
Output Load	Figure 1

1.8V	
R1	13500Ω
R2	13500Ω

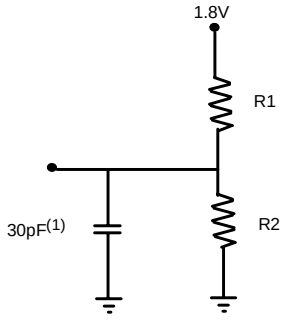


Figure 1. AC Output Test Level
(5pF for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})

AC Electrical Characteristics Over the Operating Temperature Range

(Read and Write Cycle Timing for Multiplexed Port) (V_{DD} = 1.8V +/- 100mV)

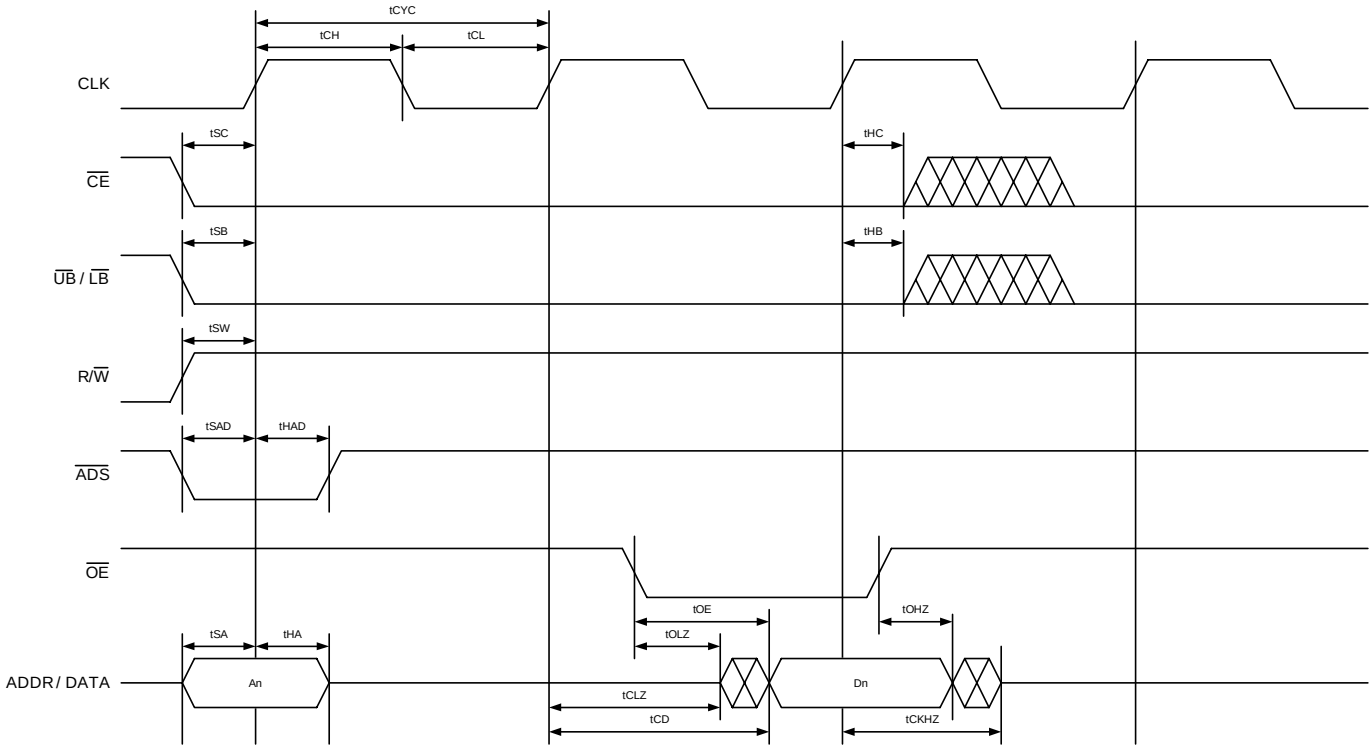
		70P9268L Ind. Only	
Symbol	Parameter	Min.	Max.
t_{CYC}	Clock Cycle Time	20	--
t_{CH}	Clock High Time	8	--
t_{CL}	Clock Low Time	8	--
t_R	Clock Rise Time	--	3
t_F	Clock Fall Time	--	3
t_{SA}	Address Setup Time	5	--
t_{HA}	Address Hold Time	1	--
t_{SC}	Chip Enable Setup Time	5	--
t_{HC}	Chip Enable Hold Time	1	--
t_{SW}	R/W Setup Time	5	--
t_{HW}	R/W Hold Time	1	--
t_{SD}	Input Data Setup Time	5	--
t_{HD}	Input Data Hold Time	1	--
t_{SAD}	ADS Setup Time	5	--
t_{HAD}	ADS Hold Time	1	--
t_{SCN}	CNTEN Setup Time	5	--
t_{HCN}	CNTEN Hold Time	1	--
t_{SRST}	CNTRST Setup Time	5	--
t_{HRST}	CNTRST Hold Time	1	--
t_{OE}	Output Enable to Data Valid	--	10
t_{OLZ}	Output Enable to High Z	2	--
t_{OHZ}	Output Enable to Low Z	--	10
t_{CD}	Clock to Data Valid	--	12
t_{DC}	Data Output Hold After Clock High	2	--
t_{CKHZ}	Clock High to Output High Z	2	9
t_{CKLZ}	Clock High to Output Low Z	2	--
t_{INS}	Interrupt Flag Set Time	12	--
t_{INR}	Interrupt Flag Reset Time	12	--
t_{CO}	Clock to Clock Offset	5	--

AC Electrical Characteristics Over the Operating Temperature Range

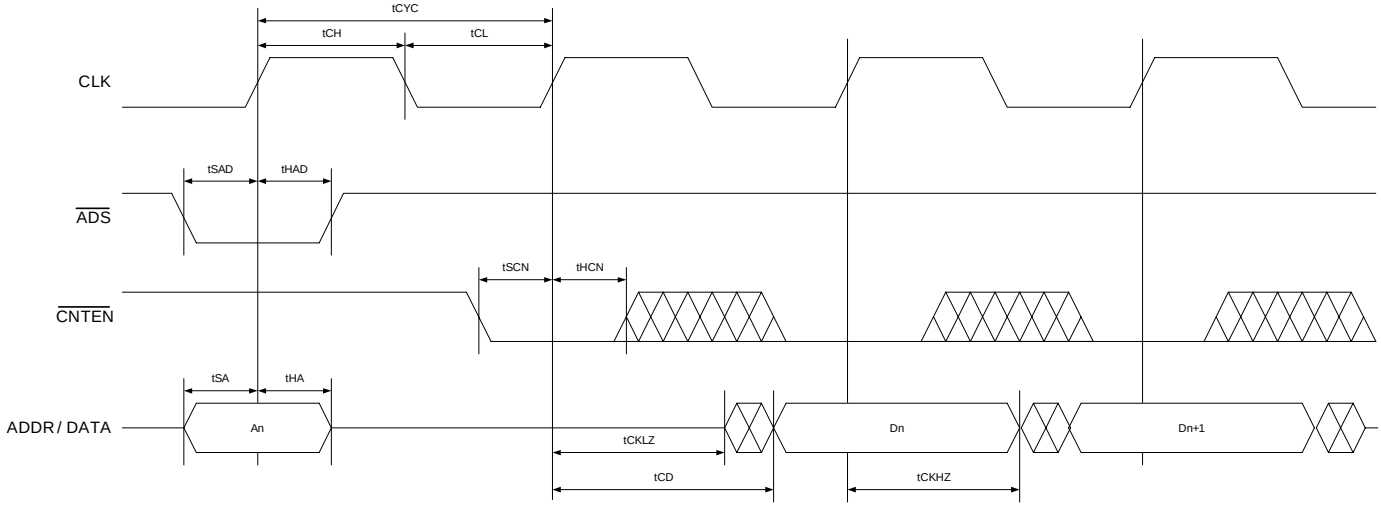
(Read and Write Cycle Timing for Non-Multiplexed Port) (V_{DD} = 1.8V +/- 100mV)

		70P9268L Ind. Only	
Symbol	Parameter	Min.	Max.
t_{CYC}	Clock Cycle Time	20	--
t_{CH}	Clock High Time	8	--
t_{CL}	Clock Low Time	8	--
t_R	Clock Rise Time	--	3
t_F	Clock Fall Time	--	3
t_{SA}	Address Setup Time	5	--
t_{HA}	Address Hold Time	1	--
t_{SC}	Chip Enable Setup Time	5	--
t_{HC}	Chip Enable Hold Time	1	--
t_{SW}	R/W Setup Time	5	--
t_{HW}	R/W Hold Time	1	--
t_{SD}	Input Data Setup Time	5	--
t_{HD}	Input Data Hold Time	1	--
t_{SAD}	ADS Setup Time	5	--
t_{HAD}	ADS Hold Time	1	--
t_{SCN}	CNTEN Setup Time	5	--
t_{HCN}	CNTEN Hold Time	1	--
t_{SRST}	CNTRST Setup Time	5	--
t_{HRST}	CNTRST Hold Time	1	--
t_{OLZ}	Output Enable to Low Z	2	--
t_{OHZ}	Output Enable to High Z	--	10
t_{CD}	Clock to Data Valid	--	12
t_{DC}	Data Output Hold After Clock High	2	--
t_{CKHZ}	Clock High to Output High Z	2	10
t_{CKLZ}	Clock High to Output Low Z	2	--
t_{INS}	Interrupt Flag Set Time	12	--
t_{INR}	Interrupt Flag Reset Time	12	--
t_{CO}	Clock to Clock Offset	5	--

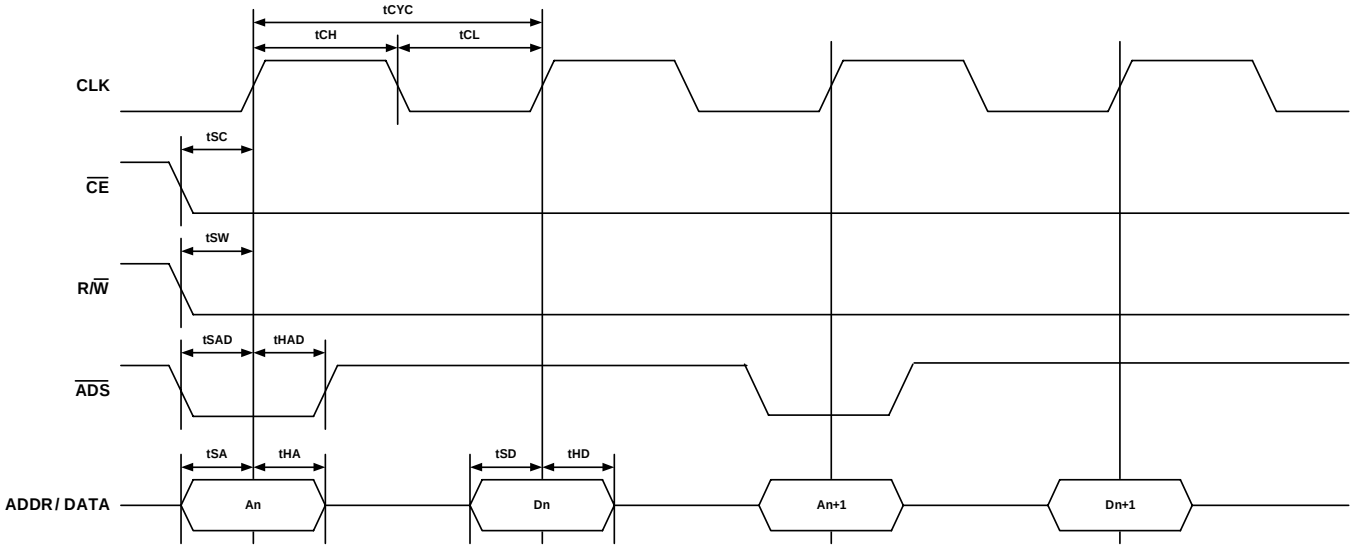
Timing Waveform for Mux'd Port Single Read Cycle



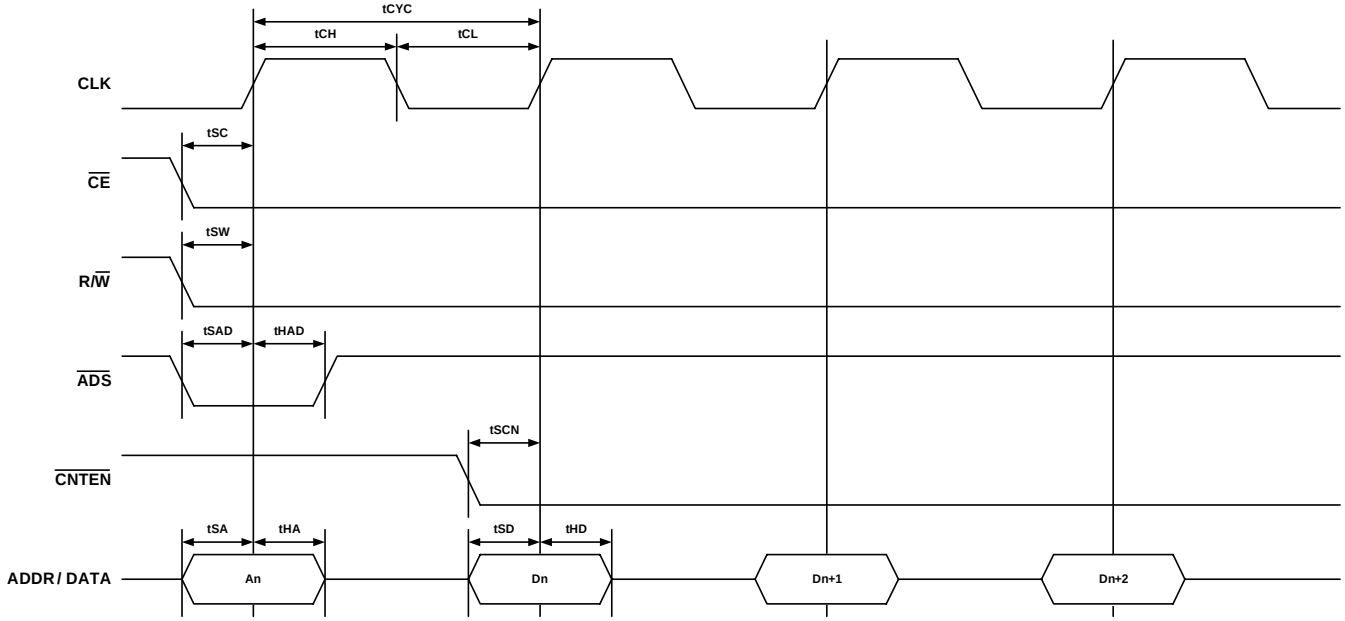
Timing Waveform for Mux'd Port Burst Read Cycle



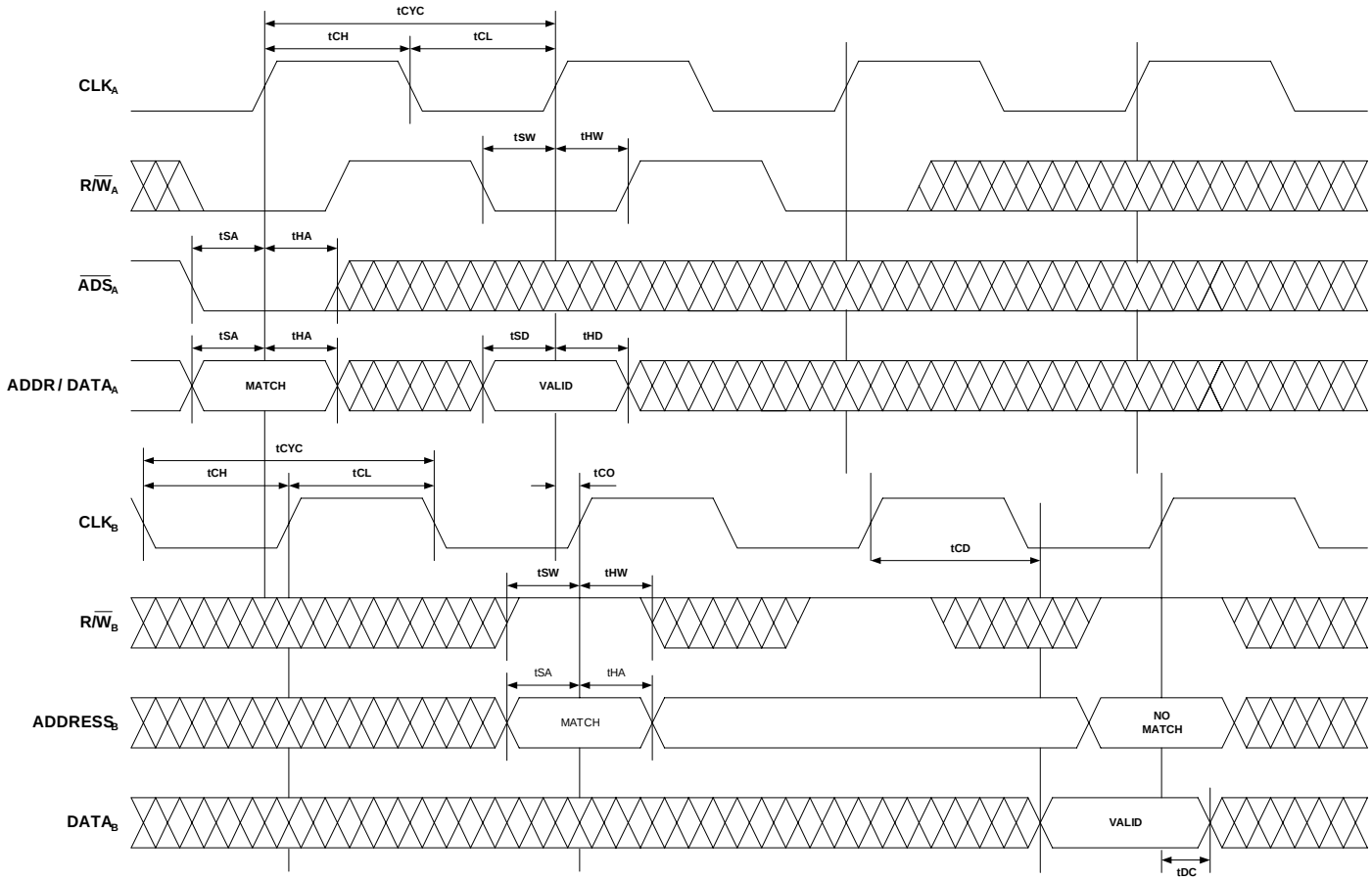
Timing Waveform for Mux'd Port Single Write Cycle



Timing Waveform for Mux'd Port Burst Write Cycle



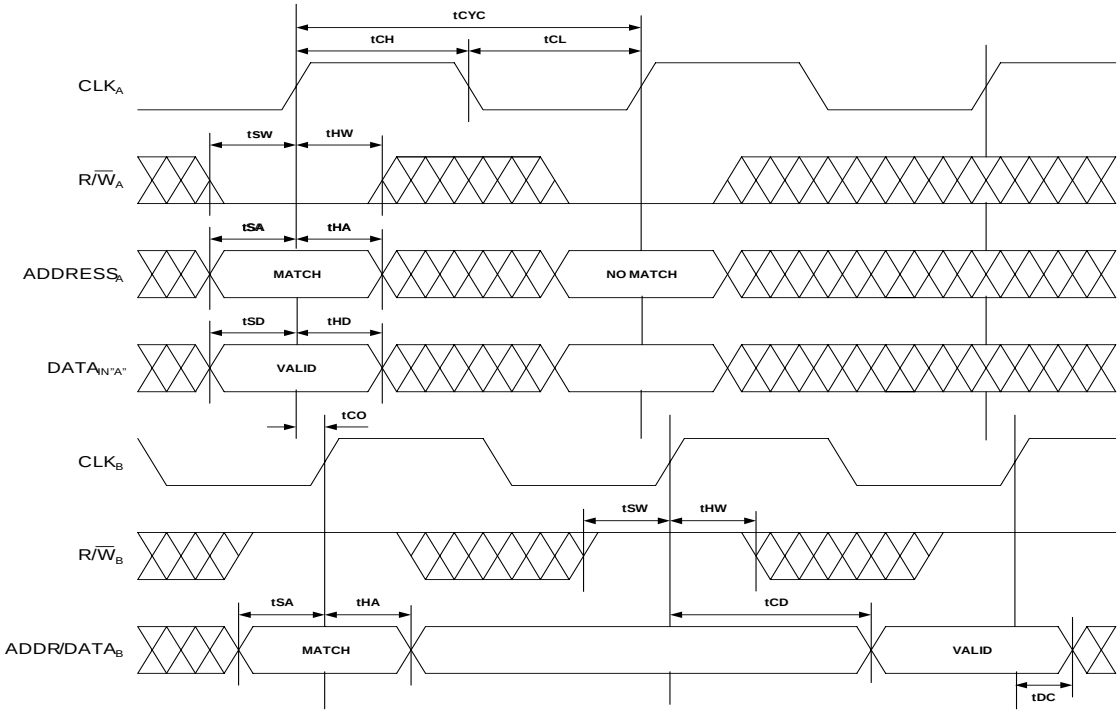
Timing Waveform of Mux'd Port Write to Non-Mux'd Port Read



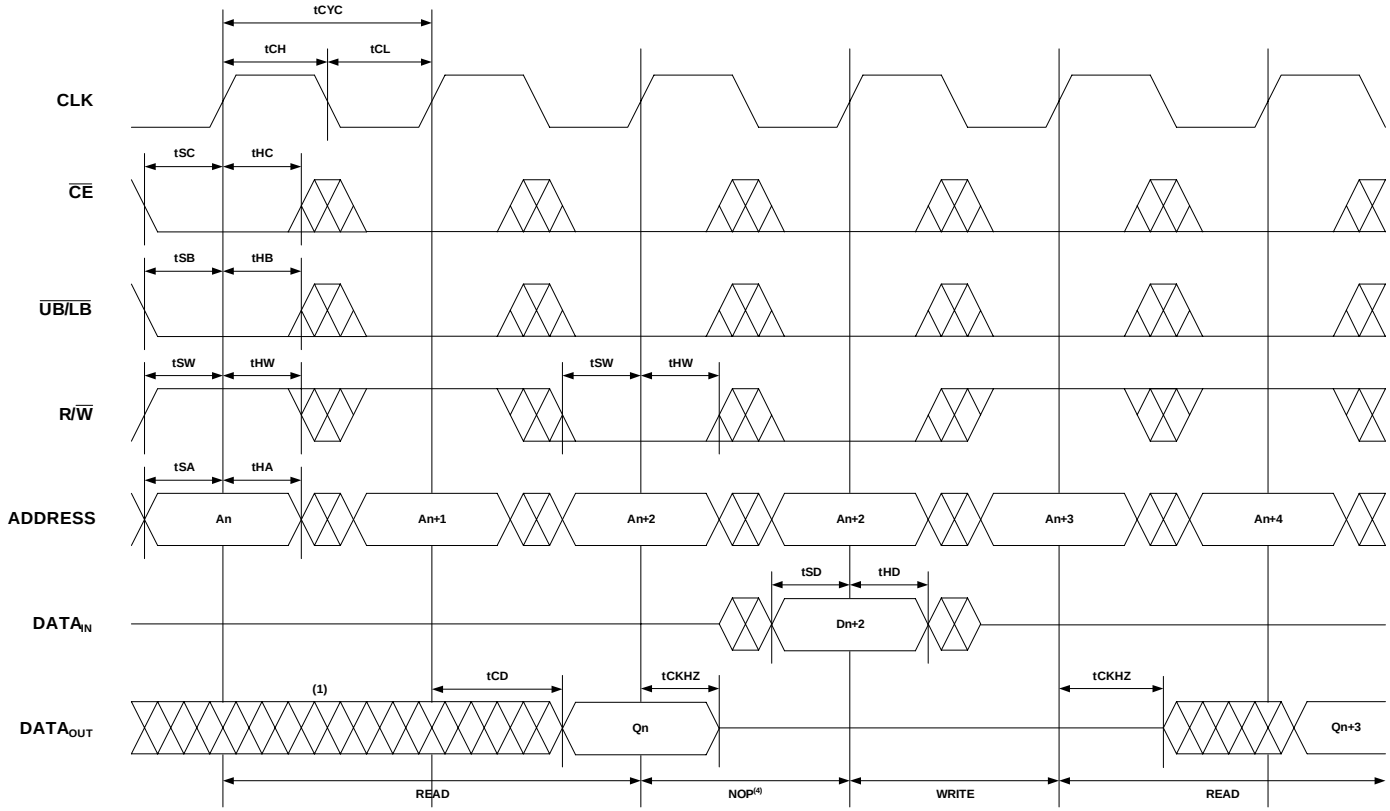
NOTES:

1. $\overline{CE}$, $\overline{UB}/\overline{LB}_n$ = V_{IL}; $\overline{CNTEN}$ and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{OE}$ = V_{IL} for Port, which is being read from. $\overline{OE}$ = V_{IH} for Mux'd Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Non-Mux'd Port read is not valid until following Non-Mux'd Port clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + 2\ t_{CYC2} + t_{CD2}$). If t_{CO} > minimum, then data from Non-Mux'd Port read is available on first Non-Mux'd Port clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).

Timing Waveform of Non-Mux'd Port Write to Mux'd Port Read



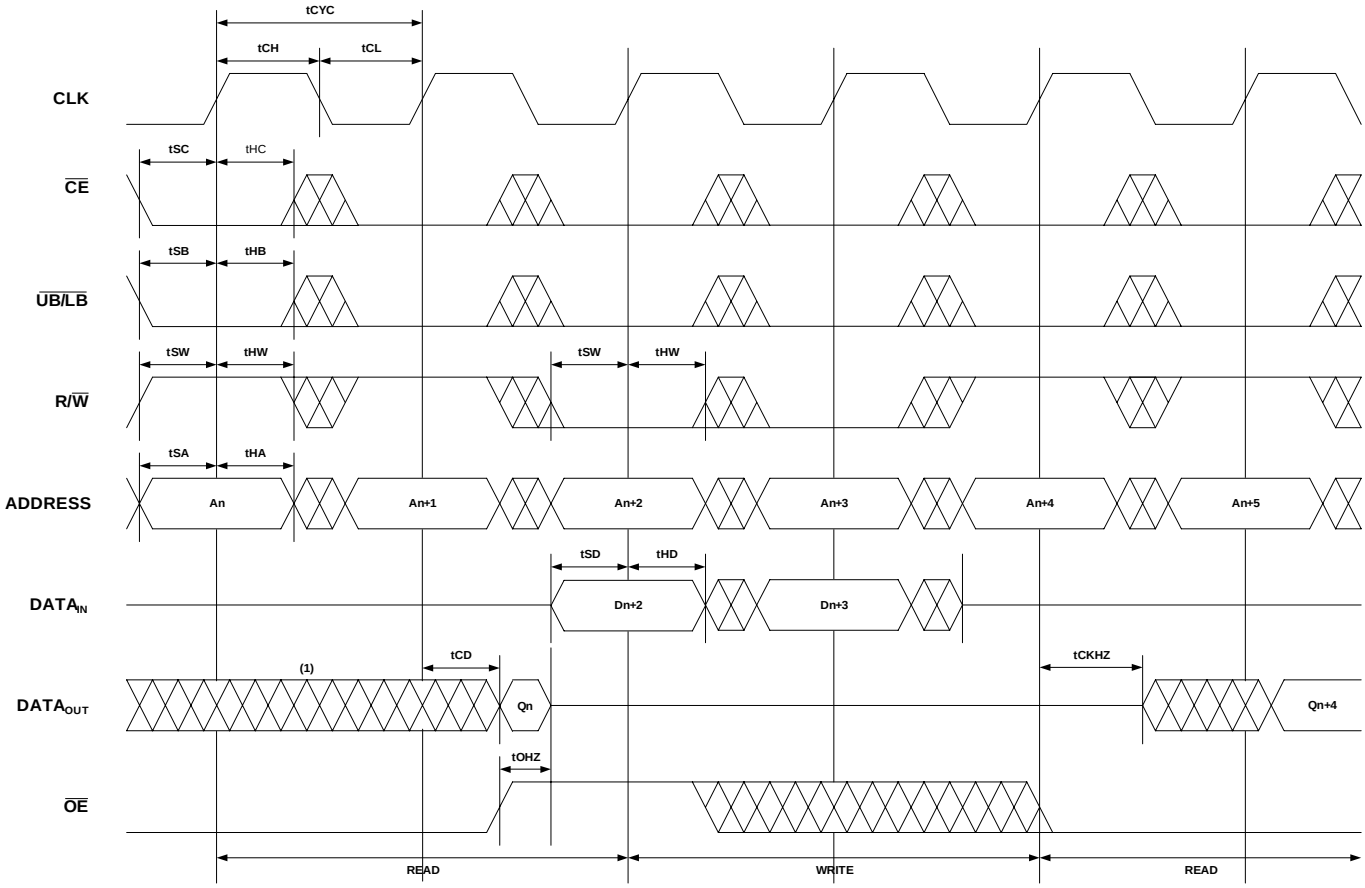
Timing Waveform of Non-Mux'd Port Read-to-Write-to-Read



NOTES:

1. Output $\overline{UB}/\overline{LB}$ state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE}$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{REPEAT}$ = V_{IH}. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Non-Mux'd Port Read-to-Write-to-Read (OE Controlled)



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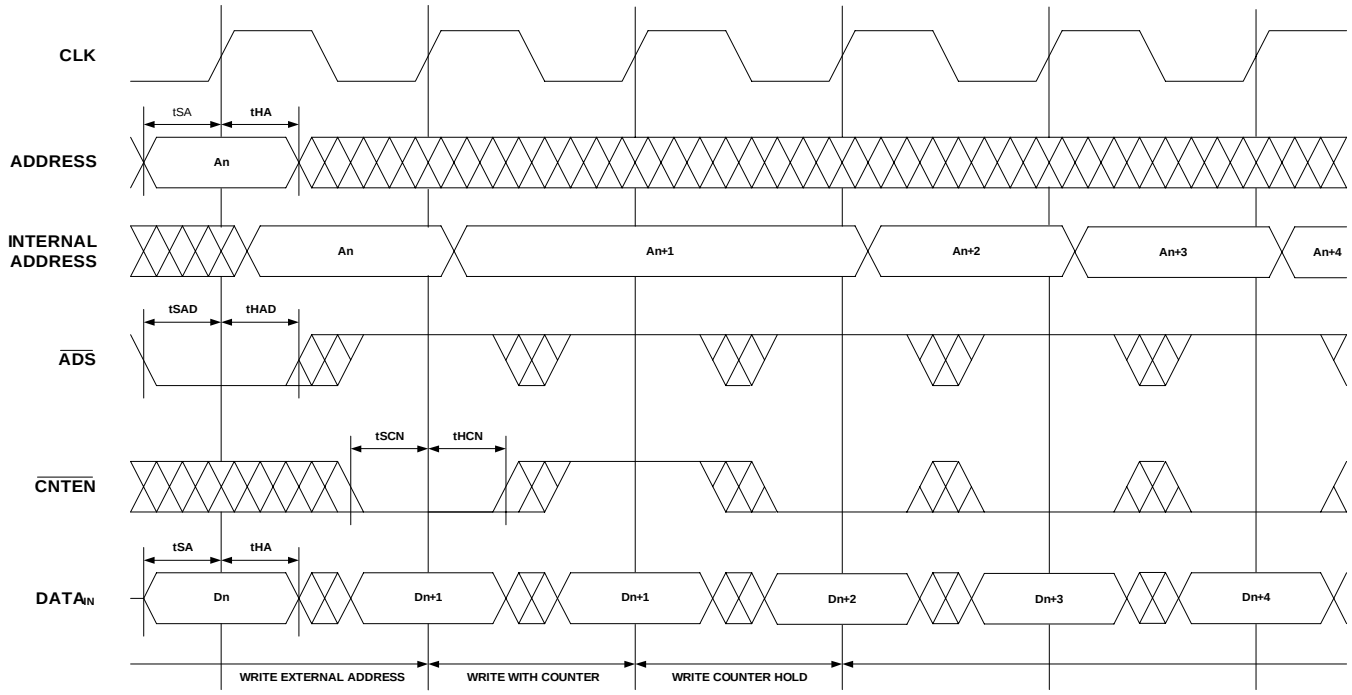
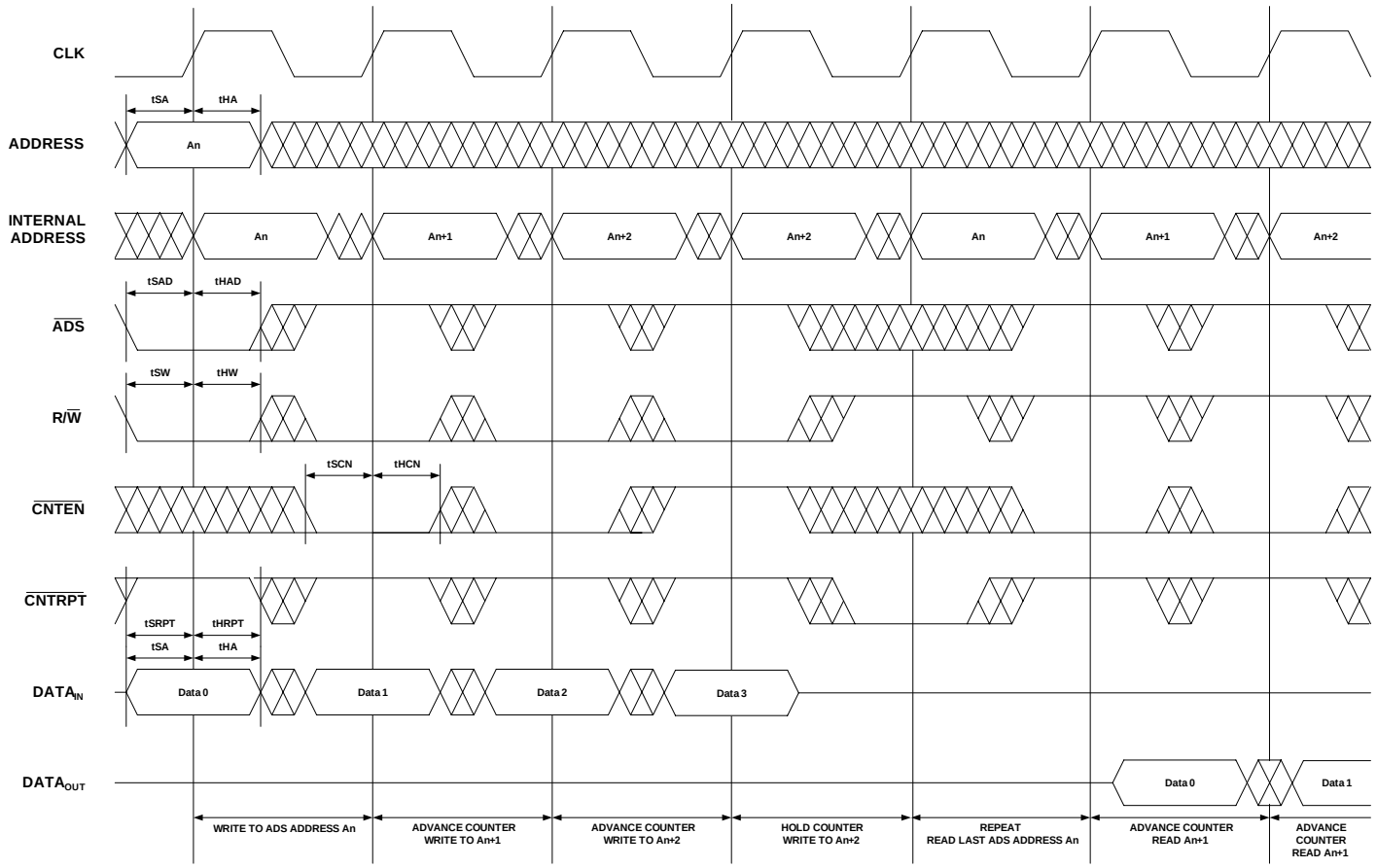
3. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK; numbers are for reference use only.

Timing Waveform of Non-Mux'd Port Write with Counter Advance



NOTES:
1. $\overline{CE}$, $\overline{UB}$/$\overline{LB}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{REPEAT}$ = V_{IH}.
2. $\overline{CE}$, $\overline{UB}$/$\overline{LB}$ = V_{IL}.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
4. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

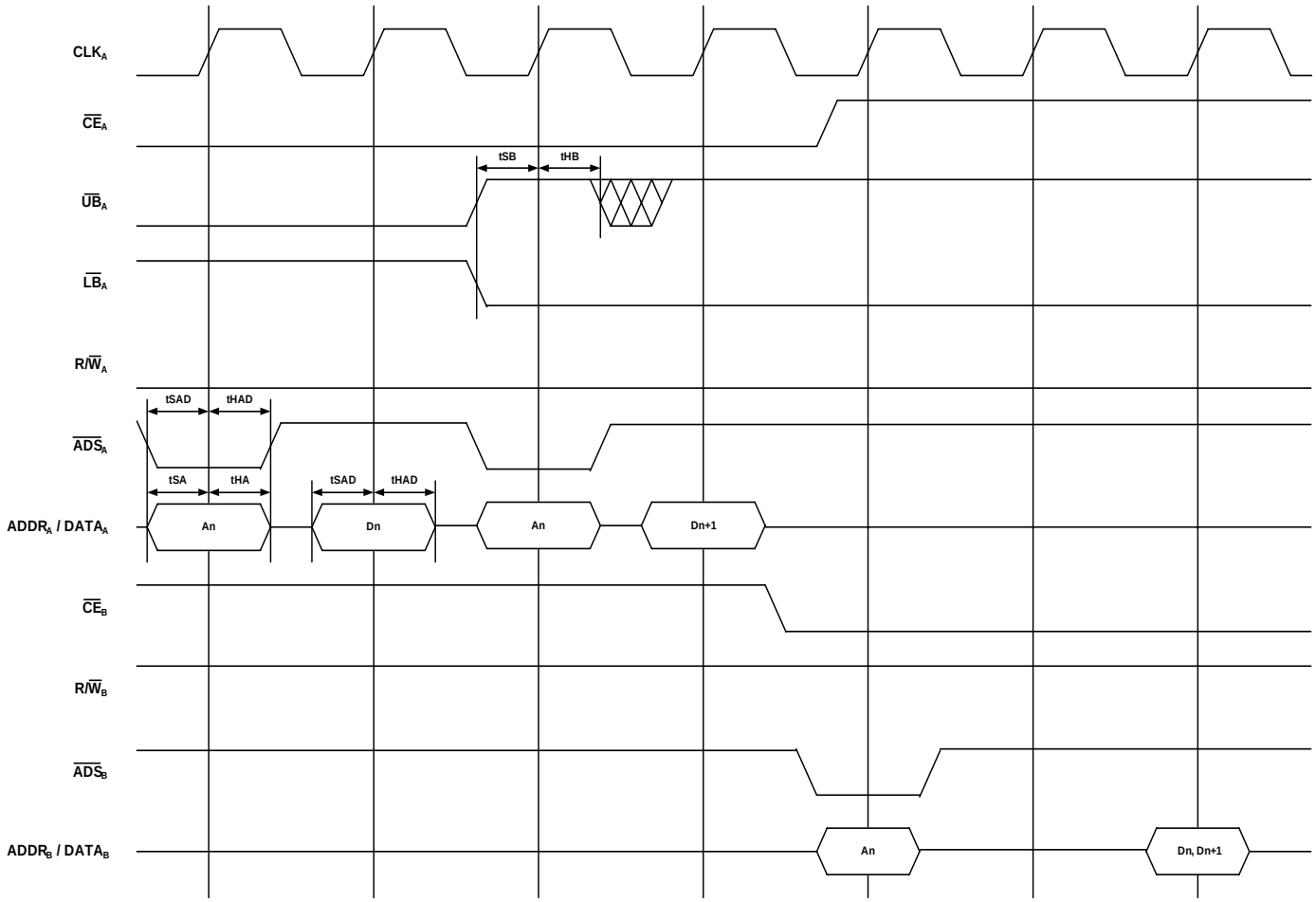
Timing Waveform of Non-Mux'd Port Operation with Counter Repeat



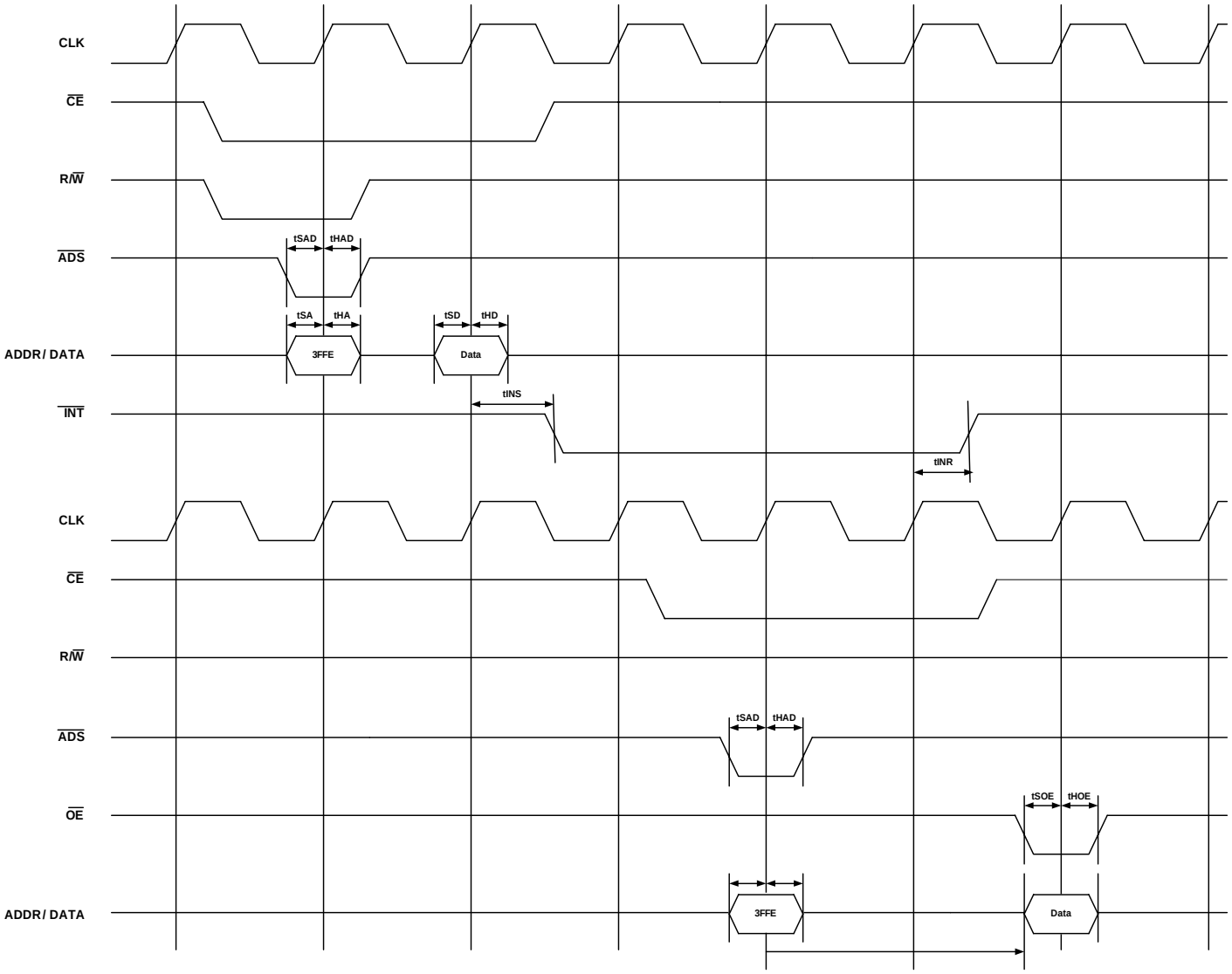
NOTES:

1. $\overline{CE}$, $\overline{UB}$/$\overline{LB}$ = V_{IL}.
2. The "Internal Address" is equal to the "External Address" when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.
3. No dead cycle exists during $\overline{CNTRPT}$ operation. A READ or WRITE cycle may be coincidental with the counter $\overline{CNTRPT}$ cycle: Address loaded by last valid $\overline{ADS}$ load will be accessed.
4. $\overline{CNTEN}$ = V_{IL} advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1'Address is written to during this cycle.

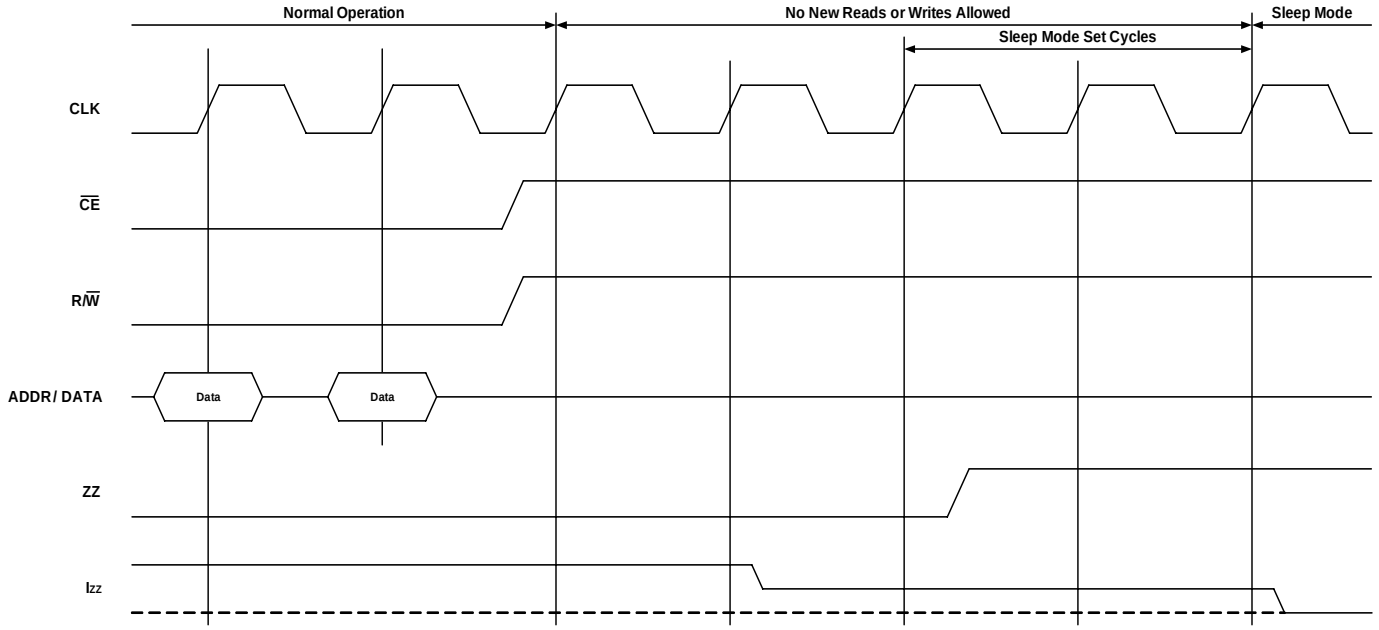
Timing Waveform for x8 to x16 Bus Matching



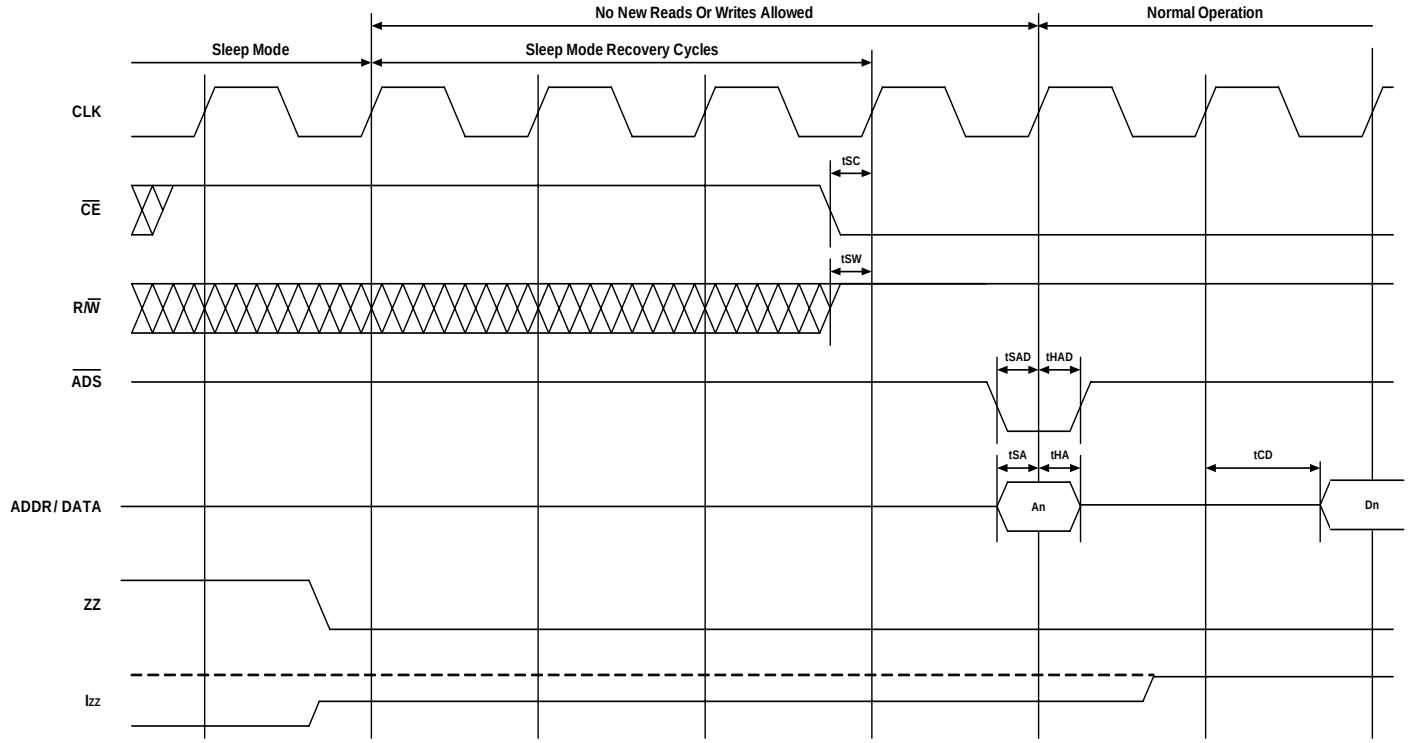
Timing Waveform - Interrupt Timing



Timing Waveform - Entering Sleep Mode



Timing Waveform - Exiting Sleep Mode



Functional Description

The 70P9268L provides a true synchronous multiplexed and non-multiplexed Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. Counter enable and counter repeat inputs are provided to facilitate burst reads and writes to the memory.

Synchronous Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (INT_L) is asserted when the right port writes to memory location 3FFE (HEX), where a write is defined as CE_R = $R/\overline{W}_R$ = V_{IL}. The left port clears the interrupt through access of address location 3FFE when CE_L = V_{IL}, $R/\overline{W}_L$ = V_{IH}. Likewise, the right port interrupt flag (INT_R) is asserted when the left port writes to memory location 3FFF (HEX) and to clear the interrupt flag (INT_R), the right port must read the memory location 3FFF. The message (16 bits) at 3FFE or 3FFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address, locations 3FFE and 3FFF are not used as mail boxes, but as part of the random access memory.

Truth Table IV - Interrupt Flag

Left Port					Right Port					Function
CLK_L	R/W_L	CE_L	ADD_L	INT_L	CLK_R	R/W_R	CE_R	ADD_R	INT_R	
↑	L	L	3FFF	X	↑	X	X	X	L	Set Right INTR Flag
↑	X	X	X	X	↑	H	L	3FFF	H	Reset Right INTR Flag
↑	X	X	X	L	↑	L	L	3FFE	X	Set Left INTL Flag
↑	H	L	3FFE	H	↑	X	X	X	X	Reset Left INTL Flag

Advanced Input Read and Output Drive Registers

The IDT70P9268L is equipped with 8 Special Function (SF_X) pins that can be programmed to function as either Input Read Register (IRR) or Output Drive Register (ODR) pins. IRR pins allow the user to capture the status of external binary state devices and report that status to a processor, ASIC, FPGA, etc. via a standard read access from either port. ODR pins allow the user to monitor and control the state of external binary state devices via standard reads and writes from either port. The functionality of the SF pins are determined by the status of the Pin Direction Register (PDR). Refer to Truth Table V for information on programming the PDR and operating the special function pins.

Truth Table V - Input Read and Output Drive Registers

SFEN	ADDR	R/W	I/O0 – I/O7	I/O8	I/O9 – I/O15	Function
L	0	L	Note 1	H	X	Program Pin Direction Register
L	0	H	Note 2	Note 3	Note 3	Reading the status of SFn and PDRn
L	0	L	Note 4	L	X	Write to Output Drive Register

NOTES:

1. If I/On = H, SFn is programmed as an output and I/On will be used to read and write to this ODR location during subsequent transactions when I/O_8 = L. If I/On= L, SFn is programmed as an input and I/On will be used to read this IRR location during subsequent reads where I/O_8 = L.
2. For n = 0-7. If PDRn = 0, I/On = IRRn (the registered value of SFn). If PDRn = 1, I/On = ODRn (the value last written to ODRn).
3. For n = 8-15, I/On = PDRn-8.
4. For I/O_0 - I/O_7, the value written to I/On will be input to each ODRn location (where PDRn = 1) with a "1" corresponding to "on" and a "0" corresponding to "off".

Special Function I/O Operation

I/O	Function
0 – 7	With SFEN = L, I/O_8 = H, the value written to address 0 on I/On will determine the status of PDRn (1 = output, 0 = input). With SFEN = L, I/O_8 = L, the value written to address 0 on I/On will be input to the corresponding ODRn location (1 = on, 0 = off).
8	With SFEN = L, writing a "0" to address 0 on this I/O causes the values of I/O_0 – I/O_7 to be input to their corresponding ODR locations. With SFEN = L, writing a "1" to address 0 on this I/O causes the values of I/O_0 – I/O_7 to be input to their corresponding PDR locations, which in turn determine whether SF_0 – SF_7 are individually programmed to be inputs (IRR) or outputs (ODR).
9 – 15	With SFEN = L, reads to address 0 will output the status of the PDR, where I/On = PDRn-8

The PDR determines whether the SF_X pins will operate as IRR or ODR. The PDR is programmed by writing to address x0000 with SFEN = V_{IL} and I/O_8 = H. Writing a "0" to I/O_X will set SF_X to be an IRR pin. Writing a "1" to I/O_X will set SF_X to be an ODR pin.

The status of the Special Function pins and the PDR can be read as a standard memory access to address x0000 from either port and the data is output via the standard I/Os (Truth Table V). During Special Function reads I/O_0 - I/O_7 output the status of the Special Function pins with I/On corresponding to SFn. I/O_8 - I/O_{15} outputs the status of the Pin Direction Register with I/On = PDRn-8.

For SF pins set to ODR operation, the status of these pins is determined by using standard write accesses from either port to address x0000 with SFEN = V_{IL} and I/O_8 = L. A written "1" will correspond to "on" for the connected binary state device and a written "0" will correspond to "off".

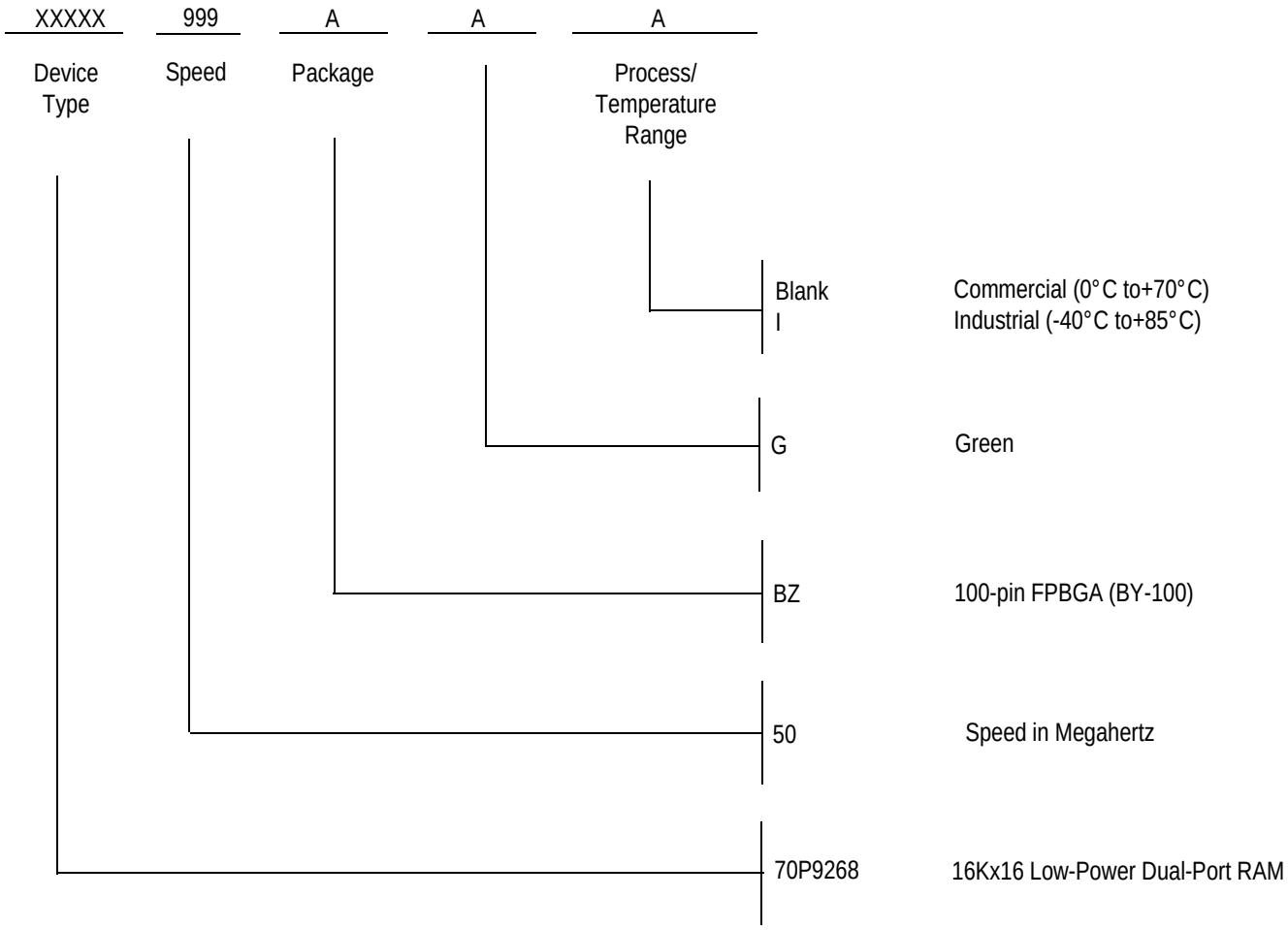
Sleep Mode

The IDT70P9268 is equipped with an optional sleep or low-power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ-pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ (ZZ_X = V_{IH}) and three cycles after de-asserting ZZ (ZZ_X = V_{IL}), the device must be disabled via the chip enable pins. If a write or a read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode ($R/\overline{W}_X$ = V_{IH}) when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.

Ordering Information



Final Datasheet: **Definition**

"Final" datasheets contain descriptions for products that are in full release.

Revision History

02/06/07: Initial Release

08/21/07: Final Datasheet. Initial Release

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