



Functional Description

The PEEL™ 16CV8 implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of macrocells further increase logic flexibility.

Architecture Overview

The PEEL™ 16CV8 features ten dedicated input pins and eight I/O pins, which allow a total of up to 16 inputs and 8 outputs for creating logic functions. At the core of the device is a programmable electrically-erasable AND array which drives a fixed OR array. With this structure the PEEL™ 16CV8 can implement up to 8 sum-of-products logic expressions.

Associated with each of the eight OR functions is a macrocell which can be independently programmed to one of up to four different basic configurations. The programmable macrocells allow each I/O to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing two possible feedback paths into the array.

Three different device modes, Simple, Complex, and Registered, support various user configurations. In Simple mode a macrocell can be configured for combinatorial function with the output buffer permanently enabled, or the output buffer can be disabled and the I/O pin used as a dedicated input. In Complex mode a macrocell is configured for combinatorial function with the output buffer enable controlled by a product term. In Registered mode, a macrocell can be configured for registered operation with the register clock and output buffer enable controlled directly from pins, or can be configured for combinatorial function with the output buffer enable controlled by a product term. In most cases the device mode is set automatically by the development software, based on the features specified in the design.

The three device modes support designs created explicitly for the PEEL™ 16CV8, as well as designs created originally for popular PLD devices such as the 16R4, 16R8, and 16L8. Table 1 shows the device mode used to emulate the various PLDs. Design conversion into the 16CV8 is accommodated by JEDEC-to-JEDEC translators available from ICT, as well as several programmers which can read the original PLD JEDEC file and automatically program the 16CV8 to perform the same function.

AND/OR Logic Array

The programmable AND array of the PEEL™ 16CV8 is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

- **32 input lines:**
 - 16 input lines carry the true and complement of the signals applied to the 8 dedicated input pins
 - 16 additional lines carry the true and complement of 8 macrocell feedback signals or inputs from I/O pins or the clock/ OE pins

- **64 product terms:**
 - 56 product terms (arranged in 8 groups of 7) form sum-of-product functions for macrocell combinatorial or registered logic
 - 8 product terms (arranged 1 per macrocell) add an additional product term for macrocell sum-of-products functions or I/O pin output enable control

At each input-line/product-term intersection there is an EEPROM memory cell which determines whether or not there is a logical connection at that intersection. Each product term is essentially a 32-input AND gate. A product term which is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, that term will always be TRUE.

When programming the PEEL™ 16CV8, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that PEEL™ device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function.)

Table 1 : PEEL™ 16CV8 Device Compatibility

PLD Architecture Compatibility	PEEL™ 16CV8 Device Mode
10H8	Simple
10L8	Simple
10P8	Simple
12H6	Simple
12L6	Simple
12P6	Simple
14H4	Simple
14L4	Simple
14P4	Simple
16H2	Simple
16HD8	Simple
16L2	Simple
16LD8	Simple
16P2	Simple
16H8	Complex
16L8	Complex
16P8	Complex
16R4	Registered
16R6	Registered
16R8	Registered
16RP4	Registered

Table 1 : PEEL™ 16CV8 Device Compatibility

PLD Architecture Compatibility	PEEL™ 16CV8 Device Mode
16RP6	Registered
14RP8	Registered

Programmable Macrocell

The macrocell provides complete control over the architecture of each output. The ability to configure each output independently permits users to tailor the configuration of the PEEL™ 16CV8 to the precise requirements of their designs.

Macrocell Architecture

Each macrocell consists of an OR function, a D-type flip-flop, an output polarity selector, and a programmable feedback path. Four EEPROM architecture bits MS0, MS1, OP, and RC control the configuration of each macrocell. Bits MS0 and MS1 are global, and select between Simple, Complex, and Registered mode for the whole device. Bits OP and RC are local for each macrocell; bit OP controls the output polarity and bit RC selects between registered and combinatorial operation and also specifies the feedback path. Table 2 shows the architecture bit settings for each possible configuration.

Equivalent circuits for the possible macrocell configurations are illustrated in Figures 3, 4, and 5. When creating a PEEL™ device design, the desired macrocell configuration generally is specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

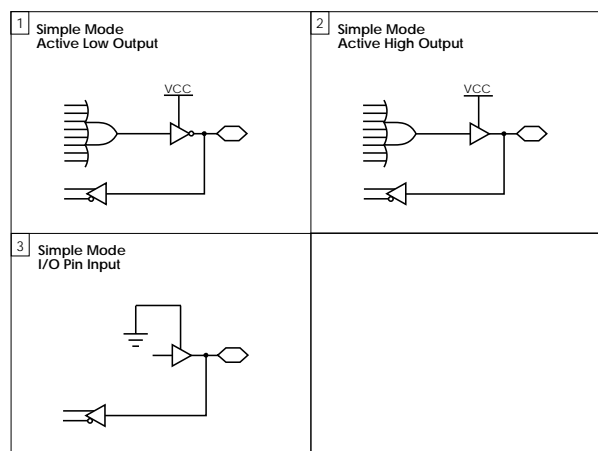
Table 2 : PEEL™ 16CV8 Device Mode/Macrocell Configuration Bits

Config. #	Mode	Architecture Bits				Function	Polarity	Feedback
		MS0	MS1	OP	RC			
1	Simple	1	0	0	0	Combinatorial	Active Low	I/O Pin
2	Simple	1	0	1	0	Combinatorial	Active High	I/O Pin
3	Simple	1	0	X	1	None	None	I/O Pin
1	Complex	1	1	0	1	Combinatorial	Active Low	I/O Pin
2	Complex	1	1	1	1	Combinatorial	Active High	I/O Pin
1	Registered	0	1	0	0	Registered	Active Low	Registered
2	Registered	0	1	1	0	Registered	Active High	Registered
3	Registered	0	1	0	1	Combinatorial	Active Low	I/O Pin
4	Registered	0	1	1	1	Combinatorial	Active High	I/O Pin

Simple Mode

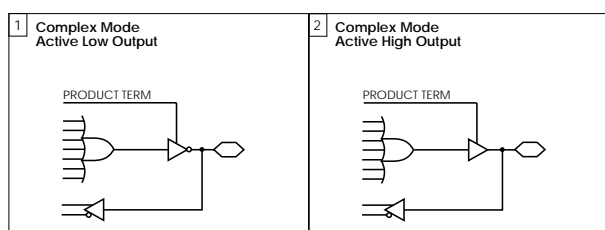
In Simple mode, all eight product terms feed the OR array which can generate a purely combinatorial function for the output pin. The programmable output polarity selector allows active-high or active-low logic, eliminating the need for external inverters. For output functions, the buffer can be permanently enabled. Feedback into the array is available on all macrocell I/O pins, except for pins 15 and 16. Figure 6 shows the logic array of the PEEL™ 16CV8 configured in Simple mode.

Simple mode also provides the option of configuring an I/O pin as a dedicated input. In this case, the output buffer is permanently disabled, and the I/O pin feedback is used to bring the input signal from the pin into the logic array. This option is available for all I/O pins except pins 15 and 16. Figure 3 shows the possible Simple mode macrocell configurations.


Figure 3 - Macrocell Configurations for Simple mode of the PEEL™ 16CV8 (see Figure 6 for Logic Array)

Complex Mode

In Complex mode, seven product terms feed the OR array which can generate a purely combinatorial function for the output pin. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. The output buffer is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all pins except 12 and 19. Figure 4 shows the possible complex mode macrocell configurations. Figure 7 shows the logic array of the PEEL™ 16CV8 configured in Complex mode.



Registered Mode

Registered mode provides eight product terms to the OR array for registered functions. The programmable output polarity selector provides active-high or active-low logic, eliminating the need for external inverters. (Note, however, that if register is selected, the PEEL™ 16CV8 registers power-up reset and so before the first clock arrives the output at the pin will be low if the user has selected active-high logic and high if the user has selected active-low logic. If combinatorial is selected, the output will be a function of the logic.) For registered functions, the output buffer enable is controlled directly from the /OE control pin. Feedback into the array comes from the macrocell register. In Registered mode, input pins 1 and 11 are permanently allocated as CLK and /OE, respectively. Figure 8 shows the logic array of the PEEL™ 16CV8 configured in Registered mode.

Figure 4 - Macrocell Configurations for the Complex Mode of the PEEL™ 16CV8 (see Figure 7 for Logic Array)

isters power-up reset and so before the first clock arrives the output at the pin will be low if the user has selected active-high logic and high if the user has selected active-low logic. If combinatorial is selected, the output will be a function of the logic.) For registered functions, the output buffer enable is controlled directly from the /OE control pin. Feedback into the array comes from the macrocell register. In Registered mode, input pins 1 and 11 are permanently allocated as CLK and /OE, respectively. Figure 8 shows the logic array of the PEEL™ 16CV8 configured in Registered mode.

Registered mode also provides the option of configuring a macrocell for combinatorial operation, with seven product terms feeding the OR function.

Again the programmable output polarity selector provides active-high or active-low logic. The output buffer enable is controlled by the eighth product term, allowing the macrocell to be configured for input, output, or bidirectional functions. Feedback into the array for input or bidirectional functions is available on all I/O pins. Macrocell Configurations for the Registered Mode of the PEEL™ 16CV8

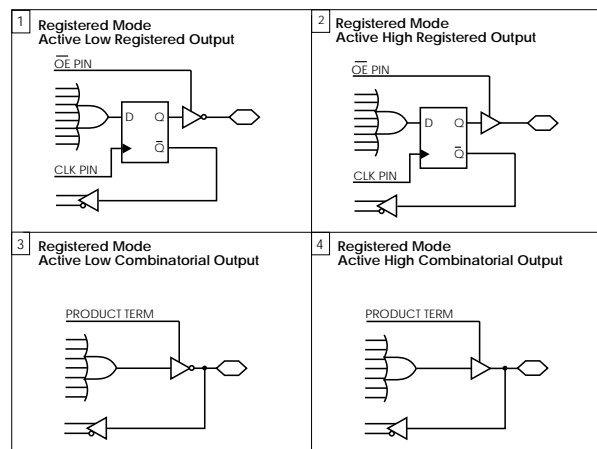


Figure 5 - Macrocell Configurations for the Registered Mode of the PEEL™ 16CV8 (see Figure 8 for Logic Array)

Design Security

The PEEL™ 16CV8 provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit has been set it is impossible to verify (read) or program the PEEL™ until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL™ 16CV8. The code cannot be read back after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

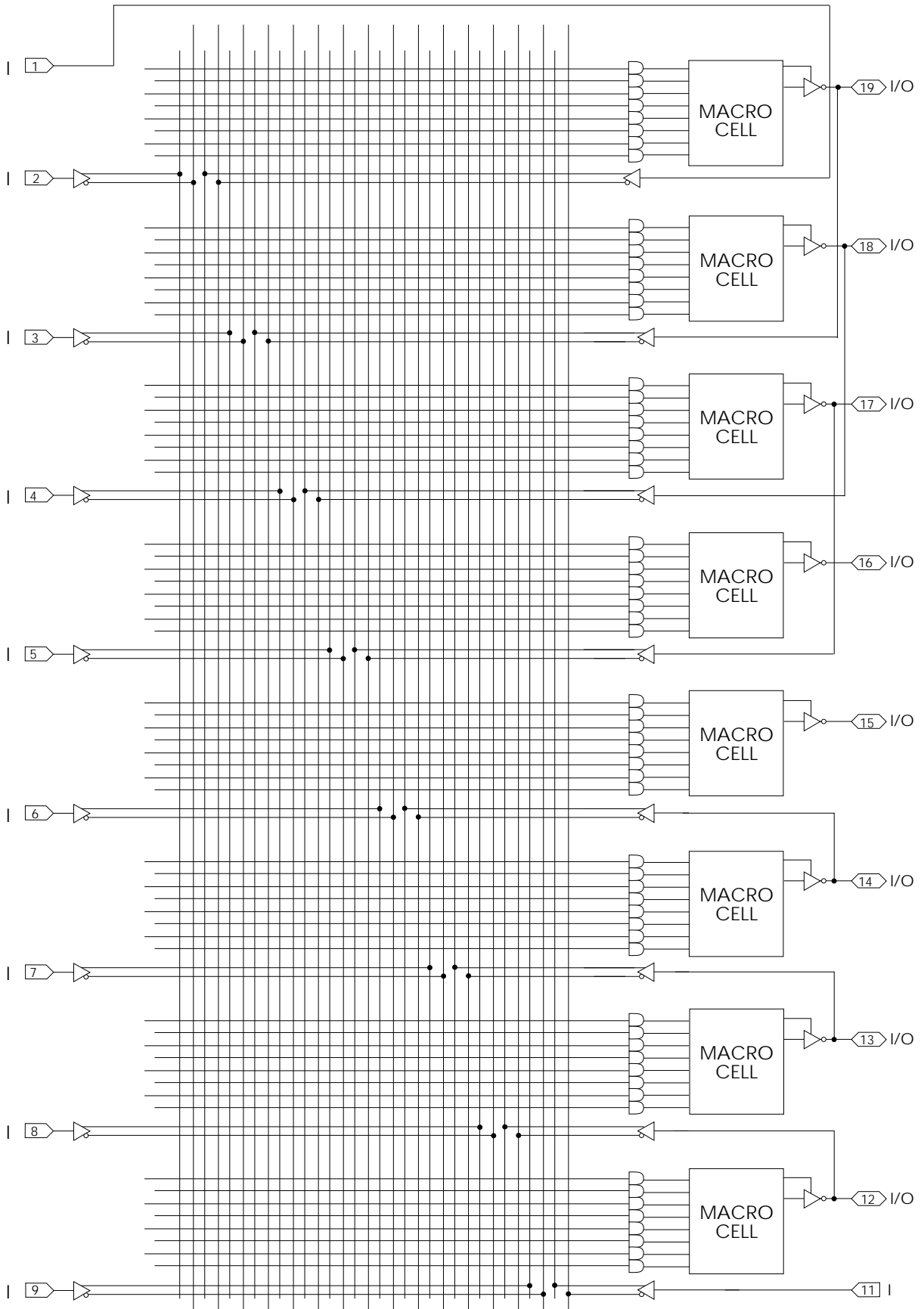


Figure 6 - PEEL™ 16CV8 Logic Array - Simple Mode (see Figure 3 for macrocell details)

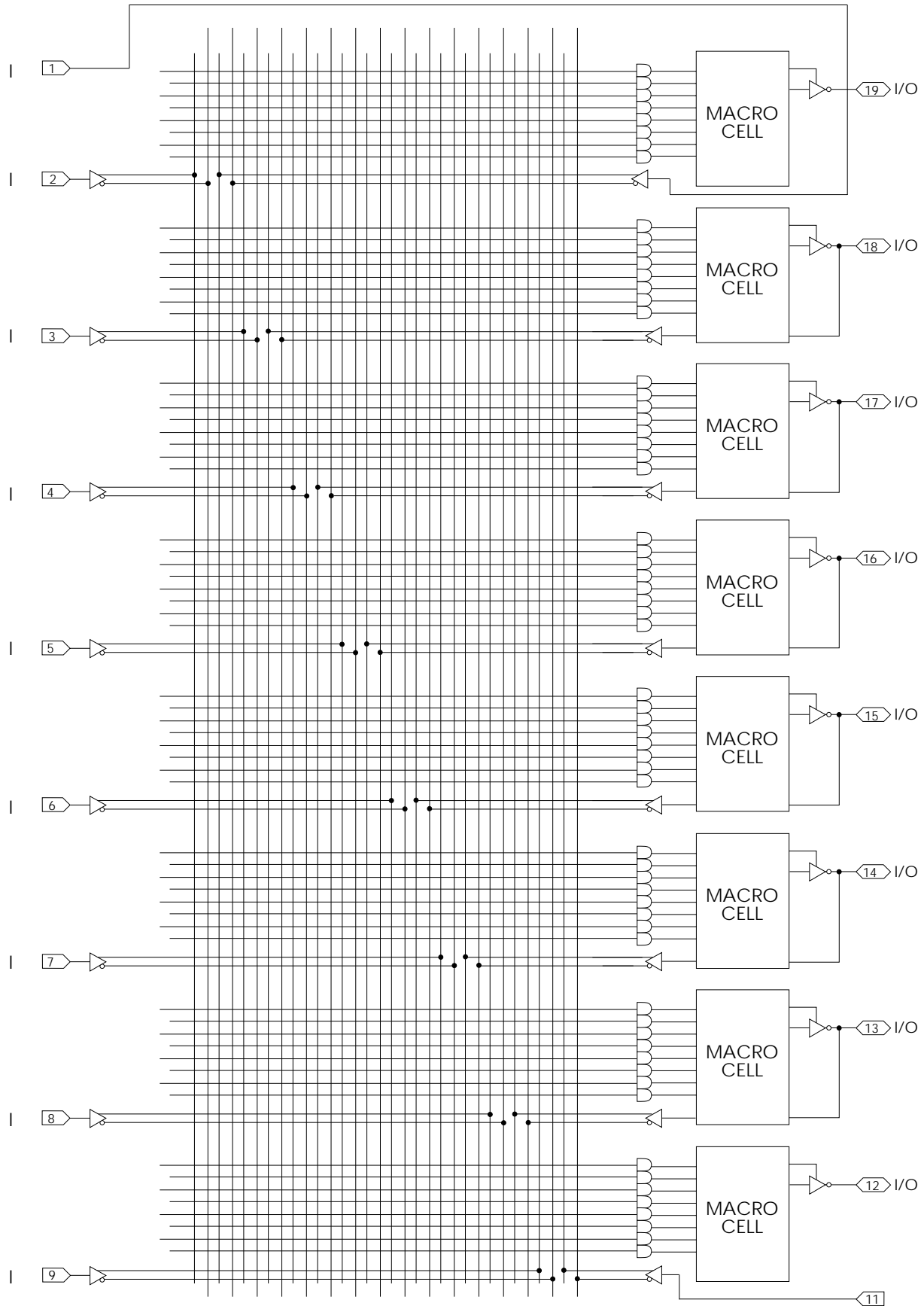


Figure 7 - PEEL™ 16CV8 Logic Array - Complex Mode (see Figure 4 for macrocell details)

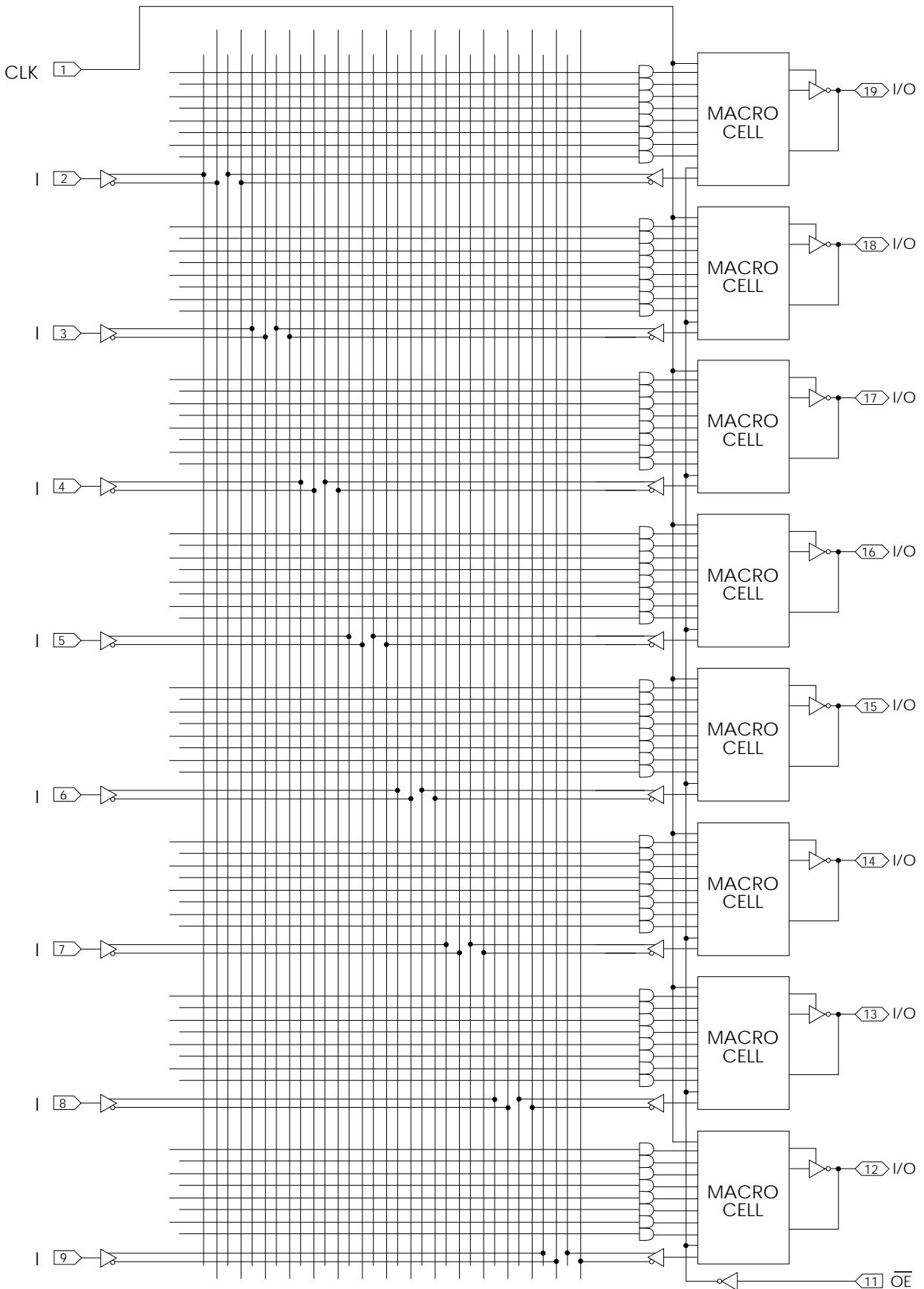


Figure 8 - PEEL™ 16CV8 Logic Array - Registered Mode (see Figure 5 for macrocell details)



This device has been designed and tested for the specified operating ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
VCC	Supply Voltage	Relative to Ground	-0.5 to + 6.0	V
VI, VO	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to VCC + 0.6	V
IO	Output Current	Per Pin (IOL, IOH)	±25	mA
TST	Storage Temperature		-65 to +150	°C
TLT	Lead Temperature	Soldering 10 Seconds	+300	°C

Operating Range

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage	Commercial	4.75	5.25	V
TA	Ambient Temperature	Commercial	0	+70	°C
TR	Clock Rise Time	See Note 3.		20	ns
TF	Clock Fall Time	See Note 3.		20	ns
TRVCC	VCC Rise Time	See Note 3.		250	ms

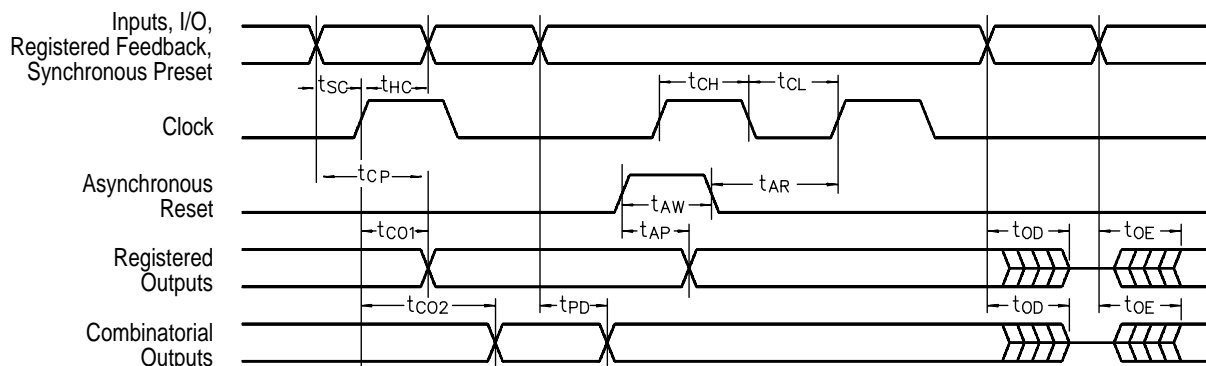
D.C. Electrical Characteristics Over the operating range (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
VOH	Output HIGH Voltage - TTL	VCC = Min, IOH = -4.0 mA	2.4		V
VOHC	Output HIGH Voltage - CMOS	VCC = Min, IOH = -10 µA	VCC - 0.3		V
VOL	Output LOW Voltage - TTL	VCC = Min, IOL = 16mA		0.5	V
VOLC	Output LOW Voltage - CMOS	VCC = Min, IOL = 10 µA		0.15	V
VIH	Input HIGH level		2.0	VCC + 0.3	V
VIL	Input LOW Voltage		-0.3	0.8	V
IIL	Input, I/O Leakage Current LOW	VCC = Max, VIN = GND, I/O = High Z		-10	µA
IIH	Input, I/O Leakage Current HIGH	VCC = Max, VIN = VCC, I/O = High Z	0 (Typical)	40	µA
ICC ¹⁰	VCC Current, f=1MHz	VIN = 0V or VCC, f = 25 MHz All Outputs disabled ⁴	-25	37	mA
CIN ⁷	Input Capacitance	TA = 25°C, VCC = 5.0V		6	pF
COU ⁷	Output Capacitance	@ f = 1 MHz		12	pF

A. C. Electrical Characteristics

Over the Operating Range 8, 11

Symbol	Parameter	-25		Unit
		Min	Max	
t _{PD}	Input ⁵ to non-registered output		25	ns
t _{OE}	Input ⁵ to output enable ⁶		25	ns
t _{OD}	Input ⁵ to output disable ⁶		25	ns
t _{CO1}	Clock to Output		15	ns
t _{CO2}	Clock to comb. output delay via internal registered feedback		35	ns
t _{CF}	Clock to Feedback		10	ns
t _{SC}	Input ⁵ or feedback setup to clock	20		ns
t _{HC}	Input ⁵ hold after clock	0		ns
t _{CL} , t _{CH}	Clock low time, clock high time ⁸	15		ns
t _{CP}	Min clock period Ext (t _{SC} + t _{CO1})	35		ns
f _{MAX1}	Internal feedback (1/t _{SC} +t _{CF}) ¹¹	28.5		MHz
f _{MAX2}	External Feedback (1/t _{CP}) ¹¹	28.5		MHz
f _{MAX3}	No Feedback (1/t _{CL} +t _{CH}) ¹¹	33.3		MHz
t _{AW}	Asynchronous Reset Pulse Width	25		ns
t _{AP}	Input ⁵ to Asynchronous Reset		25	ns
t _{AR}	Asynchronous Reset recovery time		25	ns
t _{RESET}	Power-on reset time for registers in clear state		5	μs

Switching Waveforms

Notes:

- Minimum DC input is -0.5V, however, inputs may undershoot to -2.0V for periods less than 20 ns.
- V_I and V_O are not specified for program/verify operation.
- Test Points for Clock and VCC in t_r and t_f are referenced at the 10% and 90% levels.
- I/O pins are 0V and VCC.
- "Input" refers to an input pin signal.
- t_{OE} is measured from input transition to VREF±0.1V, t_{OD} is measured from input transition to VOH-0.1V or VOL+0.1V; VREF=VL.
- Capacitances are tested on a sample basis.
- Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (Unless otherwise specified).
- Test one output at a time for a duration of less than 1 second.
- ICC for a typical application: This parameter is tested with the device programmed as an 8-bit Counter.
- Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design process modification that might affect operational frequency.



Ordering Information

Part Number	Speed	Temperature	Package
PEEL™ 16CV8P-25	25ns	C	P20
PEEL™ 16CV8J-25	25ns	C	J20
PEEL™ 16CV8S-25	25ns	C	S20
PEEL™ 16CV8T-25	25ns	C	T20

Part Number

