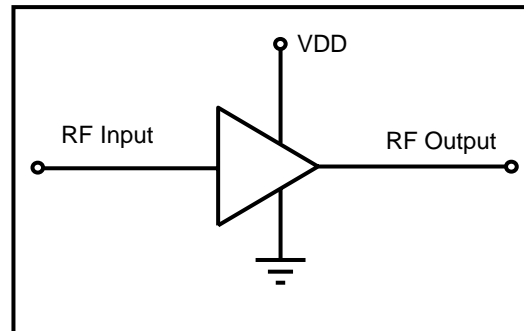


2-20 GHz BROADBAND MMIC AMPLIFIER
FEATURES:

- 15dB Gain
- Low Noise Amplifier
- Single Supply (Self Biased +5V @ 90mA)
- 12 dBm P_{1dB} Output Power at 20GHz
- pHEMT Technology
- Bias Control
- Input Return Loss < -12 dB
- Output Return Loss < -10 dB

GENERAL DESCRIPTION:

The FMA3058 is a high performance 2-20GHz Gallium Arsenide monolithic travelling wave amplifier. It is suitable for use in broadband communication, instrumentation and electronic warfare applications. The die is fabricated using the Filtronic 0.25 μ m process. The Circuit is DC blocked at both the RF input and the RF output.

FUNCTIONAL SCHEMATIC:

TYPICAL APPLICATIONS:

- Test Instrumentation
- Electronic Warfare
- Broadband Communication Infrastructure
- Fiber Optics

ELECTRICAL SPECIFICATIONS (SMALL-SIGNAL UNLESS OTHERWISE STATED):

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Small Signal Gain	2-20 GHz	-	15	-	dB
Gain Flatness	2-20 GHz	-	-	3	dB
Input Return Loss	2-20 GHz	-	-12	-	dB
Output Return Loss	2-20 GHz	-	-10	-	dB
Output Power at 1dB compression point	2 GHz, 5V drain bias	-	18	-	dBm
	10 GHz, 5V drain bias	-	18	-	dBm
	20 GHz, 5V drain bias	-	15	-	dBm
Drain Current	5V drain bias	-	90	-	mA
Noise Figure	2 GHz, 5V drain bias	-	3.5	-	dB
	10 GHz, 5V drain bias	-	3	-	dB
	20 GHz, 5V drain bias	-	6.5	-	dB

Note: $T_{AMBIENT} = +25^{\circ}C$, $Z_0 = 50\Omega$ Pads B and C open circuit

DIFFERENT BIAS CONFIGURATIONS:

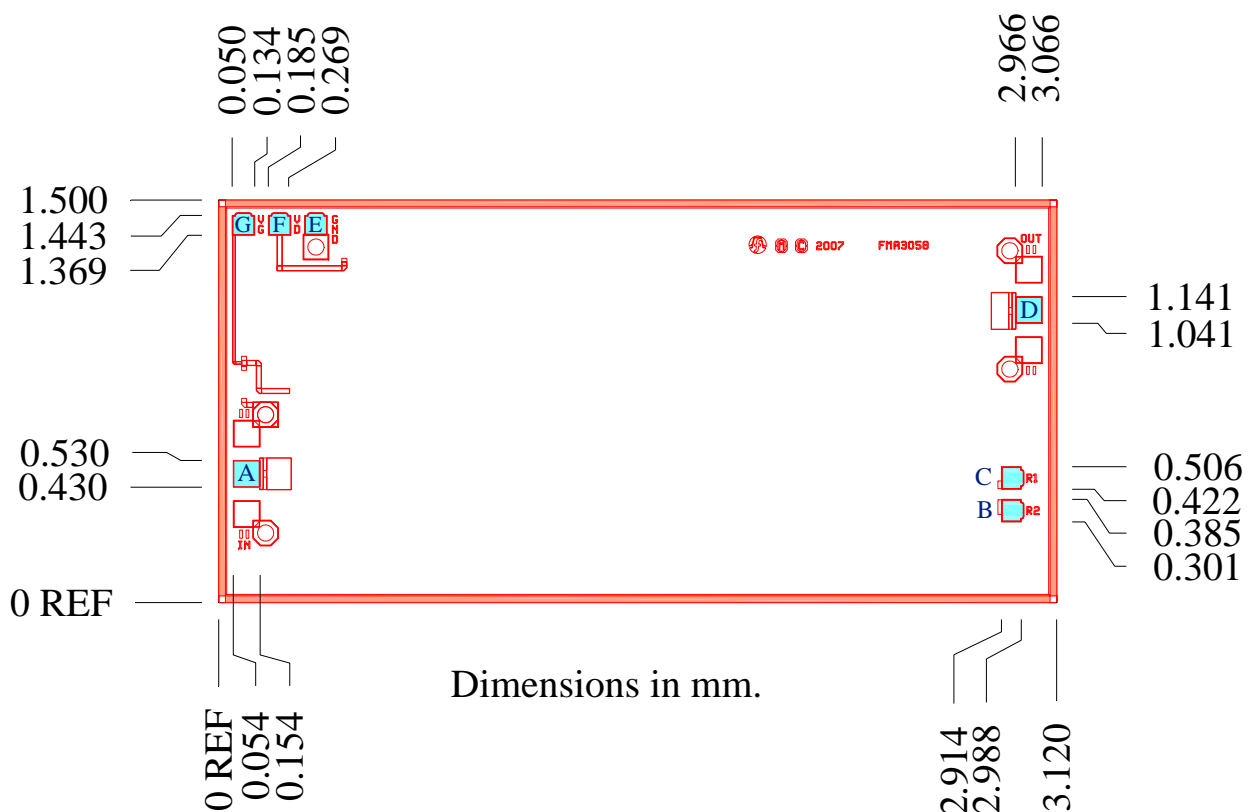
The device has a default current, set by an on chip resistor. Pads B and C can be bonded to ground to increase the device current by reducing the default resistance.

ABSOLUTE MAXIMUM RATINGS:

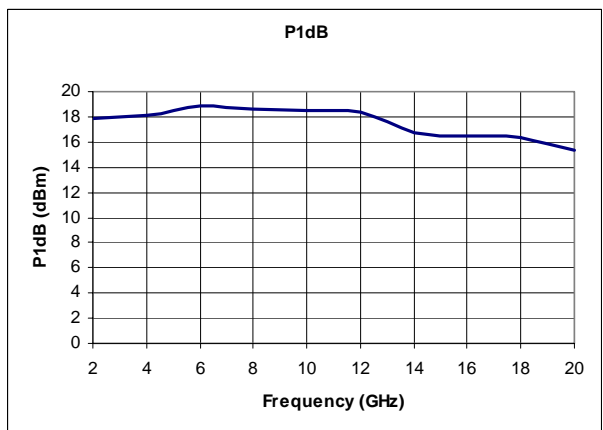
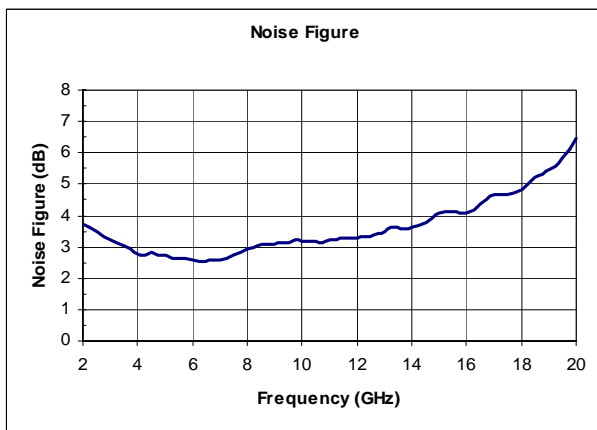
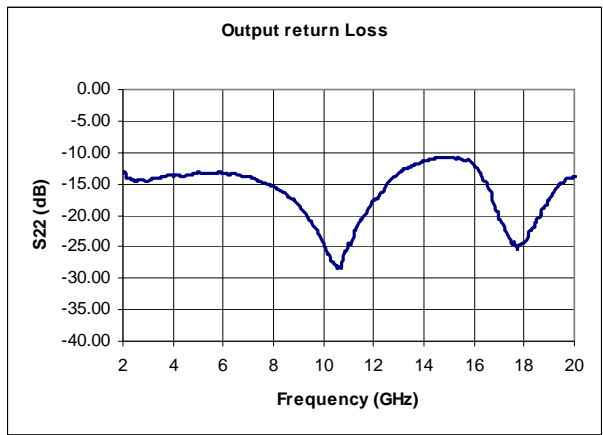
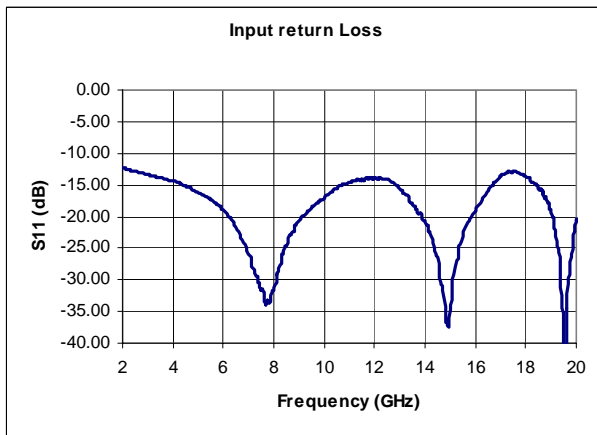
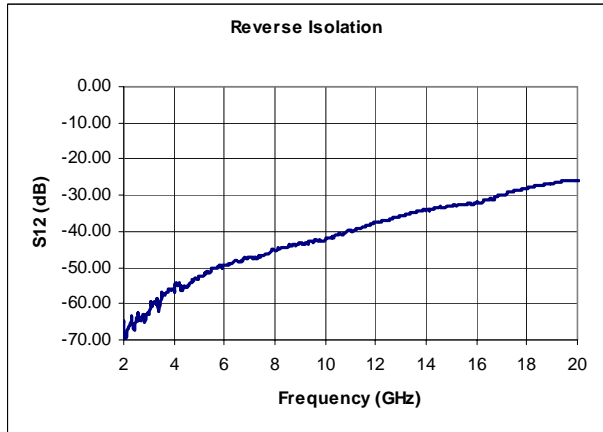
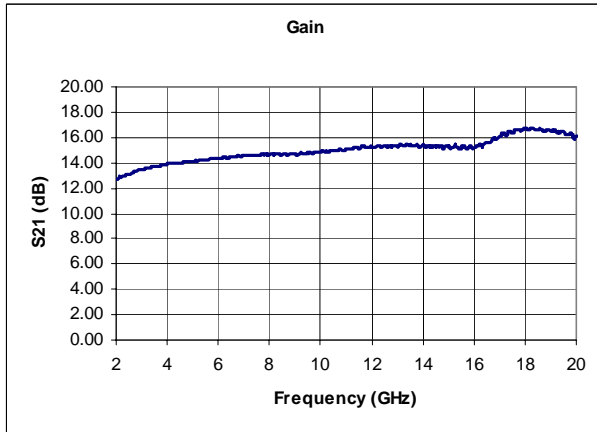
PARAMETER	SYMBOL	ABSOLUTE MAXIMUM
Max Input Power	Pin	+20dBm
Drain Voltage	VDD	+12V
Total Power Dissipation	Ptot	TBD
Thermal Resistivity	θ_{JC}	TBD
Operating Temp	Toper	-55°C to +85°C
Storage Temp	Tstor	-55°C to +150°C

PAD REF	PAD NAME	DESCRIPTION
A	IN	RF Input
B	R2	Internal Source Bias Resistor
C	R1	Internal Source Bias Resistor
D	OUT	RF Output
E	GND	Ground
F	VD	Drain voltage
G	VG	Optional Gate Voltage

Note: Exceeding any one of these absolute maximum ratings may cause permanent damage to the device.

PAD LAYOUT:


TYPICAL PERFORMANCE ON-WAFER:

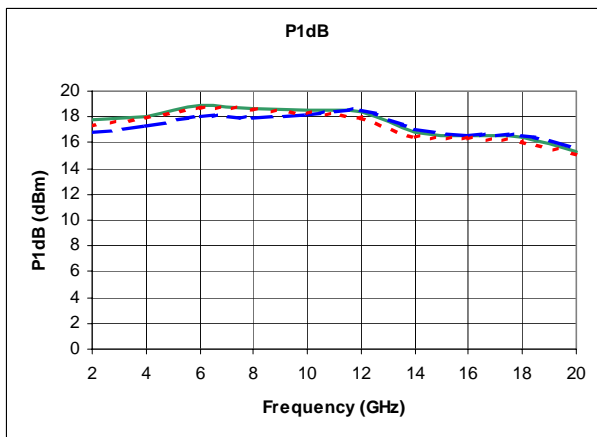
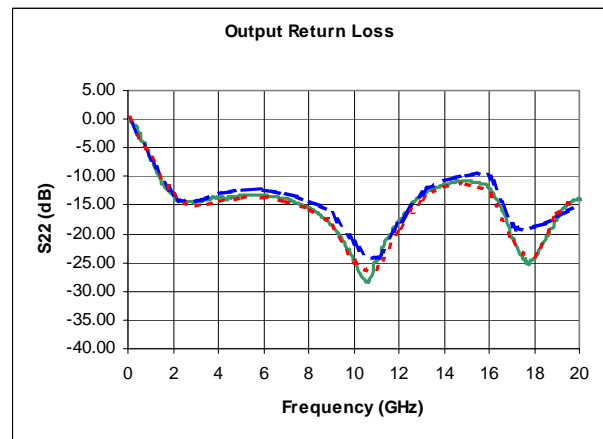
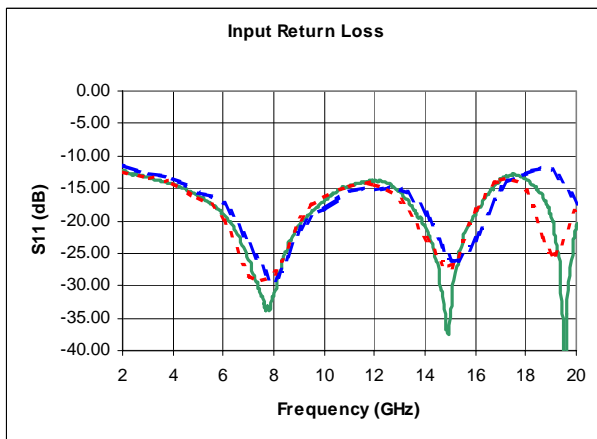
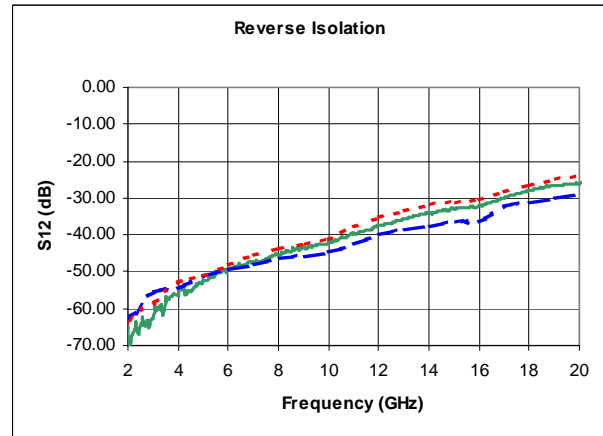
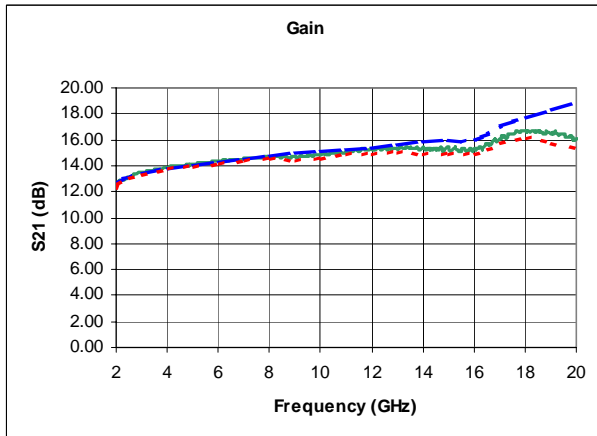
 Note: Measurement Conditions $I_D = 90\text{ mA}$, $V_{DD} = 5\text{ V}$, $T_{AMBIENT} = 25^\circ\text{C}$, Pads B and C open circuit.


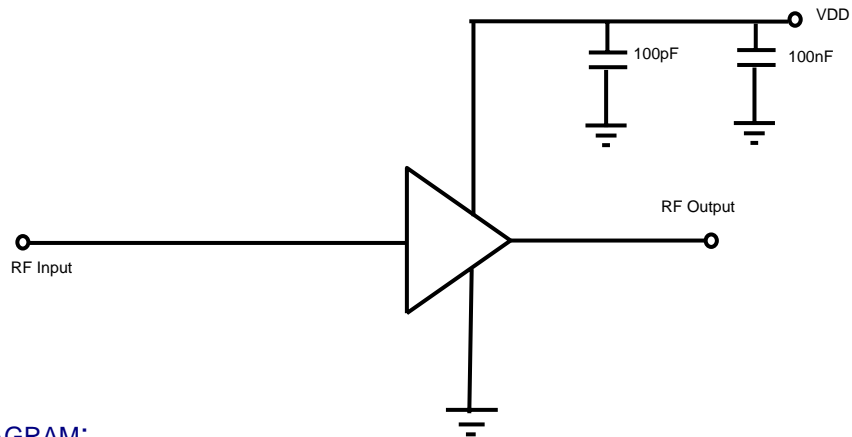
TYPICAL PERFORMANCE ON-WAFER OVER TEMPERATURE:

 Note: Measurement Conditions $I_D = 90 \text{ mA}$, $V_{DD} = 5 \text{ V}$, Pads B and C open circuit.

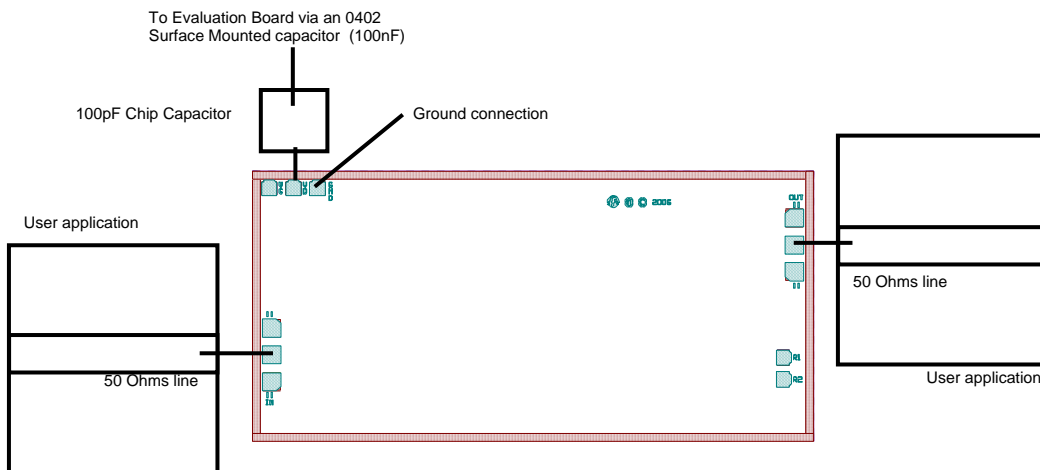
 — $T_{\text{AMBIENT}} = 25^\circ\text{C}$

 - - - $T_{\text{COLD}} = -55^\circ\text{C}$

 $T_{\text{HOT}} = +85^\circ\text{C}$


BIASING CIRCUIT SCHEMATIC:

ASSEMBLY DIAGRAM:

It is recommended that the RF connections be made using bond wires with 25 μ m diameter and a maximum length of 300 μ m. Ground connections should be made according to the required bias conditions.


BILL OF MATERIALS:

COMPONENT
All RF tracks should be 50 Ω characteristic material
Capacitor, 100pF, chip capacitor
Capacitor, 100nF, 0402

PREFERRED ASSEMBLY INSTRUCTIONS:

GaAs devices are fragile and should be handled with great care. Specially designed collets should be used where possible.

The recommended die attach is gold/tin eutectic solder under a nitrogen atmosphere. Stage temperature should be 280-290°C; maximum time at temperature is one minute. The recommended wire bond method is thermo-compression wedge bonding with 0.7 or 1.0 mil (0.018 or 0.025 mm) gold wire. Stage temperature should be 250-260°C.

Bonds should be made from the die first and then to the mounting substrate or package. The physical length of the bondwires should be minimised especially when making RF or ground connections.

ORDERING INFORMATION:

PART NUMBER	DESCRIPTION
FMA3058-000-WP	Die in Waffle-pack (Gel-pak available on request)

HANDLING PRECAUTIONS:


To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 0 (0-250 V) as defined in JEDEC Standard No. 22-A114. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

APPLICATION NOTES & DESIGN DATA:

Application Notes and design data including S-parameters are available on request.

DISCLAIMERS:

This product is not designed for use in any space based or life sustaining/supporting equipment.