STV7622

192 output plasma display panel data driver

Preliminary Data

Features

- 192 high-voltage outputs
- Output pad placements: I-shape
- 90 V absolute maximum supply
- EMI control features:
  - SmartSlope
  - ConstantSlope
  - Spread Spectrum Jitter (SSJ)
- Configurable data bus:
  - 3, 6 or 2 × 3 bits
  - TTL and LVCMOS compatible
  - RSDS mode
  - Single- or dual-edge clocking mode
  - 60 MHz clock frequency
- 3.3/5 V CMOS logic compatible
- - 60/+24 mA source/sink output current capability
- BCD Process
- Packaging according to customer request: wafer, die, bumped die/wafer, TCP or COF

Description

The STV7622 is a data driver for Plasma Display Panels (PDP) designed in the ST's proprietary BCD high-voltage technology.

It controls up to 192 outputs via an input data bus (3, 6 or 2 × 3-bits wide) operating at up to 60 MHz. This large number of outputs reduces the number of connections between the controller board and the data driver ICs.

The STV7622 contains a new logic input stage that minimizes EMI resulting from the transmission of high speed TTL or LVCMOS data and clock signals. This new input stage is RSDS compliant. It enables increasing the operating frequency without compromising noise immunity.

The input data bus is configured by dedicated input pins:

- BS1 and BS2: bus width select (3, 6, 2 × 3 bits or RSDS mode)
- DIR input: shift register loading direction

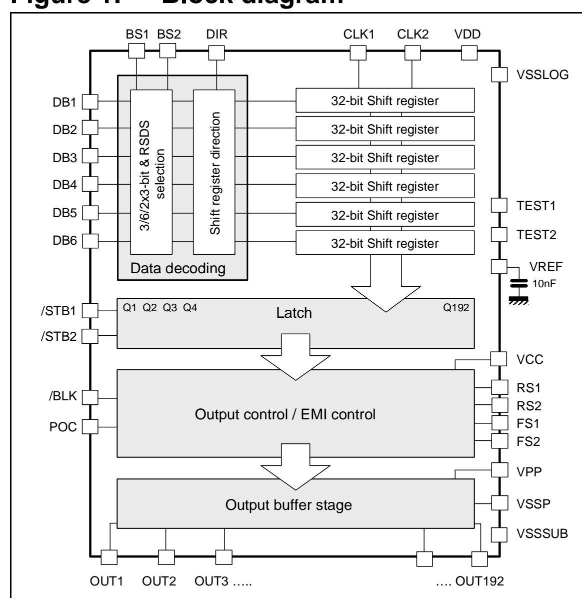
The STV7622 output stage integrates several ST patented functions aimed at reducing EMI without compromising addressing speed or performance of the PDP modules.

These functions mainly consist of:

- SmartSlope: controls the output falling edge speed /shape
- ConstantSlope: controls the output rising edge speed
- Spread Spectrum Jitter (SSJ): controls the spread of the output rising edge

The STV7622 is powered by a separate 70 V supply for the high-voltage outputs and a 5 V supply for the logic. All command input levels are 5 V CMOS as well as 3.3 V compatible.

Figure 1. Block diagram



This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Block diagram 3

2 Pin description 4

3 Output stage description 5

4 Pinout description 6

5 Circuit description 7

5.1 Data input block 7

5.2 3 x 64-bit data bus, standard transmission (BS1 = H, BS2 = L) 8

5.3 6 x 32-bit data bus, standard transmission (BS1 = L, BS2 = L) 8

5.4 2 x 3 x 32-bit data bus, standard transmission (BS1 = H, BS2 = H) 9

5.5 Differential transmission mode: RSDS (BS1 = L, BS2 = H) 10

5.6 Power output block and EMI control 12

6 Truth tables 14

7 Absolute maximum ratings 16

8 Electrical characteristics 17

9 AC timing requirements 19

10 AC timing characteristics 20

11 Pad dimensions and positions (in µm) 22

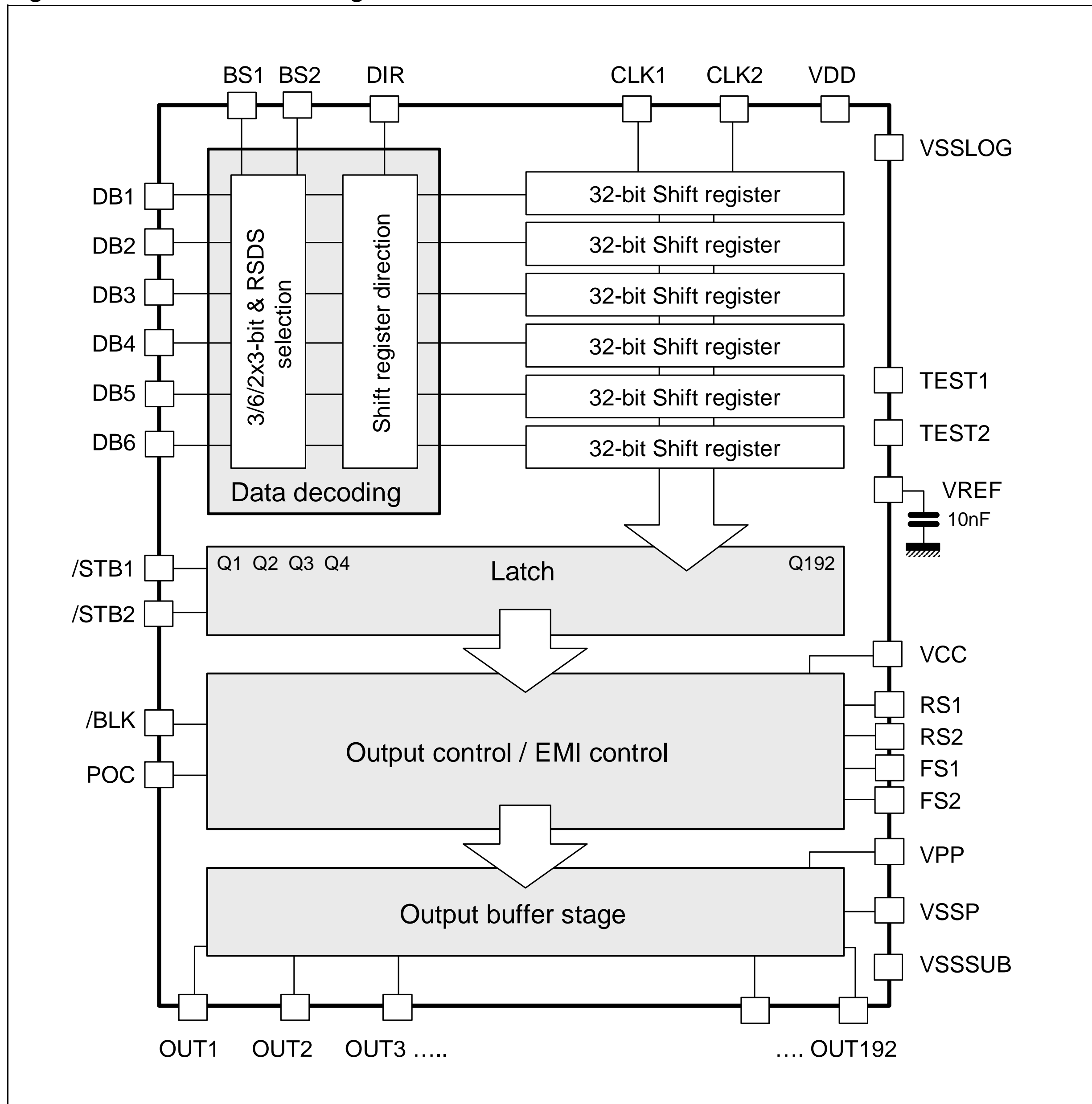
12 Tested wafer disclaimer 31

13 Ordering information 31

14 Revision history 31

1 Block diagram

Figure 2. STV7622 block diagram



2 Pin description

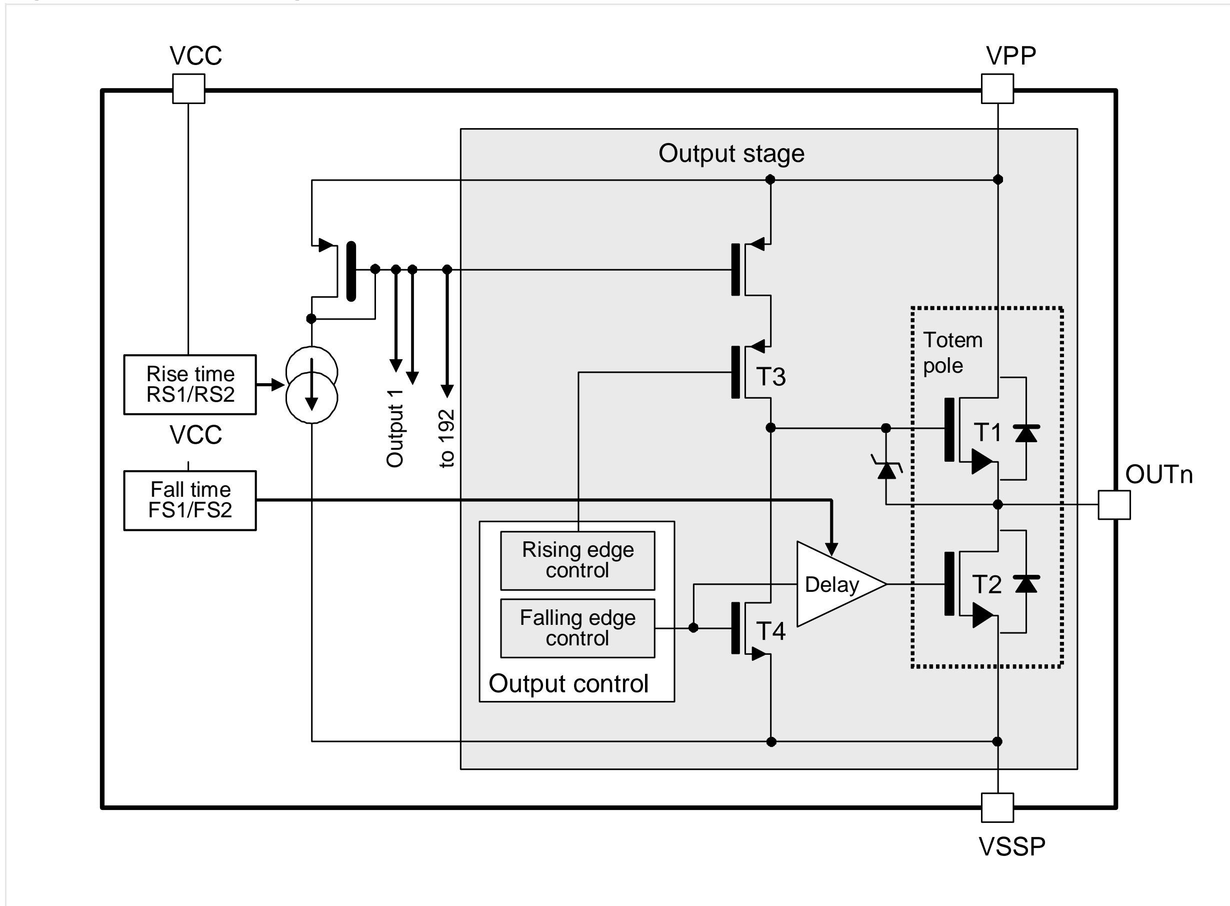
Table 1. Pin description

Pin name	Function	Description
VPP	Supply	DC high-voltage supply of power outputs
VCC	Supply	Analog 5V supply
VDD	Supply	Digital 5V supply
VSSP	Ground	Ground for power outputs
VSSSUB	Ground	Substrate ground
VSSLOG	Ground	Ground for 5V logic
OUT1 to OUT192	Outputs	Power outputs
DB1to DB6	Inputs	Shift register inputs
/BLK	Input	Blanking input
POC	Input	Power output control input
DIR	Input	Selection of shift register direction
BS1 and BS2	Inputs	Shift register configuration pins (3/6/2 × 3-bits and RSDS selection)
CLK1 and CLK2	Inputs	Clock for data shift register
/STB1 and /STB2	Inputs	Latch of data to power outputs
RS1 and RS2	Inputs	Output rise time selection pins
FS1 and FS2	Inputs	Output “slow-slope” fall time selection pins
TEST1	Test pin	Must be grounded
TEST2	Test pin	Must be grounded
VREF	Input	Filter for internal reference - must be connected to ground via a 10nF capacitor

Note: Inputs /BLK, /STB1 and /STB2 are active Low.

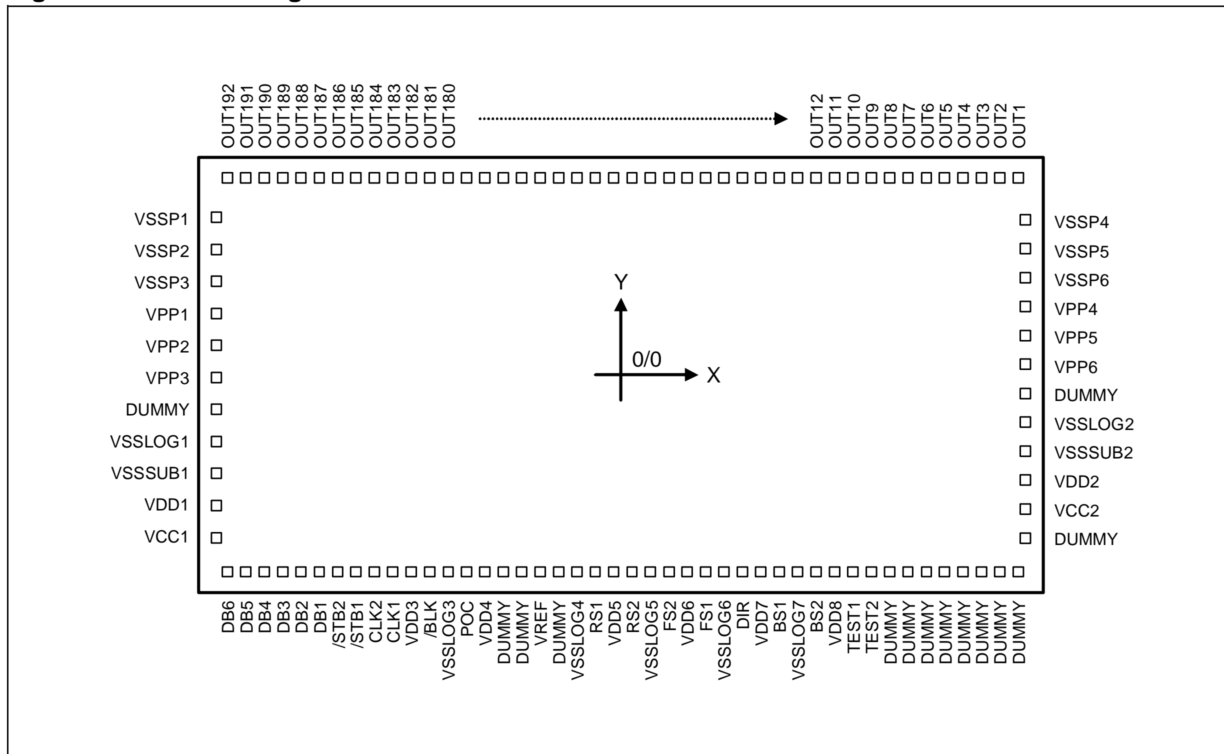
3 Output stage description

Figure 3. Output stage description



4 Pinout description

Figure 4. Pinout diagram



In the pinout diagram of *Figure 4* above:

- VDD1 to VDD8 are internally connected. It is not necessary to connect them together on the tape carrier package (TCP) - the same applies to VCC1 and VCC2.
- VSSLOG1 to VSSLOG2 are internally connected. It is not necessary to connect them together on the TCP - the same for VSSSUB1 and VSSSUB2.
- VSSLOG1 to VSSLOG7 are not internally connected to VSSSUB1 and VSSSUB2. We recommend shorting them together very close to the die, either on the TCP or at the TCP connector.
- VDD1 to VDD8 are not internally connected to VCC1 and VCC2. For good test coverage, they must not be shorted together on the TCP. In the application, VDD1 to VDD8, VCC1 and VCC2 must be connected together at the TCP connector level.
- TEST1 and TEST2 are used to test the device. For good test coverage, they must not be shorted together on the TCP. In the application, TEST1 and TEST2 must be grounded at the TCP connector level.
- VREF must be connected to ground via a 10 nF filter capacitor.

5 Circuit description

The STV7622 includes all the logic and power circuits necessary to drive the column electrodes of a Plasma Display Panel (PDP). A low-voltage logic block manages data information, and a high-voltage block converts the low-voltage information stored in the logic block into high-voltage signals applied to the display electrodes.

5.1 Data input block

The Data Bus is TTL- and LVCMOS-compatible and can also operate in an RSDS (Reduced Swing Differential Signaling) mode. The maximum clock frequency is 60 MHz.

The data input block consists of several shift registers operating in parallel to load the binary values of the digital video. The number of cells in each shift register is defined by the BS pin as described below in *Table 2*.

Table 2. BS1/BS2 truth table

BS1	BS2	Shift register configuration
L	L	6 × 32 bits
H	L	3 × 64 bits
L	H	RSDS mode
H	H	2 × 3 × 32 bits (96 + 96)

For the 3 × 64 bit configuration, only pins DB1, DB2 and DB3 of the input data bus are used, while for the 6 × 32 and 2 × 3 × 32 bit configurations all 6 bits of the input data bus input, pins DB1 to DB6, are used.

The DIR input pin is used to select the shift register loading direction.

Data is shifted for each low-to-high transition of the clock signal (CLK1). The maximum frequency of the clock is 60 MHz, which is equivalent to a 360 MHz serial shift register for a 6 × 32-bit arrangement.

When the /STB signal goes from high-to-low, data is transferred from the shift register to the latch and to the power output stages. All output data is stored and held in the latch stage when the latch input is pulled back High.

The core of the STV7622 is powered by 5 V. All logic inputs can be driven either by 5 V or 3.3 V CMOS logic.

The tables in the following sections describe the position of the first data sampled by the first rising edge of the CLK1 clock.

5.2 3 x 64-bit data bus, standard transmission (BS1 = H, BS2 = L)

The data bus is in 3-bit mode (DB1 to DB3 active) for BS1 = H and BS2 = L.

Data on DB1 is sampled by the first clock pulse and shifted from position 1 to position 190 after 64 clock pulses. The data is then applied to output 190, on the high-to-low transition of /STB.

Table 3. 3 x 64-bit data bus transmission

BS1	BS2	DIR	Input	Clock pulse number									Comment
				Position	01	02	03		...		62	63	64	
H	L	L	DB1 DB2 DB3	OUT OUT OUT	01 02 03	04 05 06	07 08 09				184 185 186	187 188 189	190 191 192	Left/Right shift
H	L	H	DB1 DB2 DB3	OUT OUT OUT	190 191 192	187 188 189	184 185 186				07 08 09	04 05 06	01 02 03	Right/Left shift

5.3 6 x 32-bit data bus, standard transmission (BS1 = L, BS2 = L)

The data bus is in 6-bit mode (DB1 to DB6 active) for BS1 = L and BS2 = L.

Table 4 below describes how data is shifted in the register.

Table 4. 6 x 32-bit data bus transmission

BS1	BS2	DIR	Input	Position	01	02	03		...		30	31	32	Comment
				Clock pulse number										
L	L	L	DB1 DB2 DB3 DB4 DB5 DB6	OUT OUT OUT OUT OUT OUT	01 02 03 04 05 06	07 08 09 10 11 12	13 14 15 16 17 18				175 176 177 178 179 180	181 182 183 184 185 186	187 188 189 190 191 192	Left/Right shift
L	L	H	DB1 DB2 DB3 DB4 DB5 DB6	OUT OUT OUT OUT OUT OUT	187 188 189 190 191 192	181 182 183 184 185 186	175 176 177 178 179 180				13 14 15 16 17 18	07 08 09 10 11 12	01 02 03 04 05 06	Right/Left shift

5.4 2 x 3 x 32-bit data bus, standard transmission (BS1 = H, BS2 = H)

The data bus is in 2 × 3-bit mode (DB1 to DB6 active) for BS1 = H and BS2 = H. *Table 5* below describes how data is shifted in the register.

Table 5. 2 x 3 x 32-bit data bus transmission

BS1	BS2	DIR	Input	Clock pulse number									Comment
				Position	01	02	03		...		30	31	32	
H	H	L	DB1	OUT	01	04	07				88	91	94	Left/Right shift
			DB2	OUT	02	05	08				89	92	95	
			DB3	OUT	03	06	09				90	93	96	
			DB4	OUT	97	100	103				184	187	190	
			DB5	OUT	98	101	104				185	188	191	
			DB6	OUT	99	102	105				186	189	192	
H	H	H	DB1	OUT	94	91	88				07	04	01	Right/Left shift
			DB2	OUT	95	92	89				08	05	02	
			DB3	OUT	96	93	90				09	06	03	
			DB4	OUT	190	187	184				103	100	97	
			DB5	OUT	191	188	185				104	101	98	
			DB6	OUT	192	189	186				105	102	99	

5.5 Differential transmission mode: RSDS (BS1 = L, BS2 = H)

In differential transmission mode, data is transmitted on two wires, one line transmits the data value, the other the inverted data. The logic level of the data is determined by the difference between data and inverted data. Two DB inputs are needed for the transmission of 1 data value. The sampling clocks, CLK1 and CLK2, as well as strobes STB1/ and STB2 are also transmitted differentially. Data is sampled on the rising and falling edges of the clock.

Table 6. 2 x 3 x 32-bit data bus transmission - differential mode

BS2	B12	DIR	Input	CLK1 clock pulse number									Comment
				Position	01↑	01↓	02↑		...		31↓	32↑	32↓	
H	L	L	DB1 DB2	OUT	01	04	07				184	187	190	Left/Right shift
			DB3 DB4		02	05	08				185	188	191	
			DB5 DB6		03	06	09				186	189	192	
H	L	H	DB1 DB2	OUT	190	187	184				07	04	01	Right/Left shift
			DB3 DB4		191	188	185				08	05	02	
			DB5 DB6		192	189	186				09	06	03	

In differential transmission operating mode, the biasing of the data input bus must be carefully arranged to reduce static power consumption. In stand-by and non-active modes, DB1, DB3, DB5, CLK1 and /STB1 should be set High to reduce bias current in the differential input buffers.

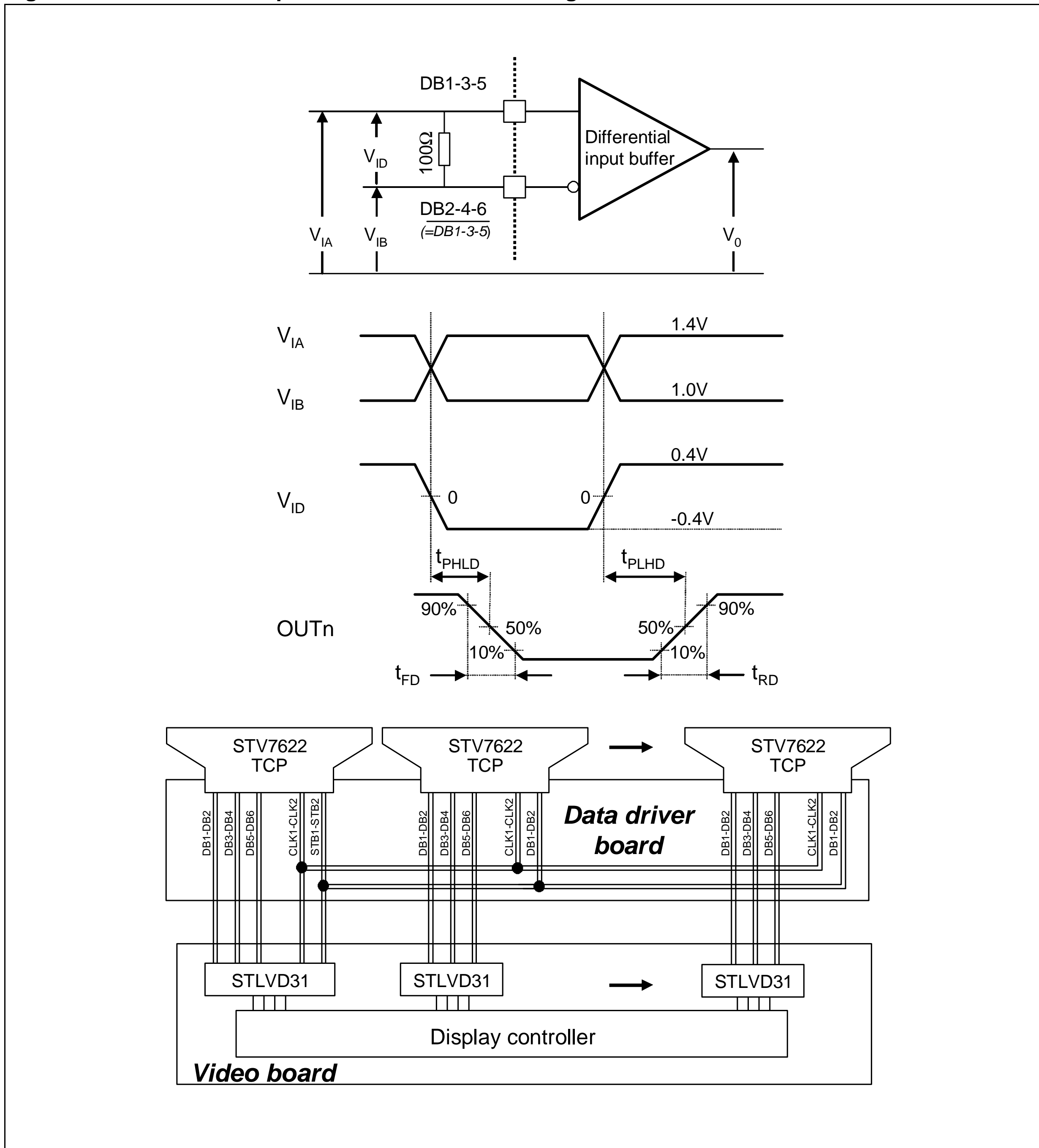
For a High level, all differential pairs should be configured with DB1, DB3, DB5, CLK1 and /STB1 High and with DB2, DB4, DB6, CLK2 and /STB2 Low.

When operating in differential transmission mode, a 100 ohm (1%) resistor termination must be connected between:

- DB1 and DB2
- DB3 and DB4
- DB5 and DB6
- CLK1 and CLK2
- STB1 and STB2

with each resistor placed as close as possible to the STV7622 itself.

Figure 5. Differential input buffer - waveform timing



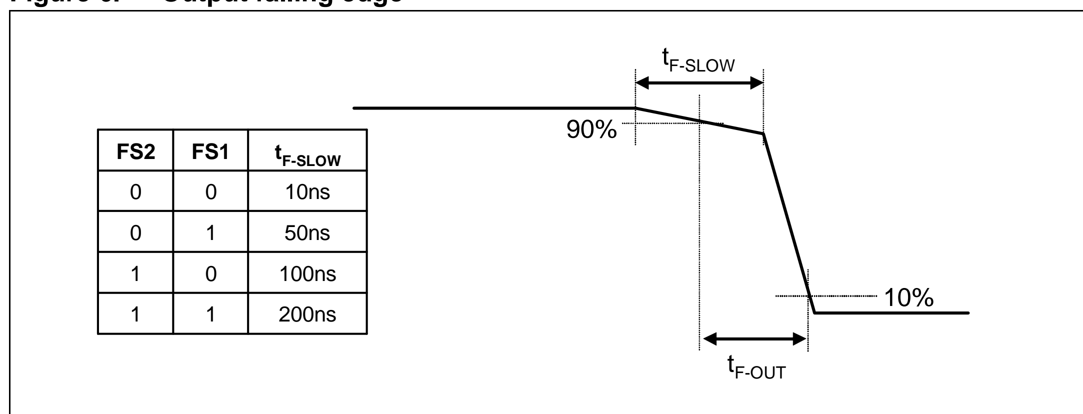
5.6 Power output block and EMI control

The high-voltage output stage has a totem pole structure (see *Figure 3*). The capacitive load is charged to Vpp by the high-side N-channel transistor, T1, and discharged to ground by the low-side N-channel transistor, T2. The status of the power outputs can also be controlled by the configuration pins, POC and /BLK, which can set the power outputs either all High or all Low.

Several functions, patented by STMicroelectronics, are implemented in the STV7622 to reduce EMI:

SmartSlope: The falling edge of the output pulse consist of 2 slopes (*Figure 6* below): a smooth slope followed by a steeper one (typically 4 times faster) The duration of the first slope is set by two logic inputs, FS1 and FS2, according to the table in *Figure 6*.

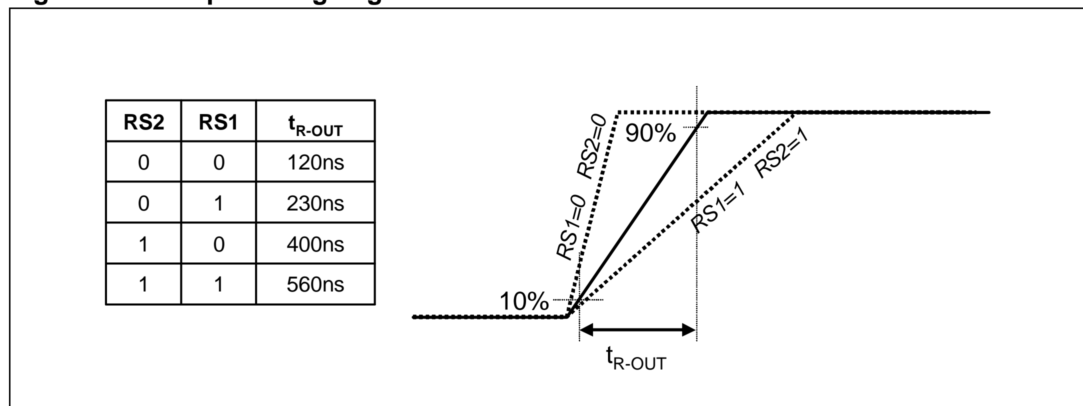
Figure 6. Output falling edge



FS2	FS1	$t_{F\text{-}SLOW}$
0	0	10ns
0	1	50ns
1	0	100ns
1	1	200ns

ConstantSlope: The duration of the output rising edge (*Figure 7*) is kept constant independent of the value of the capacitive load connected to the output. This solution minimizes the peak current in the power outputs as well as any oscillation phenomenon in the power supplies. In addition, it reduces high-frequency components of the EMI spectrum by suppressing very rapid rising edge transitions on the power outputs. The total duration of the rising edge ($t_{R\text{-}OUT}$) is set by another pair of logic inputs, RS1 and RS2, according to the table in *Figure 7* below.

Figure 7. Output rising edge



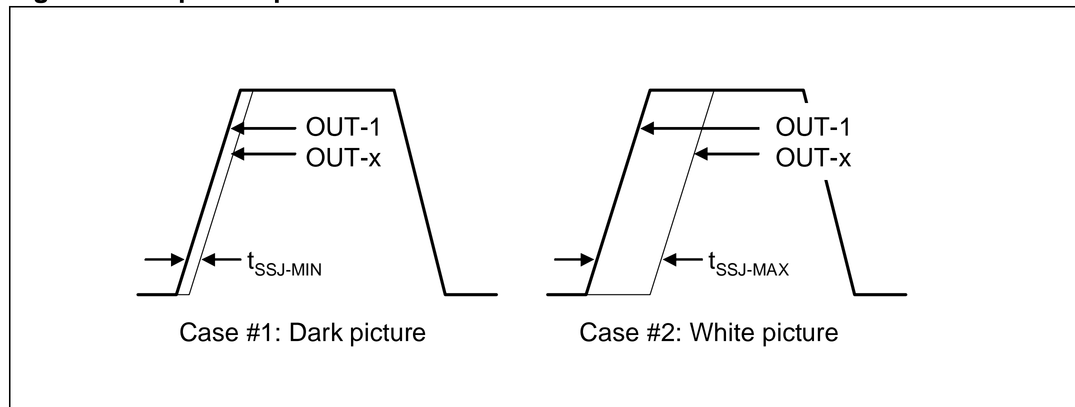
RS2	RS1	$t_{R\text{-}OUT}$
0	0	120ns
0	1	230ns
1	0	400ns
1	1	560ns

Spread Spectrum: To avoid having too large of a current in the driver during the rising edge of the power outputs, all outputs are not triggered at the same time.

Instead, the STV7622 inserts a small delay between the rising edge of two consecutive outputs. This delay depends on picture or image content (see *Figure 8*). For a dark picture, we have $t_{SSJ-MIN}$ = 1 to 2 ns (typ.) between output 1 and any output X, while for a white picture, we have $t_{SSJ-MAX}$ = 100 ns (typ.).

The SSJ function spreads the discharge current in the scan lines and, therefore, reduces EMI by “spreading” the energy spectrum.

Figure 8. Spread spectrum filter



6 Truth tables

Table 7. Shift register truth table

Input pins					Shift register function
BS2	BS1	DIR	CLK1	CLK2[1]	Q output
L	L	L	↑	N.C.	Left/Right shift DB1,2, ..6 input pins, 6 × 32-bit mode
L	L	L	H or L	N.C.	Steady
L	L	H	↑	N.C.	Right/Left shift DB1,2, ..6 input pins, 6 × 32-bit mode
L	L	H	H or L	N.C.	Steady
L	H	L	↑	N.C.	Left/Right shift DB1,2,3 input pins, 3 × 64-bit mode
L	H	L	H or L	N.C.	Steady
L	H	H	↑	N.C.	Right/Left shift DB1,2,3 input pins, 3 × 64-bit mode
L	H	H	H or L	N.C.	Steady
H	L	L	↑	↓	Left/Right shift DB1,2, ..6 input pins, RSDS mode
H	L	L	H or L	L or H	Steady
H	L	H	↑	↓	Right/Left shift DB1,2, ..6 input pins, RSDS mode
H	L	H	H or L	L or H	Steady
H	H	L	↑	N.C.	Left/Right shift, DB1,2, ...6 input pins, 2 × 3 × 32-bit mode
H	H	L	H or L	N.C.	Steady
H	H	H	↑	N.C.	Left/Right shift, DB1,2, ..6 input pins, 2 × 3 × 32-bit mode
H	H	H	H or L	N.C.	Steady

1. CLK2 is not used in LVCMOS operating mode and can be left “open” or “floating”.

Table 8. Truth table for power outputs

Q_n (1)	/STB1	/STB2 (2)	BS1	BS2	/BLK	POC	Driver output	Note	Comments
X	X	X	X	X	L	X	all L		Output at Low level
X	X	X	X	X	H	L	all H		Output at High level
X	H	X	L	L	H	H	Q_n	(3)	Data latched
X	H	L	L	H	H	H	Q_n	(4)	Data latched
X	H	X	H	L	H	H	Q_n	(5)	Data latched (RSDS)
X	H	X	H	H	H	H	Q_n	(6)	Data latched
L	L	X	L	L	H	H	L	(3)	Data copied
H	L	X	L	L	H	H	H	(3)	Data copied
L	L	H	L	H	H	H	L	(4)	Data copied (RSDS)
H	L	H	L	H	H	H	H	(4)	Data copied (RSDS)
L	L	X	H	L	H	H	L	(5)	Data copied
H	L	X	H	L	H	H	H	(5)	Data copied
L	L	X	H	H	H	H	L	(6)	Data copied
H	L	X	H	H	H	H	H	(6)	Data copied

1. Q_n is the state of the shift register output (*Figure 2*). “X” means either High or Low (H or L).
2. /STB2 is not used in LVCMOS operating mode and can be left “open” or “floating”.
3. Q_{n+1} = DB1, Q_{n+2} = DB2, Q_{n+3} = DB3, Q_{n+4} = DB4, Q_{n+5} = DB5, Q_{n+6} = DB6; n = {0, 6, 12, 18, …186}.
4. RSDS mode: Q_{n+1} = DB1, Q_{n+1} = DB2, Q_{n+2} = DB3, Q_{n+2} = DB4, Q_{n+3} = DB5, Q_{n+3} = DB6; n = {0, 6, 12, 18, …186}.
5. Q_{n+1} = DB1, Q_{n+2} = DB2, Q_{n+3} = DB3; n = {0, 3, 6, 9, …186, 189}.
6. Q_{n+1} = DB1, Q_{n+2} = DB2, Q_{n+3} = DB3, Q_{n+97} = DB4, Q_{n+98} = DB5, Q_{n+99} = DB6; n = {0, 3, 6, 9, …186, 189}.

7 Absolute maximum ratings

Table 9. Absolute maximum ratings

Symbol	Parameter	Value	Units
Vdd	Digital supply range	-0.3, +7	V
Vcc	Analog supply range	-0.3, +7	V
Vpp	Driver supply range	-0.3, +90	V
Vin	Logic input voltage range	-0.3, Vcc+0.3	V
Ipout	Driver output current x[(1), (2), (3)]	- 70/+35	mA
Idout	Diode output current[(1), (2), (3)]	-200/+300	mA
Vout	Output power voltage range	-0.3, +90	V
V_{ESD}	ESD susceptibility, Human Body Model (100pF discharged through 1.5Kohms), on all except the VCC pins[(4)]	2	KV
Tjmax	Maximum junction temperature	100	°C
Tstg	Storage temperature range	-50, +150	°C

1. Measurements done on one single output, x. The other outputs are either not used or are connected to output x. Assumes junction temperature remains less than Tjmax during measurement.
2. All transient current measurements are made under conditions close to those encountered in a typical application (that is, with duration of any output current spike always less than 300 ns).
3. These parameters are measured during STMicroelectronics' internal qualification which includes temperature characterization on standard as well as corner batches of the process. These parameters are not tested in production.
4. VCC pins withstand 1.3 KV.

8 Electrical characteristics

VCC = VDD = 5V, VPP = 70V, VSSP = VSSLOG = VSSSUB = 0V, T_{AMB} = 25°C, f_{CLK} = 50 MHz, unless otherwise specified.

Table 10. Electrical characteristics

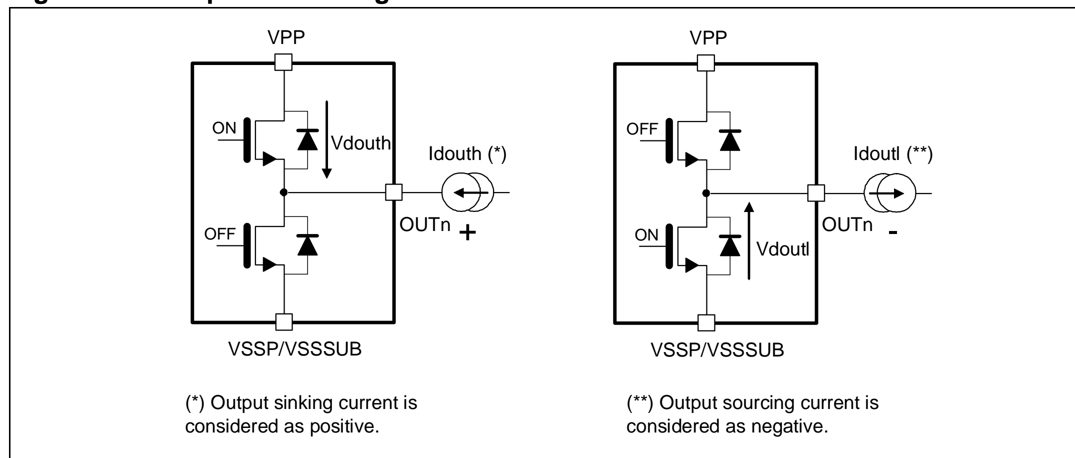
Symbol	Parameter	Min.	Typ.	Max.	Units
Supply					
Vdd	Digital supply voltage	4.50	5	5.5	V
Idd	Digital supply current (1)	-		10	µA
Iddl	Digital Dynamic Supply Current (CLK1 freq = 20MHz) (2)	-	15	20	mA
Idd	Digital Supply Current @ V_{IH} = 2.0V	250	500	900	µA
Vcc	Analog supply voltage	4.50	5	5.5	V
Icc_1	Analog supply current in standard transmission mode	-	1.1	2	mA
Icc_2	Analog supply current in RSDS mode (that is, with BS1 = BS2 = L) and with DB1, DB3, DB5, CLK1 and /STB1 less than DB2, DB4, DB6, CLK2 and /STB2, respectively	-	5	10	mA
Vpp	DC power output supply voltage	15		80	V
Ipph-1	Power output supply current (steady outputs) @ VCC = 0V	-	-	20	µA
Ipph-2	Power output supply current (steady outputs) @ VCC = 5V and RS1 = RS2 = L	300	450	600	µA
OUT1 to OUT192					
Vpouth	Power output high level (voltage drop versus Vpp) @ Ipouth = -20mA and Vpp = 70V	2	3.5	5	V
Vpoutl	Power output low level @ Ipoutl = +20mA	3	6	10	V
Vdouth	Output upper diode voltage drop @ Idouth = +30mA (see *Figure 9*)	-	1	2	V
Vdoutl	Output lower diode voltage drop @ Idoutl = -30mA (see *Figure 9*)	-2	-1	-	V
Standard Mode, TTL/LVCMOS inputs: CLK1, DIR, /STB1, POC, /BLK, BS1, BS2 and DB1 to DB6					
V_{IH}	High level input voltage	2.0	-	-	V
V_{IL}	Low level input voltage	-	-	0.8	V
I_{IH}	High level input current ($V_{IH} \geq$ 2.0V)	-	-	5	µA
I_{IL}	Low level input current (V_{IL} = 0V)	-	-	5	µA

Table 10. Electrical characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Units
RSDS Mode, inputs: CLK1, CLK2, /STB1, /STB2 and DB1 to DB6					
$\|V_{id}\|$	Magnitude of differential input voltage	100	400	600	mV
V_{ic}	Common mode input range	$0.5\|V_{id}\|$	1.2	$2.4 - 0.5\|V_{id}\|$	V
Cin	Input capacitance (3)	-	-	15	pF

1. For 5V CMOS input logic levels (0 or 5V)
2. All input data is switched at 10MHz rate.
3. Same for TTL and RSDS modes. This parameter is measured during qualification by ST Microelectronics which includes temperature characterization on standard as well as corner batches of the process. This parameter is not tested in production.

Figure 9. Output test configuration



9 AC timing requirements

VCC = VDD = 4.5 V to 5.5 V, Tamb = -20 °C to +85 °C,
input signal edge maximum rise and fall times (tr, tf) = 3 ns.

Table 11. AC timing requirements

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CLK}	Data clock period	16.7	-	-	ns
t_{WHCLK}	Duration of clock pulse at high level	8.8	-	-	ns
t_{WLCLK}	Duration of clock pulse at low level	8.8	-	-	ns
t_{SDAT}	Input data set-up time before low-to-high clock transition	5	-	-	ns
t_{HDAT}	Input data hold-time after low-to-high clock transition	5	-	-	ns
t_{HSTB}	Strobe hold-time after low-to-high clock transition	5	-	-	ns
t_{STB}	Duration of strobe Low level	10	-	-	ns
t_{SSTB}	Strobe set-up time before low-to-high clock transition	5			ns

10 AC timing characteristics

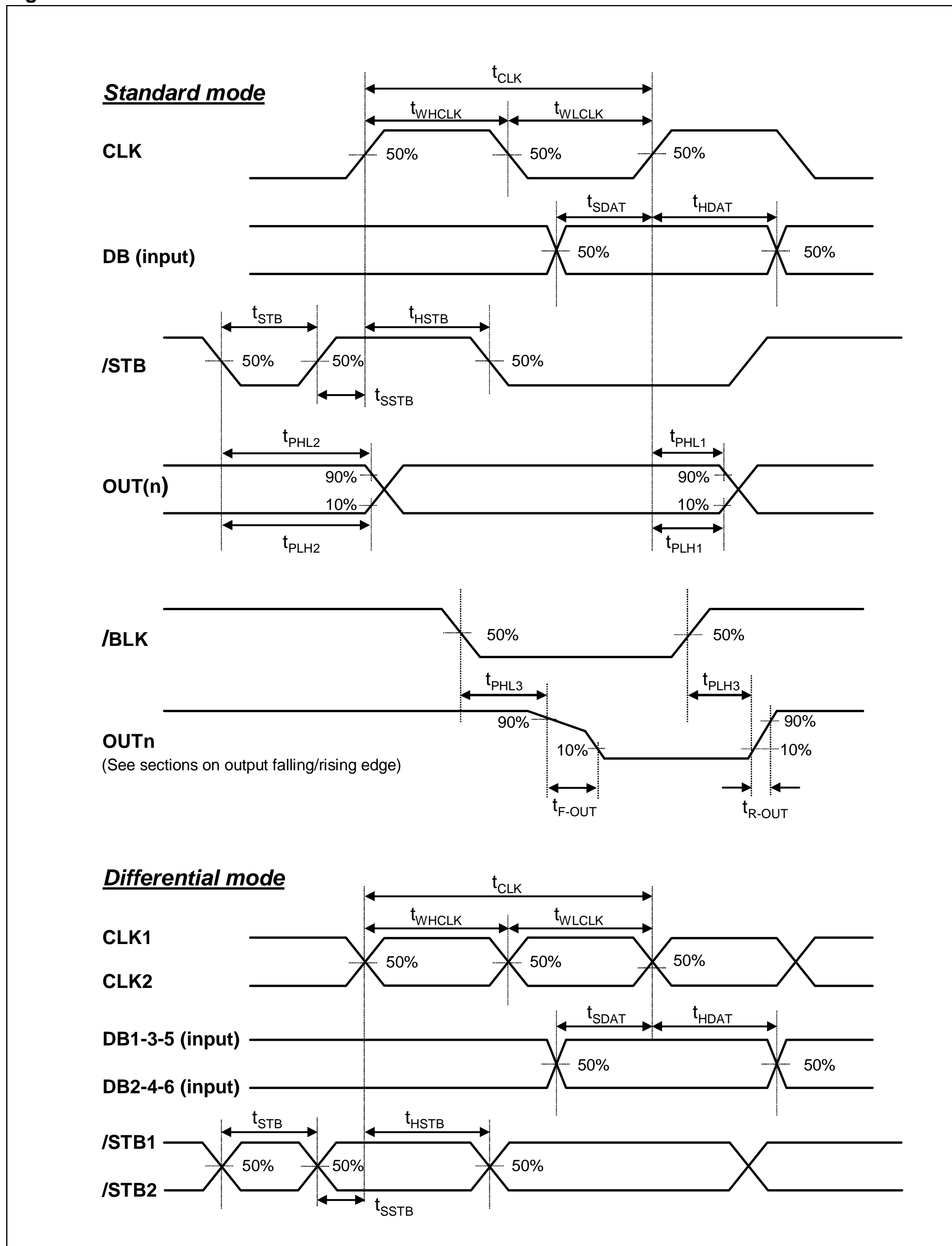
VCC = VDD = 5V, VPP = 70V, VSSP = VSSLOG = VSSSUB = 0V, Tamb = 25°C,
Fclk= 60MHz, $V_{ILmax} = 0.2 \times$ VCC, $V_{IHmin} = 0.8 \times$ VCC.

Table 12. AC timing characteristics

Symbol	Parameter	Min	Typ	Max	Units
t_{PHL1} t_{PLH1}	Delay of power output change after CLK1/CLK2 transition - high to low - low to high	- -	35 30	100 100	ns ns
t_{PHL2} t_{PLH2}	Delay of power output change after /STB1/STB2 transition - high to low - low to high	 -	- -	95 95	ns ns
t_{PHL3} t_{PLH3}	Delay of power output change after /BLK transition - high to low - low to high	- -	25 20	90 90	ns ns
$t_{R\text{-}OUT}$	Power output rise time[1] (RS = “L” and RS2 = “L”)	90	120	150	ns
$t_{R\text{-}OUT}$	Power output rise time[1] (RS = “H” and RS2 = “L”)	180	230	280	ns
$t_{R\text{-}OUT}$	Power output rise time[1] (RS= “L” and RS2 = “H”)	320	400	480	ns
$t_{R\text{-}OUT}$	Power output rise time[1] (RS = “H” and RS2 = “H”)	470	560	670	ns
$t_{F\text{-}OUT}$	Power output fall time[2]	50	-	200	ns
$t_{F\text{-}SLOW}$	Soft slope duration[3] (FS1 = “L” and FS2 = “L”)	8	10	12	ns
$t_{F\text{-}SLOW}$	Soft slope duration[3] (FS1 = “H” and FS2 = “L”)	40	50	60	ns
$t_{F\text{-}SLOW}$	Soft slope duration[3] (FS1 = “L” and FS2 = “H”)	80	100	120	ns
$t_{F\text{-}SLOW}$	Soft slope duration[3] (FS1 = “H” and FS2 = “H”)	160	200	240	ns

1. $t_{R\text{-}OUT}$ is set externally by inputs RS1 and RS2.
2. Measurement made on one of the 192 power outputs with FS1 = “H” and FS2 = “L”. Load capacitor CL = 50pF, all other power outputs Low.
3. $t_{F\text{-}SLOW}$ is set externally by inputs FS1 and FS2.

Figure 10. AC characteristic waveforms



11 Pad dimensions and positions (in µm)

The reference (x=0, y=0) is the centre of the die. Output pad pitch is 76.5µm.

Pad placement coordinate values correspond to the center of each bump pad center. Pad size is specified for bumping.

Table 13. Pad placement and bump pad dimensions (in microns)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
TOP SIDE from left to right				
OUT192	-7303.1	624.2	43.5	65.6
OUT191	-7226.6	624.2	43.5	65.6
OUT190	-7150.1	624.2	43.5	65.6
OUT189	-7073.6	624.2	43.5	65.6
OUT188	-6997.1	624.2	43.5	65.6
OUT187	-6920.6	624.2	43.5	65.6
OUT186	-6844.1	624.2	43.5	65.6
OUT185	-6767.6	624.2	43.5	65.6
OUT184	-6691.1	624.2	43.5	65.6
OUT183	-6614.6	624.2	43.5	65.6
OUT182	-6538.1	624.2	43.5	65.6
OUT181	-6461.6	624.2	43.5	65.6
OUT180	-6385.1	624.2	43.5	65.6
OUT179	-6308.6	624.2	43.5	65.6
OUT178	-6232.1	624.2	43.5	65.6
OUT177	-6155.6	624.2	43.5	65.6
OUT176	-6079.1	624.2	43.5	65.6
OUT175	-6002.6	624.2	43.5	65.6
OUT174	-5926.1	624.2	43.5	65.6
OUT173	-5849.6	624.2	43.5	65.6
OUT172	-5773.1	624.2	43.5	65.6
OUT171	-5696.6	624.2	43.5	65.6
OUT170	-5620.1	624.2	43.5	65.6
OUT169	-5543.6	624.2	43.5	65.6
OUT168	-5467.1	624.2	43.5	65.6
OUT167	-5390.6	624.2	43.5	65.6
OUT166	-5314.1	624.2	43.5	65.6

Table 13. Pad placement and bump pad dimensions (in microns) (continued)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
OUT165	-5237.6	624.2	43.5	65.6
OUT164	-5161.1	624.2	43.5	65.6
OUT163	-5084.6	624.21	43.5	65.6
OUT162	-5008.1	624.2	43.5	65.6
OUT161	-4931.6	624.2	43.5	65.6
OUT160	-4855.1	624.2	43.5	65.6
OUT159	-4778.6	624.2	43.5	65.6
OUT158	-4702.1	624.2	43.5	65.6
OUT157	-4625.6	624.2	43.5	65.6
OUT156	-4549.1	624.2	43.5	65.6
OUT155	-4472.6	624.2	43.5	65.6
OUT154	-4396.1	624.2	43.5	65.6
OUT153	-4319.6	624.2	43.5	65.6
OUT152	-4243.1	624.2	43.5	65.6
OUT151	-4166.6	624.2	43.5	65.6
OUT150	-4090.1	624.2	43.5	65.6
OUT149	-4013.6	624.2	43.5	65.6
OUT148	-3937.1	624.2	43.5	65.6
OUT147	-3860.6	624.2	43.5	65.6
OUT146	-3784.1	624.2	43.5	65.6
OUT145	-3707.6	624.2	43.5	65.6
OUT144	-3631.1	624.2	43.5	65.6
OUT143	-3554.6	624.2	43.5	65.6
OUT142	-3478.1	624.2	43.5	65.6
OUT141	-3401.6	624.2	43.5	65.6
OUT140	-3325.1	624.2	43.5	65.6
OUT139	-3248.6	624.2	43.5	65.6
OUT138	-3172.1	624.2	43.5	65.6
OUT137	-3095.6	624.2	43.5	65.6
OUT136	-3019.1	624.2	43.5	65.6
OUT135	-2942.6	624.2	43.5	65.6
OUT134	-2866.1	624.2	43.5	65.6
OUT133	-2789.6	624.2	43.5	65.6

Table 13. Pad placement and bump pad dimensions (in microns) (continued)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
OUT132	-2713.1	624.2	43.5	65.6
OUT131	-2636.6	624.2	43.5	65.6
OUT130	-2560.1	624.2	43.5	65.6
OUT129	-2483.6	624.2	43.5	65.6
OUT128	-2407.1	624.2	43.5	65.6
OUT127	-2330.6	624.2	43.5	65.6
OUT126	-2254.1	624.215	43.5	65.6
OUT125	-2177.6	624.2	43.5	65.6
OUT124	-2101.1	624.2	43.5	65.6
OUT123	-2024.6	624.2	43.5	65.6
OUT122	-1948.1	624.2	43.5	65.6
OUT121	-1871.6	624.2	43.5	65.6
OUT120	-1795.1	624.2	43.5	65.6
OUT119	-1718.6	624.2	43.5	65.6
OUT118	-1642.1	624.2	43.5	65.6
OUT117	-1565.6	624.2	43.5	65.6
OUT116	-1489.1	624.2	43.5	65.6
OUT115	-1412.6	624.2	43.5	65.6
OUT114	-1336.1	624.2	43.5	65.6
OUT113	-1259.6	624.2	43.5	65.6
OUT112	-1183.1	624.2	43.5	65.6
OUT111	-1106.6	624.2	43.5	65.6
OUT110	-1030.1	624.2	43.5	65.6
OUT109	-953.6	624.2	43.5	65.6
OUT108	-877.1	624.2	43.5	65.6
OUT107	-800.6	624.2	43.5	65.6
OUT106	-724.1	624.2	43.5	65.6
OUT105	-647.6	624.2	43.5	65.6
OUT104	-571.1	624.2	43.5	65.6
OUT103	-494.6	624.2	43.5	65.6
OUT102	-418.1	624.2	43.5	65.6
OUT101	-341.6	624.2	43.5	65.6
OUT100	-265.1	624.2	43.5	65.6

Table 13. Pad placement and bump pad dimensions (in microns) (continued)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
OUT99	-188.6	624.2	43.5	65.6
OUT98	-112.1	624.2	43.5	65.6
OUT97	-35.6	624.2	43.5	65.6
OUT96	40.9	624.2	43.5	65.6
OUT95	117.4	624.2	43.5	65.6
OUT94	193.9	624.2	43.5	65.6
OUT93	270.4	624.2	43.5	65.6
OUT92	346.9	624.2	43.5	65.6
OUT91	423.4	624.2	43.5	65.6
OUT90	499.9	624.2	43.5	65.6
OUT89	576.4	624.2	43.5	65.6
OUT88	652.9	624.2	43.5	65.6
OUT87	729.4	624.2	43.5	65.6
OUT86	805.9	624.2	43.5	65.6
OUT85	882.4	624.2	43.5	65.6
OUT84	958.9	624.2	43.5	65.6
OUT83	1035.4	624.2	43.5	65.6
OUT82	1111.9	624.2	43.5	65.6
OUT81	1188.4	624.2	43.5	65.6
OUT80	1264.9	624.2	43.5	65.6
OUT79	1341.4	624.2	43.5	65.6
OUT78	1417.9	624.2	43.5	65.6
OUT77	1494.4	624.2	43.5	65.6
OUT76	1570.9	624.2	43.5	65.6
OUT75	1647.4	624.2	43.5	65.6
OUT74	1723.9	624.2	43.5	65.6
OUT73	1800.4	624.2	43.5	65.6
OUT72	1876.9	624.2	43.5	65.6
OUT71	1953.4	624.2	43.5	65.6
OUT70	2029.9	624.2	43.5	65.6
OUT69	2106.4	624.2	43.5	65.6
OUT68	2182.9	624.2	43.5	65.6
OUT67	2259.4	624.2	43.5	65.6

Table 13. Pad placement and bump pad dimensions (in microns) (continued)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
OUT66	2335.8	624.2	43.5	65.6
OUT65	2412.3	624.2	43.5	65.6
OUT64	2488.9	624.2	43.5	65.6
OUT63	2565.4	624.2	43.5	65.6
OUT62	2641.9	624.2	43.5	65.6
OUT61	2718.4	624.2	43.5	65.6
OUT60	2794.9	624.2	43.5	65.6
OUT59	2871.4	624.2	43.5	65.6
OUT58	2947.9	624.2	43.5	65.6
OUT57	3024.4	624.2	43.5	65.6
OUT56	3100.9	624.2	43.5	65.6
OUT55	3177.4	624.2	43.5	65.6
OUT54	3253.9	624.2	43.5	65.6
OUT53	3330.4	624.2	43.5	65.6
OUT52	3406.9	624.2	43.5	65.6
OUT51	3483.4	624.2	43.5	65.6
OUT50	3559.9	624.2	43.5	65.6
OUT49	3636.4	624.2	43.5	65.6
OUT48	3712.9	624.2	43.5	65.6
OUT47	3789.4	624.2	43.5	65.6
OUT46	3865.9	624.2	43.5	65.6
OUT45	3942.4	624.2	43.5	65.6
OUT44	4018.9	624.2	43.5	65.6
OUT43	4095.4	624.2	43.5	65.6
OUT42	4171.9	624.2	43.5	65.6
OUT41	4248.4	624.2	43.5	65.6
OUT40	4324.9	624.2	43.5	65.6
OUT39	4401.4	624.2	43.5	65.6
OUT38	4477.9	624.2	43.5	65.6
OUT37	4554.4	624.2	43.5	65.6
OUT36	4630.9	624.2	43.5	65.6
OUT35	4707.4	624.2	43.5	65.6
OUT34	4783.9	624.2	43.5	65.6

Table 13. Pad placement and bump pad dimensions (in microns) (continued)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
OUT33	4860.4	624.2	43.5	65.6
OUT32	4936.9	624.2	43.5	65.6
OUT31	5013.4	624.2	43.5	65.6
OUT30	5089.9	624.2	43.5	65.6
OUT29	5166.4	624.2	43.5	65.6
OUT28	5242.9	624.2	43.5	65.6
OUT27	5319.4	624.2	43.5	65.6
OUT26	5395.9	624.2	43.5	65.6
OUT25	5472.4	624.2	43.5	65.6
OUT24	5548.9	624.2	43.5	65.6
OUT23	5625.4	624.2	43.5	65.6
OUT22	5701.9	624.2	43.5	65.6
OUT21	5778.4	624.2	43.5	65.6
OUT20	5854.9	624.2	43.5	65.6
OUT19	5931.4	624.2	43.5	65.6
OUT18	6007.9	624.2	43.5	65.6
OUT17	6084.4	624.2	43.5	65.6
OUT16	6160.9	624.2	43.5	65.6
OUT15	6237.4	624.2	43.5	65.6
OUT14	6313.9	624.2	43.5	65.6
OUT13	6390.4	624.2	43.5	65.6
OUT12	6466.9	624.2	43.5	65.6
OUT11	6543.4	624.2	43.5	65.6
OUT10	6619.9	624.2	43.5	65.6
OUT9	6696.4	624.2	43.5	65.6
OUT8	6772.9	624.2	43.5	65.6
OUT7	6849.4	624.2	43.5	65.6
OUT6	6925.9	624.2	43.5	65.6
OUT5	7002.4	624.2	43.5	65.6
OUT4	7078.9	624.2	43.5	65.6
OUT3	7155.4	624.2	43.5	65.6
OUT2	7231.9	624.2	43.5	65.6
OUT1	7308.4	624.2	43.5	65.6

Table 13. Pad placement and bump pad dimensions (in microns) (continued)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
RIGHT SIDE from top to bottom				
VSSP4	7461.3	635.2	65.6	43.5
VSSP5	7473.2	560.3	65.6	43.5
VSSP6	7473.2	485.4	65.6	43.5
VPP4	7473.2	260.1	65.6	43.5
VPP5	7473.2	185.2	65.6	43.5
VPP6	7473.2	110.3	65.6	43.5
DUMMY	7473.2	35.5	65.6	43.5
VSSLOG2	7473.2	-39.4	65.6	43.5
VSSSUB2	7473.2	-114.3	65.6	43.5
VDD2	7473.2	-189.2	65.6	43.5
VCC2	7473.2	-555.2	65.6	43.5
DUMMY	7461.3	-633.5	65.6	43.5
BOTTOM SIDE from right to left				
DUMMY	6838.2	-622.5	43.5	65.6
DUMMY	6749.7	-622.5	43.5	65.6
DUMMY	6673.1	-622.5	43.5	65.6
DUMMY	6486.3	-622.5	43.5	65.6
DUMMY	6409.8	-622.5	43.5	65.6
DUMMY	6333.3	-622.5	43.5	65.6
DUMMY	6256.8	-622.5	43.5	65.6
DUMMY	6103.6	-622.5	43.5	65.6
TEST2	5928.9	-622.5	43.5	65.6
TEST1	5617.8	-622.5	43.5	65.6
VDD8	4783.9	-622.5	43.5	65.6
BS2	4634.4	-622.5	43.5	65.6
VSSLOG7	4466.3	-622.5	43.5	65.6
BS1	4325.9	-622.5	43.5	65.6
VDD7	4095.4	-622.5	43.5	65.6
DIR	3949.6	-622.5	43.5	65.6
VSSLOG6	3709.5	-622.5	43.5	65.6
FS1	3560.2	-622.5	43.5	65.6
VDD6	3327.0	-622.5	43.5	65.6

Table 13. Pad placement and bump pad dimensions (in microns) (continued)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
FS2	3178.1	-622.5	43.5	65.6
VSSLOG5	2944.5	-622.5	43.5	65.6
RS2	2798.8	-622.5	43.5	65.6
VDD5	2629.4	-622.5	43.5	65.6
RS1	2486.6	-622.5	43.5	65.6
VSSLOG4	2314.1	-622.5	43.5	65.6
DUMMY	648.6	-622.5	43.5	65.6
VREF	117.6	-622.5	43.5	65.6
DUMMY	-271.1	-622.5	43.5	65.6
DUMMY	-424.1	-622.5	43.5	65.6
VDD4	-572.067	-622.5	43.5	65.6
POC	-870.5	-622.5	43.5	65.6
VSSLOG3	-1110.0	-622.5	43.5	65.6
BLK/	-1458.1	-622.5	43.5	65.6
VDD3	-1722.0	-622.5	43.5	65.6
CLK1	-1958.7	-622.5	43.5	65.6
CLK2	-2567.3	-622.5	43.5	65.6
STB1/	-3018.9	-622.5	43.5	65.6
STB2/	-3561.8	-622.5	43.5	65.6
DB1	-4021.4	-622.5	43.5	65.6
DB2	-4632.8	-622.5	43.5	65.6
DB3	-5015.9	-622.5	43.5	65.6
DB4	-5840.8	-622.5	43.5	65.6
DB5	-6114.5	-622.5	43.5	65.6
DB6	-7094.6	-622.5	43.5	65.6

Table 13. Pad placement and bump pad dimensions (in microns) (continued)

Lead pad name	Pad placements		Bump dimensions	
	X	Y	X	Y
LEFT SIDE from bottom to top				
VCC1	-7474.9	-555.2	65.6	43.5
VDD1	-7474.9	-189.2	65.6	43.5
VSSSUB1	-7474.9	-114.3	65.6	43.5
VSSLOG1	-7474.9	-39.4	65.6	43.5
DUMMY	-7474.9	35.5	65.6	43.5
VPP3	-7474.9	110.3	65.6	43.5
VPP2	-7474.9	185.2	65.6	43.5
VPP1	-7474.9	260.1	65.6	43.5
VSSP3	-7474.9	485.5	65.6	43.5
VSSP2	-7474.9	560.3	65.6	43.5
VSSP1	-7462.9	635.2	65.6	43.5

12 Tested wafer disclaimer

All wafers are tested and guaranteed to comply with this specification until the wafer sawing stage, for a period of ninety (90) days from the delivery date.

Please remember that it is the customer's responsibility to test and qualify their application using the STMicroelectronics die. STMicroelectronics is ready to support customers when qualifying the product.

13 Ordering information

Table 14. Order codes

Part number	Description
STV7622/BMP	Tested and usawn bump wafer (u = die)

14 Revision history

Table 15. Document revision history

Date	Revision	Changes
29-May-2007	1	Initial release

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