TSM1N60S

N-Channel Power Enhancement Mode MOSFET

TO-92

Pin assignment:
1. Gate
2. Drain
3. Source

V_{DS} = 600V
I_D = 0.3A
$R_{DS\ (on)}$, Vgs @ 10V, Ids @ 0.3A = 11Ω

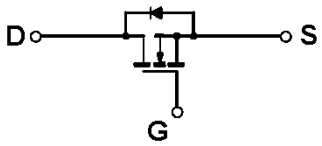
General Description

The TSM1N60s is used an advanced termination scheme to provide enhanced voltage-blocking capability without degrading performance over time. In addition, this advanced MOSFET is designed to withstand high energy in avalanche and commutation modes. The new energy efficient design also offers a drain- to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies and converters, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional and safety margin against unexpected voltage transients.

Features

- ✧ Robust high voltage termination
- ✧ Avalanche energy specified
- ✧ Diode is characterized for use in bridge circuits
- ✧ Source to Drain diode recovery time comparable to a discrete fast recovery diode.
- ✧ I_{DSS} and $V_{DS(on)}$ specified at elevated temperature

Block Diagram



Ordering Information

Part No.	Packing	Package
TSM1N60SCT B0	Bulk Pack	TO-92
TSM1N60SCT A3	Ammo Pack	TO-92

Absolute Maximum Rating (Ta = 25 °C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	600V	V
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current		I_D	0.3	A
Pulsed Drain Current		I_{DM}	1.2	A
Maximum Power Dissipation	Ta = 25 °C	P_D	3	W
	Ta > 25 °C		0.025	W/°C
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C
Single Pulse Drain to Source Avalanche Energy (V_{DD} = 50V, V_{GS}=10V, I_{AS}=0.3A, L=115mH)		E_{AS}	50	mJ

Thermal Performance

Parameter	Symbol	Limit	Unit
Lead Temperature (1/8" from case)	T_L	10	S
Junction to Ambient Thermal Resistance (PCB mounted)	Rθja	50	°C/W

Note: Surface mounted on FR4 board t<=10sec.

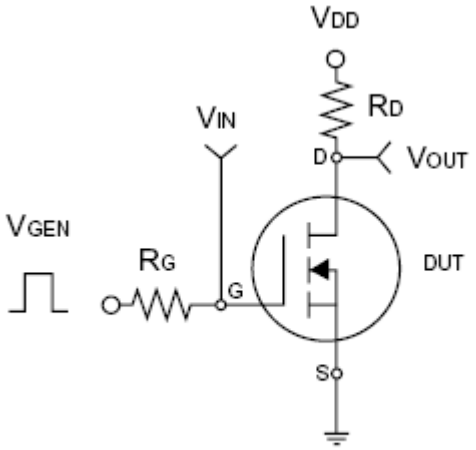
Electrical Characteristics

Tj = 25 °C, unless otherwise noted

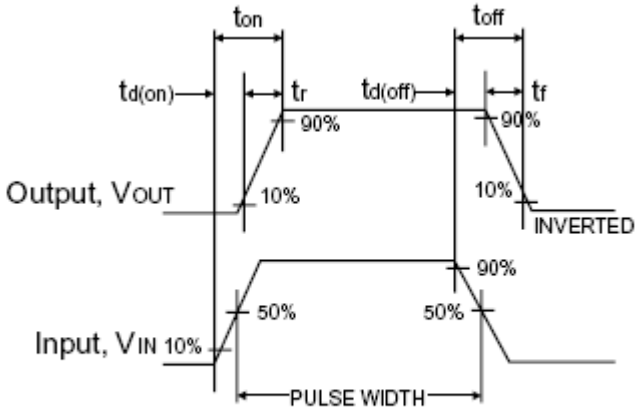
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = 250uA	BV_{DSS}	600	--	--	V
Drain-Source On-State Resistance	V_{GS} = 10V, I_D = 0.3A	$R_{DS(ON)}$	--	11	13	Ω
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250uA	$V_{GS(TH)}$	2.0	--	4.0	V
Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V	I_{DSS}	--	--	10	uA
Gate Body Leakage	V_{GS} = ± 30V, V_{DS} = 0V	I_{GSS}	--	--	± 100	nA
Forward Transconductance	V_{DS} ≧50V, I_D = 0.3A	g_{fs}	--	5	--	S
Dynamic						
Total Gate Charge	V_{DS} = 480V, I_D = 0.3A, V_{GS} = 10V	Q_g	--	4.5	6.0	nC
Gate-Source Charge		Q_{gs}	--	1.1	--	
Gate-Drain Charge		Q_{gd}	--	2.0	--	
Turn-On Delay Time	V_{DD} = 300V, I_D = 0.3A, V_{GEN} = 10V, R_G = 4.7Ω	$t_{d(on)}$	--	10	30	nS
Turn-On Rise Time		t_r	--	20	50	
Turn-Off Delay Time		$t_{d(off)}$	--	25	45	
Turn-Off Fall Time		t_f	--	24	60	
Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	155	200	pF
Output Capacitance		C_{oss}	--	20	26	
Reverse Transfer Capacitance		C_{rss}	--	3	4	
Source-Drain Diode						
Max. Diode Forward Current		I_S	--	--	0.3	A
Diode Forward Voltage	I_S = 0.3A, V_{GS} = 0V	V_{SD}	--	--	1.4	V

Note: 1. pulse test: pulse width <=300uS, duty cycle <=2%

2. Negligible, Dominated by circuit inductance.



Switching Test Circuit

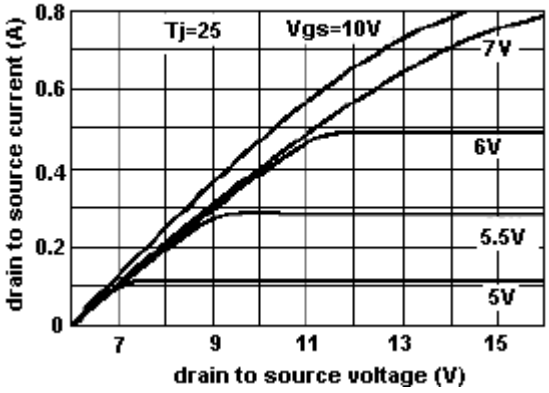


Switchin Waveforms

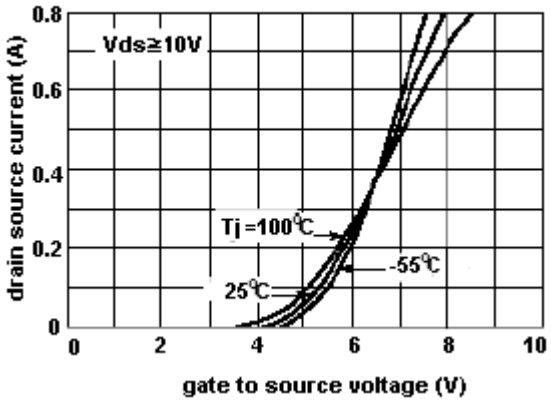
TSC

Typical Characteristics Curve (Ta = 25 °C unless otherwise noted)

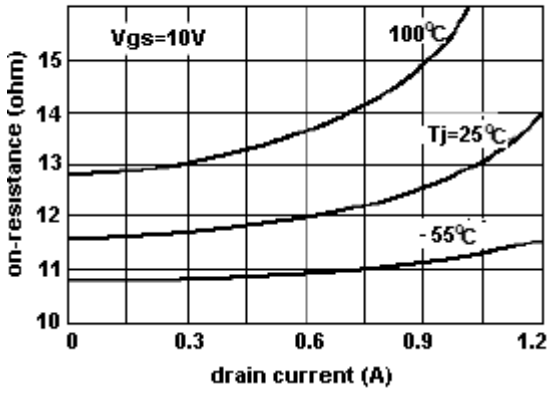
Output Characteristic



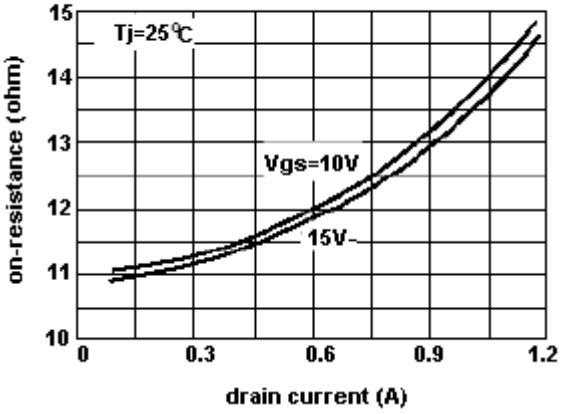
Transfer Characteristic



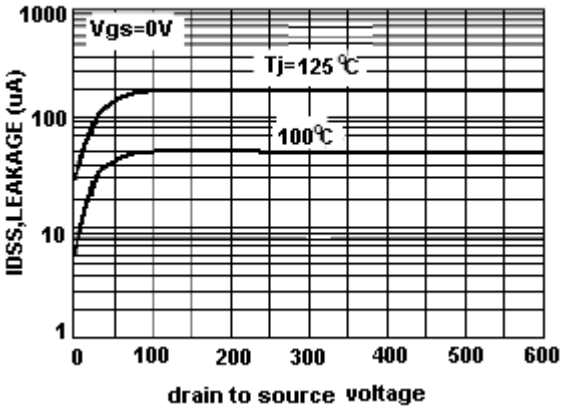
On Resistance vs Drain Current



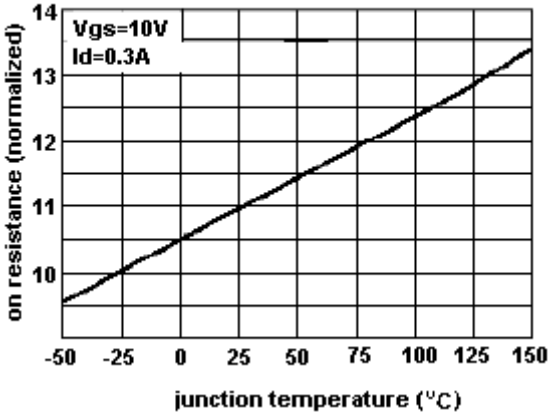
On Resistance vs Gate-Source



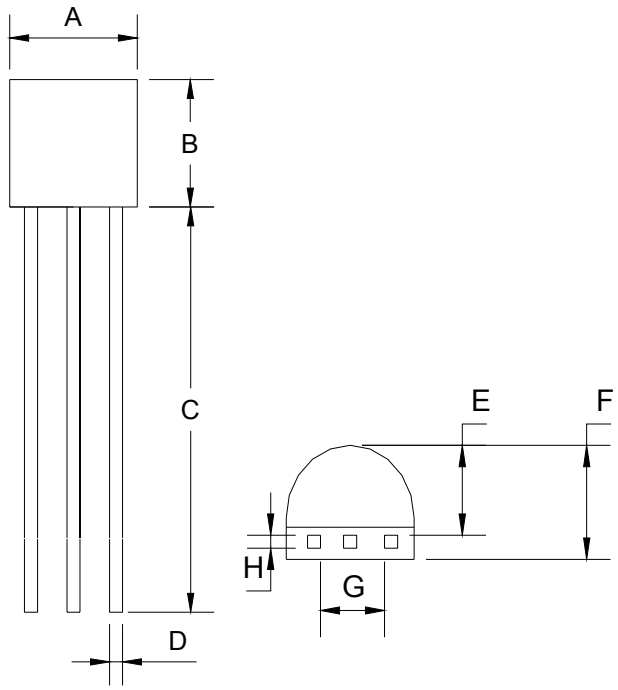
Drain To Source Leakage



On Resistance vs Junction temp



TO-92 Mechanical Drawing



TO-92 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.70	0.169	0.185
B	4.30	4.70	0.169	0.185
C	14.30(typ)		0.563(typ)	
D	0.43	0.49	0.017	0.019
E	2.19	2.81	0.086	0.111
F	3.30	3.70	0.130	0.146
G	2.42	2.66	0.095	0.105
H	0.37	0.43	0.015	0.017