TOSHIBA Bipolar Linear Integrated Circuit Silicon Monolithic

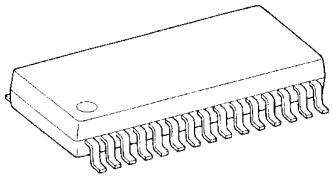
TA1383AFG

NTSC Chroma Decoder, Multi-Point Scan Sync Processor,
H/V Frequency Counter IC for Color TV

TA1383AFG integrates an NTSC chroma decoder, multi-point scan sync processor (equivalent to pin D4), and H/V frequency counter in a 30-pin flat package. The IC is ideal for double scan TVs.

The baseband signal processing block incorporates sub adjustment circuits and a RGB/Y color difference matrix. The sync processor block supports 525I/P, 750P, and 1125I.

TA1383AFG incorporates the I^2C bus. The device can control various functions via the bus line.



SSOP30-P-375-1.00

Weight: 0.63 g (typ.)

Features

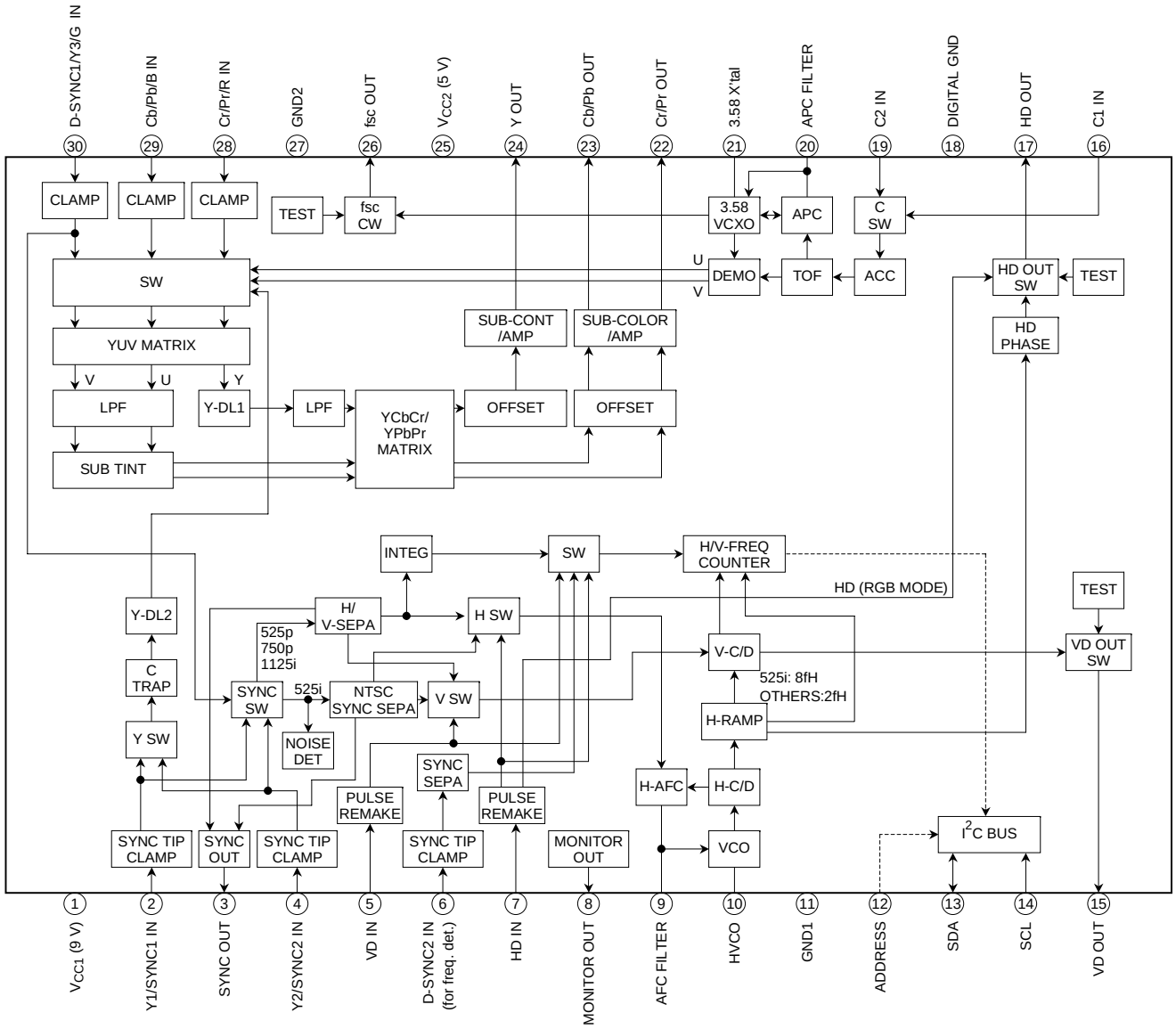
Luminance block
- Chroma trap
- Y delay line

Chroma block
- NTSC decoder
- TOF

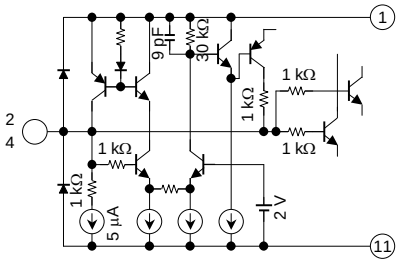
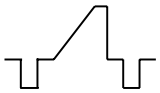
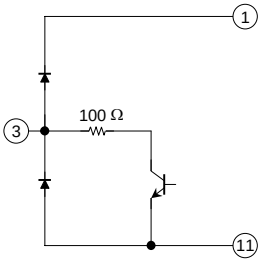
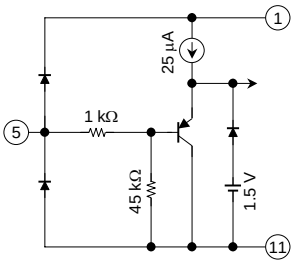
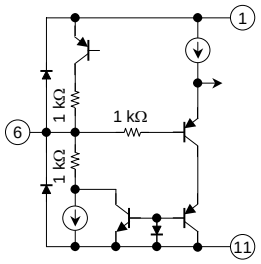
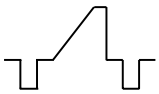
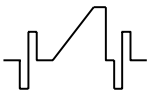
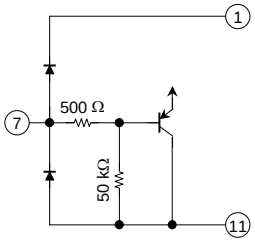
Baseband block
- Sub contrast
- Sub tint
- Sub color
- Y delay line
- Offset adjustment
- ADC pre-filter (LPF)
- +6dB amp (ON/OFF)
- YCbCr/YPbPr/RGB input supported
- YCbCr/YPbPr output switchable

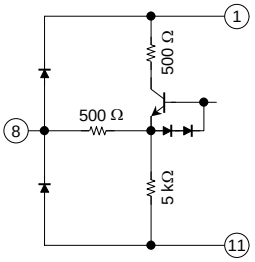
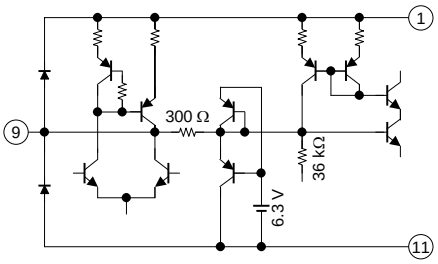
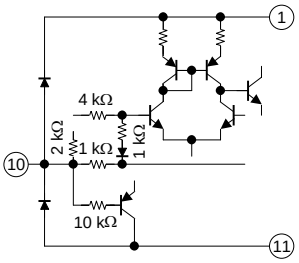
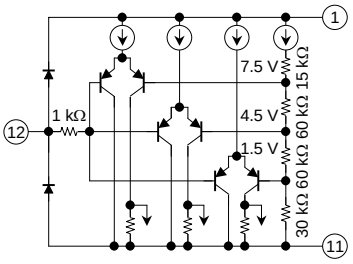
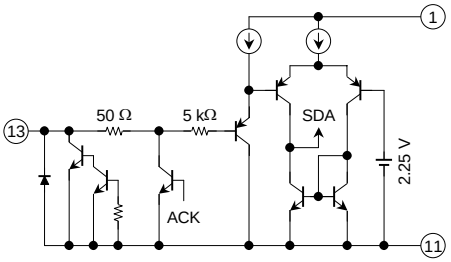
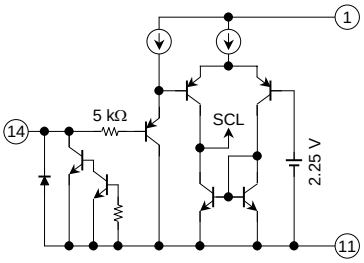
Sync block
- High-performance sync separator (at NTSC (525I))
- Horizontal sync (15.734 k, 31.5 k, 33.75 k, 45 kHz)
- Vertical sync playback function (525I/P, 750P, 1125I)
- 2- and 3-level sync separator circuit
- HD/VD input (positive and negative polarities)
- HD/VD output (positive and negative polarities switchable)
- Horizontal/vertical frequency counting function
- Copy guard

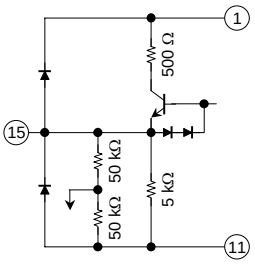
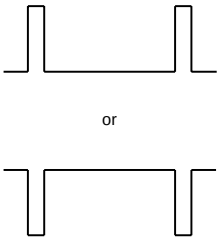
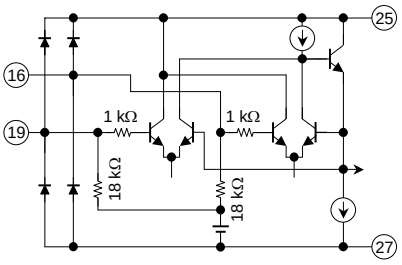
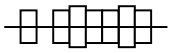
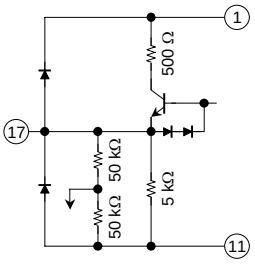
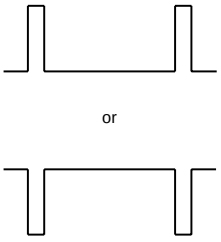
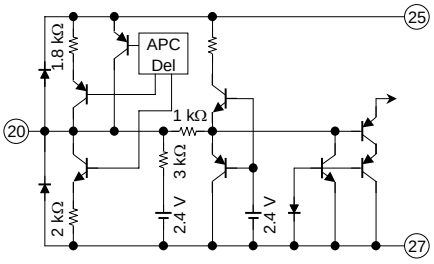
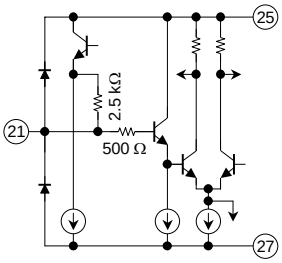
Block Diagram

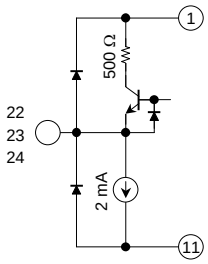
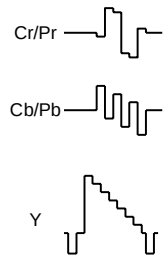
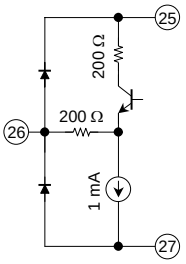
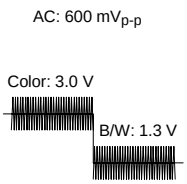
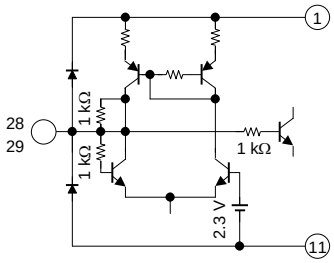
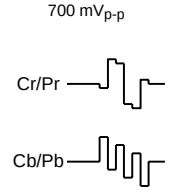
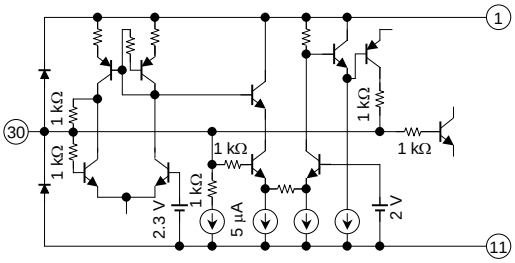
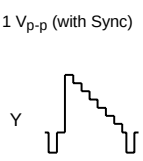


Pins (unless otherwise specified, V_{CC1} = 9 V, V_{CC2} = 5 V, Ta = 25°C)

Pin No.	Symbol	Function	Interface	I/O Signal
1	V_{CC1} (9 V)	V_{CC} for sync separation block, outputs, and interface. Connects 9 V (typ.).	—	—
2 4	Y1/SYNC1 IN Y2/SYNC2 IN	Y signal input pin. Inputs NTSC (525I) signal via clamp capacitor. Sync signal is separated from Y signal input to this pin. Can also be used for sync-only input pins. When not used, leave open.		1 V_{p-p} (with Sync) Sync-Tip: 2.0 V 
3	SYNC OUT	Outputs sync-separated C-SYNC. Open collector output.		High/Low
5	VD IN	Inputs vertical sync VD signal. Inputs positive- and negative-polarity signals. When not used, leave open.		Th: 0.7 V or Th: 0.7 V
6	D-SYNC2 IN (for freq. det.)	Inputs Y signal for identifying frequency. Inputs Y signals such as 525IP, 720P, and 1125I via clamp capacitor. When not used, leave open.		1 V_{p-p} (with Sync) Sync-Tip: 2.0 V  or 
7	HD IN	Inputs horizontal sync HD signal. Inputs positive- and negative-polarity signals. When not used, leave open.		Th: 0.7 V or Th: 0.7 V

Pin No.	Symbol	Function	Interface	I/O Signal
8	MONITOR OUT	Monitor output pin. Emitter follower output. Selects output signal according to bus setting.		—
9	AFC FILTER	Connects horizontal AFC filter. Voltage of this pin determines horizontal output frequency.		—
10	HVCO	Connects ceramic oscillator for horizontal oscillation. Use Murata CSBLA503KECZF30 or CSBFB503KJCZF60.		—
11	GND1	GND pin for 9-V block.	—	—
12	ADDRESS	Switches slave addresses. Slave addresses are set according to voltage of this pin. V_{CC} (9 V): DE_H/DF_H 6 V: DC_H/DD_H 3 V: DA_H/DB_H GND: $D8_H/D9_H$		V_{CC}: DE_H/DF_H — V_{CC} (9 V) 6 V: DC_H/DD_H — 7.5 V 3 V: DA_H/DB_H — 4.5 V GND: $D8_H/D9_H$ — 1.5 V GND
13	SDA	I^2C bus SDA pin.		—
14	SCL	I^2C bus SCL pin.		—

Pin No.	Symbol	Function	Interface	I/O Signal
15	VD OUT	Vertical sync VD output pin. Emitter follower output. Sets polarity of output signal according to bus setting.		
16 19	C1 IN C2 IN	Inputs chroma signal via clamp capacitor. When not used, leave open.		Burst: 300 mV_{p-p} 
17	HD OUT	Horizontal sync HD output pin. Emitter follower output. Sets polarity of output signal according to bus setting.		
18	DIGITAL GND	GND pin for digital block.	—	—
20	APC FILTER	Connects APC filter for chroma demodulation.		—
21	3.58 MHz X'tal	Connects recommended 3.58-MHz oscillator for chroma demodulation.		—

Pin No.	Symbol	Function	Interface	I/O Signal
22 23 24	Cr/Pr OUT Cb/Pb OUT Y OUT	Output Y, Cb, and Cr, or Y, Pb, and Pr signals. Emitter follower output. Set output format and amplitude according to bus setting.		
25	V_{CC2} (5 V)	V_{CC} for Y, chroma, and baseband processing block. Connects 5 V (typ.).	—	—
26	CW OUT	fsc carrier wave (CW) output pin. Emitter follower output.		
27	GND2	GND pin for 5-V block	—	—
28 29	Cr/Pr/R IN Cb/Pb/B IN	Inputs 525I/P, 1125I, and 750P Cr/Pr/R and Cb/Pb/B signal via clamp capacitor. Set input format according to bus setting. When not used, connect 0.1 μF between this pin and GND.		
30	D-SYNC1/Y3/G IN	Inputs 525I/P, 750P, and 1125I Y signal or G signal via clamp capacitor. Sync signal is separated from Y (G) signal input to this pin. Set input format according to bus setting. When not used, connect 0.1 μF between this pin and GND.		

Bus Control Map

Write Data Slave Address: D8/DA/DC/DE$_H$

SA	D7	D6	D5	D4	D3	D2	D1	D0	Preset	
00	READ SW	INPUT SW			H/V FREQ			AFC-RAN	1000	0000
01	FREQ DET SW		H-SEP LVL		V-SEP LVL		D-SY2 SEP LVL		1000	0000
02	AFC-MODE			NOISE LVL		MONITOR			1000	0000
03	525I-SEP	MATRIX SW		BANDWIDTH		V-MODE	TEST		1000	0000
04	GAIN SW	HD-POL	VD-POL	C-TRAP	HD POSI				1000	0000
05	SUB-CONT					TOF f0			1000	0000
06	SUB-COLOR					TOF Q			1000	0000
07	SUB-TINT				Y-DL1		Y-DL2		1000	0000
08	Y BLACK ADJ								1000	0000
09	Cr BLACK ADJ								1000	0000
0A	Cb BLACK ADJ								1000	0000

Note 1: SA: Sub-Address

Read Data Slave Address: D9/DB/DD/DF$_H$

Read Mode 1 (read SW = 1)

	D7	D6	D5	D4	D3	D2	D1	D0
0	POR	COLOR	C-GUARD	N-DET	V-STD	H-LOCK	HD-OUT	VD-OUT
1	SYNC-IN	Y1/2-IN	Y3-IN	D-SYNC2	H-STAB	V-SYNC	ACC	V-SKEW

Read Mode 2 (read SW = 0)

	D7	D6	D5	D4	D3	D2	D1	D0
0	C-SYNC	V FREQUENCY DET						
1	H FREQUENCY DET							

Bus Control Functions

Write Function

Signal	Function	Power-On Initial Value
READ SW	Switches Read Mode. Switches Read Mode. 0: READ MODE 2 (counts frequency) 1: READ MODE 1 (self diagnosis)	Self diagnosis (1)
INPUT SW	Switches luminance, chroma, and sync signals. 000: SYNC1/Y1/C1 001: SYNC2/Y1/C1 010: SYNC2/Y2/C2 011: SYNC2/Y3/CbCr (PbPr) 100: D-SYNC1/Y3/CbCr (PbPr) 101: D-SYNC1/RGB 110: HD/VD/Y3/CbCr (PbPr) 111: HD/VD/RGB	SYNC1/Y1/C1 (000)
H/V FREQ	Switches horizontal oscillation frequency and vertical pull-in range. 000: Horizontal oscillation frequency 15.734 kHz, vertical pull-in range 224.5H to 297H (262.5H at quiescent) 001: Horizontal oscillation frequency 31.5 kHz, vertical pull-in range 48H to 612H (525H at quiescent) 010: Horizontal oscillation frequency 33.75 kHz, vertical pull-in range 48H to 636H (562.5H at quiescent) 011: Horizontal oscillation frequency 45 kHz, vertical pull-in range 48H to 848H (750H at quiescent) 100: Horizontal oscillation frequency 15.734 kHz, forced vertical pull-in range 262.5H 101: Horizontal oscillation frequency 15.734 kHz, vertical pull-in range 32.5H to 297H (at multi-windows) 110: D5 (1125P/60 Hz) input mode (H: 33.75 kHz Free-run, V: 48H to 636H) Internal clamping pulse, internal H-BLK and HD output are generated by inputted sync. When no-signal inputted, the clamp pulse, the H-BLK and VD output are switched to free-run signals of 33.75 kHz/562.5H. And then, HD output is gone. Set AFC-Mode = (111) and INPUT SW = (100), when this mode used. 111: RGB Input Mode (H frequency 33.75 kHz Free-run, V pull-in range 48H to 740H) Input HD signal is used as clamp pulse. HD/VD-OUT outputs are remade of input signals. (H-pull-in range: 5.7 kHz to 120 kHz, V-pull-in range: 47 Hz to 688 Hz, HD input width: 0.2 μs to 10 μs, VD input width: 3 μs to 1.45 ms) When no-signal inputted, the clamp pulse, the H-BLK and VD output are switched to free-run signals of 33.75 kHz/562.5 H. And then, HD output is gone. Set AFC-Mode = (111) and INPUT SW = (111), when this mode used. In this mode, when TEST = 01, V-pull-in range becomes 0 to 688 Hz. Then, VD output is gone when no-input.	H: 15.734 kHz V: 224.5H to 297H (000)
AFC-RAN	Switches horizontal AFC pull-in range. Switches pull-in range of 525I/P, 750P, and 1125I horizontal frequencies. 0: NORMAL 1: Narrow	NORMAL (0)
FREQ DET SW	Switches frequency counting input. Switches input pin for counting frequency. 00: 525I1 (rejects pulse of 1.75 μs or less.) (pins 2, 4, and 30) 01: 525I2 (inputs H-sync for AFC. (and rejects pulse of 0.3 μs or less.)) (pins 2, 4, and 30) 10: D-SYNC2 (pin 6) 11: HD/VD (pins 5 and 7) Note: To count frequency, use Bus Mode (10/11). However, note that in Bus Mode (00/01), frequencies such as 525P, 750P, and 1125I cannot be counted. In this mode (00/01), frequencies may not be counted accurately due to weak electric fields or ghosts.	D-SYNC2 (10)

Signal	Function	Power-On Initial Value
H-SEP LVL	Switches sync separation level of horizontal sync signal. Switches sync separation level of horizontal sync signal input to sync input pins. At 525I 00: 20% 01: 27% 10: 34% 11: 40% At 525P 00: 20% 01: 30% 10: 40% 11: 50% Three-level sync 00: 25% 01: 35% 10: 45% 11: 55%	20% (00)
V-SEP LVL	Switches sync separation level of vertical sync signal. Switches sync separation level of vertical sync signal input to sync input pins. At 525I 00: 40% 01: 50% 10: 60% 11: 70% At 525P 00: 20% 01: 30% 10: 40% 11: 50% Three-level sync 00: 25% 01: 35% 10: 45% 11: 55%	40% (00)
D-SY2 SEP LVL	Switches sync separation level of D-SYNC2 IN (pin 6). Switches sync separation level of sync signal input to pin 6. 00: 20% 01: 30% 10: 40% 11: 50%	20% (00)
AFC-MODE	Switches AFC gain. Switches AFC gain setting mode. 000: AUTO1 (normal: 0dB, at skew: +6dB, at noise: −12dB) 001: AUTO2 (AUTO1 + prevention against AFC disoperation at noise + stabilization of AFC in weak electric field + ghost prevention) 010: AUTO3 (Video input mode: AUTO2 + 0dB at V-SKEW detected) 011: AUTO4 (RF input mode: AUTO2 + 0dB at V-SKEW detected, however, −12dB at normal. Also, AFC gain is not controlled by noise detection result) 100: Forced +6dB 101: Forced 0dB 110: Forced −12dB 111: Forced Off (horizontal free running) Note: Set AUTO1 to 4 according to input signal status.	Forced +6dB (100)
NOISE LVL	Switches noise detection level. Switches noise detection level. Noise is detected only in NTSC signals (525I). Noise detection result is reflected in BUS READ and AFC-GAIN operation (as in AUTO1 to 3 modes). 00: max 11: min	max (00)
MONITOR	Switches MONITOR output. Switches signal output from MONITOR OUT (pin 8). Field identification output is valid for 525I and 1125I standard signal. 000: 1-bit DAC output (high) 001: 1-bit DAC output (low) 010: Field identification output (ODD: low, EVEN: high) 011: Noise detection output 100: V sync separation output at 525I 101: Skew detection output 110: Clamp pulse output 111: H/V-SYNC at D-SYNC2 input	DAC HIGH (000)

Signal	Function	Power-On Initial Value
525I-SEP	Switches 525I SEP Mode Switches H-SEP Mode. (Countermeasure ghost signal) 0: ON Automatically controls that H-SEP level does not go higher than V-SEP level, the initial value is 40%. 1: OFF	(1) OFF
MATRIX SW	Switches matrix. Sets I/O signal format for input pins (28, 29, and 30) and output pins (22, 23, and 24). 00: MODE-1 (YC1/YC2 → YCbCr, Y3/CbCr → YCbCr, RGB → YCbCr) 01: MODE-2 (YC1/YC2 → YCbCr, Y3/PbPr → YCbCr, RGB → YCbCr) 10: MODE-3 (YC1/YC2 → YPbPr, Y3/CbCr → YPbPr, RGB → YPbPr) 11: MODE-4 (YC1/YC2 → YPbPr, Y3/PbPr → YPbPr, RGB → YPbPr) Note: Set this function together with INPUT SW, H/V FREQUENCY for each input signal.	(00)
BANDWIDTH	Switches bandwidth limiting filter (ADC pre-filter). Sets bandwidth of bandwidth limiting filter and image mute. 00: OFF (through) 01: Filter 1 (Y: 10.3 MHz/−3dB, Cb/Cr: 4.2 MHz/−3dB) 10: Filter 2 (Y: 14.6 MHz/−3dB, Cb/Cr: 6.5 MHz/−3dB) 11: Image mute (Y: −20IRE, CbCr: 0IRE)	OFF (00)
V-MODE	Switches vertical sync playback mode. Switches VD OUT (pin 15) sync playback mode. 0: PLL Mode for standard signals 1: Direct Sync Mode Note 1: Setting 0 is valid only for standard signals. For other signals, set to Direct Sync Mode. In PLL Mode for standard signals, VD output starts with 4-μs delay in relation to V-SYNC. For other signals, 0.25-H delay. Note 2: Set this register to (1) except inputting the NTSC and 525I composite sync format.	PLL for standard signals (0)
TEST	Shipment Test Mode. When TEST = 01 and H/V FREQ = 111, V-pull-in range is expanded (Refer to H/V FREQ function explanation). In other case, set to 00.	(00)
GAIN SW	Switches output gain. Sets output amp gain for pins 22, 23, and 24. 0: +6dB 1: 0dB	0dB (1)
HD-POL	Switches HD output polarity. Sets HD OUT (pin 17) polarity. 0: Positive polarity 1: Negative polarity	Positive polarity (0)
VD-POL	Switches VD output polarity. Sets VD OUT (pin 15) polarity. 0: Positive polarity 1: Negative polarity	Positive polarity (0)
C-TRAP	Switches chroma trap. Switches chroma trap for image signals input to pins 2 and 4. 0: OFF 1: ON	OFF (0)
HD POSI	Adjusts HD output phase. Sets output phase of HD OUT (pin 17). 0000: 800 ns (2.7% of H cycle) ahead of sync center 1111: Sync center Note: Sync center is based on 33.75 kHz/3-level sync.	(0000)

Signal	Function	Power-On Initial Value
SUB-CONT	Adjusts subcontrast. Adjusts amplitude of output Y signal (pin 24). 00000: min (−3dB) 11111: max (+3dB)	CENTER (10000)
TOF f0	Switches TOF center frequency. Controls center frequency of chroma filter for chroma signals input to pins 16 and 19. 000: OFF 001: min (0.56 fsc) 111: max (1.05 fsc)	OFF (000)
SUB-COLOR	Adjusts sub color. Adjusts amplitude of output Cb/Cr (Pb/Pr) signals (pins 22 and 23). 00000: min (−3dB) 11111: max (+3dB)	CENTER (10000)
TOF Q	Switches TOF Q characteristic. Controls center frequency of chroma filter for chroma signals input to pins 16 and 19. 000: min (0.6) 111: max (1.2)	min (000)
SUB-TINT	Adjusts sub tint. Adjusts tint for output Cb/Cr (Pb/Pr) signals (pins 22 and 23). 0000: min (−7 deg) 1111: max (+7 deg)	CENTER (1000)
Y-DL1	Adjusts Y delay time 1 (baseband block). Switches delay amount of Y signal in baseband block. 00: −10 ns 01: 0 ns 10: +10 ns 11: +10 ns Note: Sets delay amount according to settings such as BANDWIDTH.	−10 ns (00)
Y-DL2	Adjusts Y delay time 2 (NTSC Y processing block). Switches delay amount of Y signal in NTSC Y processing block. 00: OFF 01: +40 ns 10: +80 ns 11: +120 ns Note: Sets delay amount according to settings such as TOF f0/Q.	OFF (00)
Y BLACK ADJ	Adjusts Y black level. Adjusts black level offset of Y OUT (pin 24). 00000000: OFF 00000001: min (−140 mV) 11111111: max (+140 mV)	CENTER (10000000)
Cb BLACK ADJ	Adjusts Cb (Pb) black level. Adjusts black level offset of Cb (Pb) OUT (pin 23). 00000000: OFF 00000001: min (−140 mV) 11111111: max (+140 mV)	CENTER (10000000)
Cr BLACK ADJ	Adjusts Cr (Pr) black level. Adjusts black level offset of Cr (Pr) OUT (pin 22). 00000000: OFF 00000001: min (−140 mV) 11111111: max (+140 mV)	CENTER (10000000)

Read Function

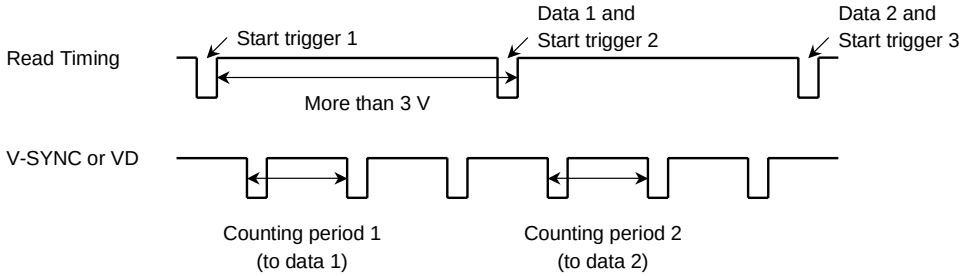
Signal	Function
POR	Power-on reset 0: RESISTER PRESET 1: NORMAL After power on, 0 is returned at first read; 1, at second and subsequent reads.
COLOR	Detects NTSC color or BW (Black and White). 0: BW 1: NTSC color

Signal	Function
C-GUARD	Detects copy guard (pseudo SYNC). 0: No copy guard detected 1: Copy guard detected Detects whether input signal has copy-guard signal in the systems of 60-Hz 525 I/P, 60-Hz 1125 I, and 60-Hz 750 P, but does not detect copy-guard of HD/VD input signal.
N-DET	Detects noise. 0: Small amount detected 1: Large amount detected Set noise detection level in NOISE LEVEL. N-DET is detected only when 525I Y or CVBS signal is input.
V-STD	Detects NTSC standard/non-standard. 0: Standard detected 1: Non-standard detected Detects vertical-sync-signal input in standard cycle. V-STD is detected only when 525I Y or CVBS signal is input.
H-LOCK	Detects H-LOCK. 0: Unlock detected 1: Lock detected Detects lock/unlock of input signal and H-AFC. H-LOCK is detected in the systems of 60-Hz 525 I/P, 60-Hz 1125 I, and 60-Hz 750 P. Note: This register may show UN-LOCK, when H-SYNC width of 525I Y or CVBS input is narrow.
HD-OUT	Detects HD-OUT (pin 17) self-diagnosis. 0: NG (no signal) 1: OK (signal detected)
VD-OUT	Detects VD-OUT (pin 15) self-diagnosis. 0: NG (no signal) 1: OK (signal detected)
SYNC-IN	Detects SYNC IN (pins 2 and 4 or 30) self-diagnosis. 0: NG (no signal) 1: OK (signal detected) At small signal, NG.
Y1/2-IN	Detects Y1/2 IN (pin 2 or 4) self-diagnosis. 0: NG (no signal) 1: OK (signal detected) At small signal, NG.
Y3-IN	Detects Y3 IN (pin 30) self-diagnosis. 0: NG (no signal) 1: OK (signal detected) At small signal, NG.
D-SYNC2	Detects D-SYNC2 IN (pin 6) self-diagnosis. 0: NG (no signal) 1: OK (signal detected) At small signal, NG.
H-STAB	Detects stability of horizontal signal. 0: Stable 1: Not stable Determines not stable when fluctuation of horizontal signal is detected within one field. H-STAB is detected only when 525I Y or CVBS signal is input.
V-SYNC	Detects vertical sync of input signal. 0: No vertical sync detected 1: Vertical sync detected Detects whether input signal has vertical sync. V-SYNC is detected in the systems of 60-Hz 525 I/P, 60-Hz 1125 I, and 60-Hz 750 P.
ACC	Detects status of automatic color control (ACC) circuit. 0: Maximum 1: Other ACC is detected only when NTSC signal is input.

Signal	Function
V-SKEW	Detects vertical skew of VCR. 0: no skew 1: skew V-SKEW is detected only when NTSC signal is input.
C-SYNC	Detects 2-/3-level sync of D-SYNC2 IN (pin 6). 0: 2-level sync 1: 3-level sync Detects sync width per 1H. Note: If 525I/P 60-Hz signal has half SYNC width or less, 3-level sync may be determined.
V FREQUENCY DET	Counts vertical frequency of signal selected by FREQ DET SW. 0000000 to 0011100: No VD 0011101: Vicinity of 195 Hz 1111111: Vicinity of 44.6 Hz How to calculate vertical frequency (X); Converts data read from V-FREQ DET into decimal value and calls value Y. Z = 176.54 μs. Vertical frequency (X) = 1 ÷ (Y × Z) [Hz] Vertical frequency error is Y = −1 to +1. When vertical frequency is 195 Hz or more, frequency cannot be counted accurately. Note that time constant used to integrate C.SYNC then separate V-SYNC is 9 μs (error ±1 μs). Data read first time after power on are undefined.
H FREQUENCY DET	Counts horizontal frequency of signal selected by FREQ DET SW. 00000000: Quiescent 11111111: 120 kHz or more How to calculate horizontal frequency (X); X, Y, and Z are defined the same as those for vertical frequency. Horizontal frequency (X) = Y ÷ (12 × Z) [kHz] Horizontal frequency error is Y = −1 to +2. When horizontal frequency is 120 kHz or more, frequency cannot be counted accurately. When horizontal frequency is approx. 142 kHz to approx. 200 kHz, data are read as 00000000 by the timing of counting. When V-SYNC or VD is not input, horizontal frequency cannot be counted. Data are read as 00000000. Data read first time after power on are undefined.

Note 1: To count horizontal or vertical frequency, data are read between the first V-SYNC/VD and the second V-SYNC/VD following the reset pulse generated at the second byte as the start trigger. To stabilize data, set the bus read interval to 3 V or longer. Discard the data read the first time because they are undefined. However the frequency is counted when BUS is read at Read Mode 1. Therefore the data that is BUS read at Read Mode 2 is valid.

Note 2: Even when Read Mode 1 is switched to Read Mode 2, set the BUS read interval to 3 V or longer.
Figures of BUS read interval at Read Mode 2



Figures of BUS read interval at Read Mode 2

Note 3: Though there is no restriction for setting BUS read interval at Read Mode 1, set the interval to 1 V per one period at shortest to read the data accurately.

Decision algorithm (detection range, detection times and so on) for H/V frequency detection should be determined under consideration of forward Notes and the other factors such as signal strength, existence of ghost signal, APC stability, I^2C BUS data transmission and so on via prototype TV set evaluation.

How To Start I^2C Bus

After power on, TA1383FG pins 28 and 29 (Cr/Pr/R IN, Cb/Pb/B IN) are in Full-Field Clamp Mode.

Full-Field Clamp Mode is released by writing or reading. And then, clamp is performed only during the clamp pulse period.

Described below is how to send bus data after power on. Use software to handle the procedure.

1. Turn power on.
2. Transmit all write data.

How To Transmit/Receive Via I^2C Bus

Slave Address: Can Be Changed Using Pin 12. (V_{CC1} = 9 V, V_{CC2} = 5 V)

Pin 12-GND (GND to 1.2 V): D8H/D9H

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	0	0	0/1

Pin 12-3 V (1.8 to 4.2 V): DAH/DBH

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	0	1	0/1

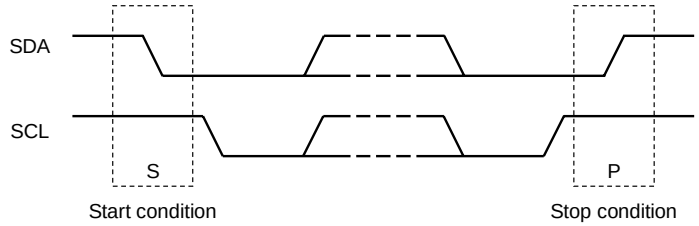
Pin 12-6 V (4.8 to 7.2 V): DCH/DDH

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	0	0/1

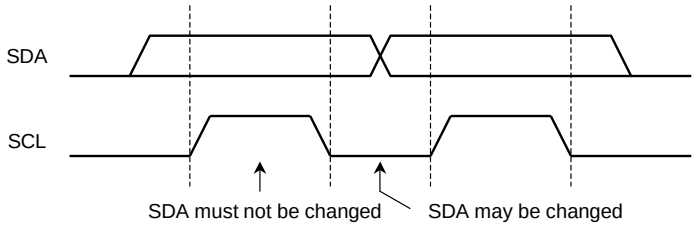
Pin 12-V_{CC1} (7.8 to V_{CC1}) DEH/DFH

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	1	1	0/1

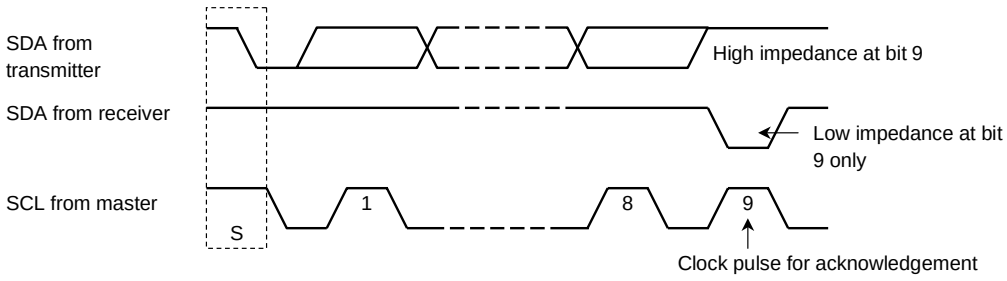
Start and Stop Conditions



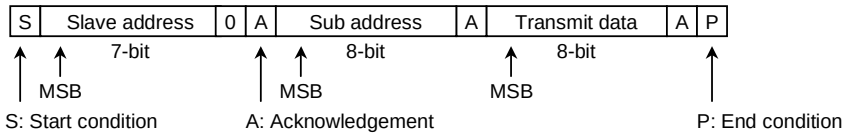
Bit Transmission



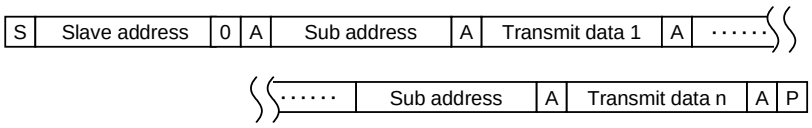
Acknowledgement



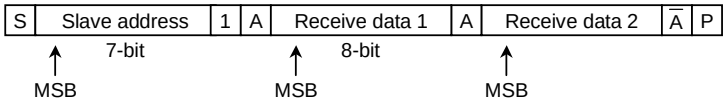
Data Transmit Format 1



Data Transmit Format 2



Data Receive Format

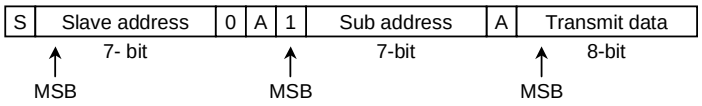


To receive data, the master transmitter changes to the receiver immediately after the first acknowledgement. The slave receiver changes to the transmitter.

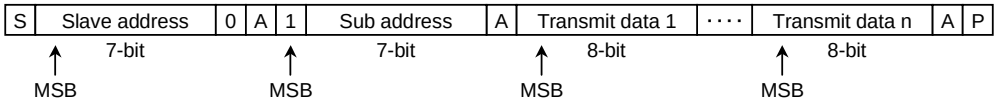
The end condition is always created by the master.

Optional Data Transmit Format

Auto Increment Mode 1



Auto Increment Mode 2



In this way, sub addresses are automatically incremented from the specified sub address and data are set.

I^2C BUS Conditions

Characteristics	Symbol	Min	Typ.	Max	Unit
Low level input voltage	V_{IL}	0	—	1.0	V
High level input voltage	V_{IH}	1.8	—	Vcc	V
Low level output voltage at 3 mA sink current	V_{OL1}	0	—	0.4	V
Input current each I/O pin with an input voltage between 0.1 VDD and 0.9 VDD	I_i	−10	—	10	μA
Capacitance for each I/O pin	C_i	—	—	10	pF
SCL clock frequency	f_{SCL}	0	—	100	kHz
Hold time START condition	$t_{HD;STA}$	4.0	—	—	μs
Low period of SCL clock	t_{LOW}	4.7	—	—	μs
High period of SCL clock	t_{HIGH}	4.0	—	—	μs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	—	—	μs
Data hold time	$t_{HD;DAT}$	350	—	—	ns
Data set-up time	$t_{SU;DAT}$	250	—	—	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	—	—	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	—	—	μs

Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CCmax}	12	V
Input pin voltage	V_{in}	GND − 0.3 to V_{CC} + 0.3	V
Power dissipation	P_D (Note 4)	1471	mW
Power dissipation reduction rate depending on temperature	1/θja	11.8	mW/°C
Operating temperature	T_{opr}	−20~65	°C
Storage temperature	T_{stg}	−55~150	°C

Note 4: See the figure below. (the figure is based on when the IC is mounted on a board of 50 × 50 × 1.6 mm and 30% Cu area. this is the minimum board size.)

Note 5: Misoperation may be caused in the IC due to leakage from high electric fields generated by the CRT. Install the IC at least 20 cm from the CRT. If not possible, use a shield to shield electric fields.

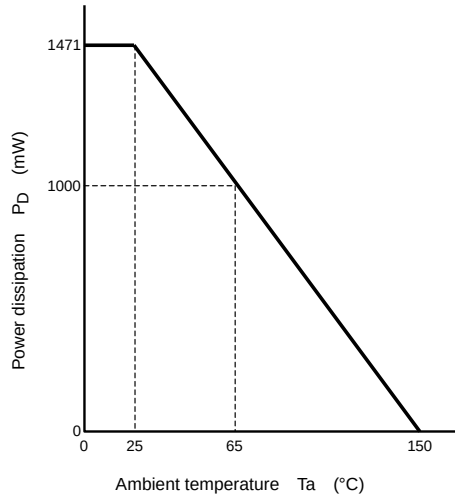


Figure Power dissipation reduction curve

Operating Conditions

Characteristic		Description		Min	Typ.	Max	Unit
Supply voltage (V_{CC})		pin 1		8.5	9.0	9.5	V
		pin 25		4.7	5.0	5.3	
Y signal input amplitude		pins 2, 4, 6, 30 including sync		—	1.0	—	V_{p-p}
Chroma signal input amplitude		pins 16, 19 burst signal amplitude		—	300	—	mV_{p-p}
Cb, Cr (Pb, Pr) signal input amplitude		pins 28, 29 100% color bar signal		—	700	—	mV_{p-p}
R, G, B signal input amplitude		pins 28, 29, 30 100% white signal		—	700	—	mV_{p-p}
HD, VD signal amplitude		pins 5, 7		1.2	5	6	V_{p-p}
HD input width	Syncronization	Pin 7, H/V FREQ = 000 to 101		0.5 μs	—	0.2 H	—
	RGB mode	Pin 7, H/V FREQ = 111		0.2	—	10	μs
	Frequency detection	Pin 7		0.2 μs	—	0.2 H (Note 6)	—
VD input width	Syncronization	Pin 5, H/V FREQ = 000 to 101		3 μs	—	31 H	—
	RGB mode	Pin 5, H/V FREQ = 111		3 μs	—	1.45 ms	—
	Frequency detection	Pin 5		3	—	400	μs
HD input frequency		Pin 7, H/V FREQ = 111		5.7	—	120	kHz
VD input frequency		Pin 5, H/V FREQ = 111		47	—	688	Hz
SYNC OUT input current		Pin 3		—	—	1.6	mA
Address switching voltage		Pin 12	DE/DF_H	8.25	9	9	V
			DC/DD_H	5.25	6	6.75	
			DA/DB_H	2.25	3	3.75	
			$D8/D9_H$	0	0	0.75	
SCL/SDA pull-up voltage		Pin 13,14		2.5	5	7.5	V
SDA input current		Pin 13		—	—	2	mA

Note 6: The ratio of H-cycle for HD input for frequency detection.

Electrical Characteristics
(unless otherwise specified, V_{CC1} = 9 V, V_{CC2} = 5 V, Ta = 25°C ± 3°C, bus data: preset values)

Current Dissipation

Pin Name	Symbol	Test Circuit	Min	Typ.	Max	Unit
V_{CC1} (9 V)	I_{CC1}	—	29.3	36.5	44.4	mA
V_{CC2} (5 V)	I_{CC2}	—	52.9	66.0	80.2	mA

Pin Voltage

Pin No.	Pin Name	Symbol	Test Circuit	Min	Typ.	Max	Unit
2	Y1/SYNC1 IN	V2	—	1.7	2.0	2.3	V
4	Y2/SYNC2 IN	V4	—	1.7	2.0	2.3	V
22	Cr/Pr OUT	V22	—	3.15	3.50	3.85	V
23	Cb/Pb OUT	V23	—	3.15	3.50	3.85	V
24	Y OUT	V24	—	2.85	3.20	3.55	V
28	Cr/Pr/R IN	V28	—	2.0	2.3	2.6	V
29	Cb/Pb/B IN	V29	—	2.0	2.3	2.6	V
30	YD-SYNC1/Y3/G IN	V30	—	1.7	2.0	2.3	V

Y/Cb/Cr Block

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Y input dynamic range		VDY	—	Pins 2, and 4	1.35	1.50	1.65	V_{p-p}
		VDY30	—	Pins 30	1.26	1.40	1.54	
Color difference input dynamic range		VDCb	—	Pin 28	1.0	—	—	V_{p-p}
		VDCr	—	Pin 29	1.0	—	—	
Chroma trap characteristic		GCT	—	fsc attenuation	—	—	−20	dB
Y delay time switching 1 (pre-filter block)	(00)	YDY100	—	SA07H: 80H	−17	−10	−5	ns
	(01)	YDY101	—	SA07H: 84H	−5	0	5	
	(10)	YDY110	—	SA07H: 88H	7	10	13	
	(11)	YDY111	—	SA07H: 8CH	7	10	13	
Y delay time switching 2 (TOF block)	(01)	YDL2A	—	SA07H: 81H	30	40	55	ns
	(10)	YDL2B	—	SA07H: 82H	70	80	110	
	(11)	YDL2C	—	SA07H: 83H	100	120	160	
I/O gain 1 (YCbCr → YCbCr)	Y	GMYC	—	SA03H: 80H, Between pins 30 and 24	−1.00	0.00	1.00	dB
	Cb	GMBC	—	SA03H: 80H, Between pins 29 and 23	−1.00	0.00	1.00	
	Cr	GMRC	—	SA03H: 80H, Between pins 28 and 22	−1.00	0.00	1.00	
I/O gain 2 (YPbPr → YCbCr)	Y	GMYC1	—	(Note Y1)	−1.00	0.00	1.00	dB
	B → Y	GMBC1	—		−21.4	−19.9	−18.4	
	B → B	GMBC2	—		−1.1	−0.1	0.9	
	B → R	GMBC3	—		−25.5	−24.0	−22.5	
	R → Y	GMRC1	—		−14.1	−13.1	−12.1	
	R → B	GMRC2	—		−21.1	−19.1	−17.6	
	R → R	GMRC3	—		−1.2	−0.2	0.9	
I/O gain 3 (YCbCr → YPbPr)	Y	GMYP1	—	(Note Y2)	−1.00	0.00	1.00	dB
	B → Y	GMBP1	—		−20.0	−18.5	−17.0	
	B → B	GMBP2	—		−0.8	0.2	1.2	
	B → R	GMBP3	—		−24.5	−22.5	−20.5	
	R → Y	GMRP1	—		−14.4	−13.4	−12.4	
	R → B	GMRP2	—		−20.8	−18.8	−17.3	
	R → R	GMRP3	—		−0.8	0.22	1.2	
I/O gain 4 (YPbPr → YPbPr)	Y	GMYP	—	SA03H: E0H, Between pins 30 and 24	−1.00	0.00	1.00	dB
	Pb	GMBP	—	SA03H: E0H, Between pins 29 and 23	−1.00	0.00	1.00	
	Pr	GMRP	—	SA03H: E0H, Between pins 28 and 22	−1.00	0.00	1.00	
I/O gain 5 (RGB → YCbCr)	G → Y	GMGA1	—	(Note Y3)	−5.0	−4.0	−3.0	dB
	G → B	GMGA2	—		−10.6	−9.6	−8.6	
	G → R	GMGA3	—		−8.6	−7.6	−6.6	
	B → Y	GMBA1	—		−20.4	−18.9	−17.4	
	B → B	GMBA2	—		−7.0	−6.0	−5.0	
	B → R	GMBA3	—		−25.0	−23.0	−21.0	
	R → Y	GMRA1	—		−10.5	−9.5	−8.5	
	R → B	GMRA2	—		−16.5	−15.5	−14.5	
	R → R	GMRA3	—		−7.0	−6.0	−5.0	

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
I/O gain 6 (RGB → YPbPr)	G → Y	GMGB1	—	(Note Y4)	−3.1	−2.1	−1.1	dB
	G → B	GMGB2	—		−9.3	−8.3	−7.3	
	G → R	GMGB3	—		−7.9	−6.9	−5.9	
	B → Y	GMBB1	—		−22.8	−21.8	−20.8	
	B → B	GMBB2	—		−7.0	−6.0	−5.0	
	B → R	GMBB3	—		−29.0	−27.0	−25.0	
	R → Y	GMRB1	—		−13.5	−12.5	−11.5	
	R → B	GMRB2	—		−21.0	−19.0	−17.0	
	R → R	GMRB3	—		−7.0	−6.0	−5.0	
Pre-filter 1 (Y axis)	Filter 1	GFY1	—	SA03H: 88H, at 11.3 MHz	−8	−4	−1	dB
		GFY2	—	SA03H: 88H, at 16 MHz	−30	−18	−9	
	Filter 2	GFY3	—	SA03H: 90H, at 16 MHz	−11	−4	−1	
		GFY4	—	SA03H: 80H, at 27 MHz	−34	−26	−18	
Pre-filter 2 (B-Y, R-Y axes)	Filter 1	GFBR1	—	SA03H: 88H, at 5.65 MHz	−8	−5	−2	dB
		GFBR2	—	SA03H: 88H, at 16 MHz	−42	−35	−28	
	Filter 2	GFBR3	—	SA03H: 90H, at 8 MHz	−8	−5	−2	
		GFBR4	—	SA03H: 90H, at 27 MHz	−48	−35	−26	
Y black-level range	Positive	YBMAX	—	SA08H: FFH, pin 24	126	140	154	mV
	Negative	YBMIN	—	SA08H: 01H, pin 24	−154	−140	−126	
R-Y, B-Y black-level range	Positive	RBBMAX	—	SA09H/10H: FFH, pin 23/22	126	140	154	mV
	Negative	RBBMIN	—	SA09H/10H: 01H, pin 23/22	−154	−140	−126	
Output gain switching		GGSW	—	SA04H: 00H/80H	5	6	7	dB
Y I/O gain (Y1/Y2 IN)		GY	—	Between pins 2/4 and 24	−1.0	0	1.0	dB
Sub contrast characteristic	max	GSCMAX	—	SA05H: F8H/80H	2.0	3.0	4.0	dB
	min	GSCMIN	—	SA05H: 80H/00H	−4.0	−3.0	−2.0	
Sub color characteristic	max	GCLMAX	—	SA06H: F8H/80H	2.0	3.0	4.0	dB
	min	GCLMIN	—	SA06H: 80H/00H	−4.0	−3.0	−2.0	
Input crosstalk		GCLT	—	—	−35	−50	—	dB
Tint characteristic	max	TNTMAX	—	SA07H: F0H/80H	6.0	7.0	8.0	°
	min	TNTMIN	—	SA70H: 80H/00H	−8.0	−7.0	−6.0	
Frequency characteristic	Y1/Y2	GY1IN	—	at 13 MHz, Input; pins 2 and 4	−2	0	2	dB
	Y3	GY3IN	—	at 40 MHz, Input; pin 30	−2	0	2	
	Cb/Cr	GBRIN	—	at 40 MHz, Input; pins 28 and 29	−2	0	2	

Chroma Block

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
ACC characteristic		F601	—	(Note CH1)	280	330	380	mV_{p-p}
		F301	—		280	330	380	
		F31	—		270	320	370	
		F11	—		115	130	145	
		A1	—		0.85	1.00	1.15	—
Color difference output level	B	VBO	—	100% color bar	600	720	840	mV_{p-p}
	R	VRO	—		600	705	840	
Color difference output relative amplitude		RRB	—	100% color bar, Cb/Cr	0.93	1	1.15	—
Demodulation angle	B	θB	—	—	−3	0	3	°
	R	θR	—	—	87	90	93	
Color difference output relative phase		θBR	—	—	86	90	93	°
Identification sensitivity	Killer OFF	VCI	—	(Note CH2)	4.0	5.4	10.0	mV
	Killer ON	VBI	—		3.5	4.6	6.0	
Free-running frequency		f03	—	Pins 16 and 19: AC GND	3.579345	3.579545	3.579745	MHz
APC frequency control sensitivity		βf	—	(Note C3H)	0.5	1.0	1.5	Hz/mV
APC pull-in and hold ranges	Hold +	f3HH	—	Upper hold range	250	500	2000	Hz
	Pull-in +	f3PH	—	Upper pull-in range	250	500	2000	
	Hold −	f3HL	—	Lower hold range	−2000	−500	−250	
	Pull-in −	f3PL	—	Lower pull-in range	−2000	−500	−250	
CW output amplitude		Vfsc	—	Pin 26	400	600	720	mV_{p-p}
CW output DC level	High	V26H	—	Pin 26 at NTSC input	2.7	3.0	3.3	V
	Low	V26L	—	Pin 26 at quiescent	1.0	1.3	1.6	
Residual carrier wave level		VNE	—	Pins 22 and 23, fsc leakage level, when rainbow signal (B = C = 300 mV_{p-p}) input	—	—	4.0	mV_{p-p}
Residual harmonic level		VHNE	—	Pins 22 and 23, 2 × fsc leakage level when rainbow signal (B = C = 300 mV_{p-p}) input	—	—	4.0	mV_{p-p}
TOF characteristic	0 kHz	GFH	—	(Note CH4)	19	21	23	dB
	+500 kHz	GFC	—		17	19	21	
	−500 kHz	GFL	—		14	16	18	
TOF (f0·Q) control characteristic	f0+	GF+	—	(Note CH5)	14	16	18	dB
	f0−	GF−	—		22.5	24.5	26.5	

Sync Block

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
SYNC IN sync phase	SYNC1/2	S_{PH}	—	(Note SY01)	2.8	3.0	3.2	μs
	D-SYNC1	DS1PH	—		0.75	0.85	0.95	
HD IN horizontal sync phase		HD_{PH}	—	(Note SY02)	0.8	0.9	1.0	μs
Delayed HD pulse width	15.73 kHz	$W_{d\text{-}HD0}$	—	(Note SY03)	3.9	4.2	4.6	μs
	31.5 kHz	$W_{d\text{-}HD1}$	—		1.4	1.6	1.8	
	33.75 kHz	$W_{d\text{-}HD2}$	—		1.3	1.5	1.7	
	45 kHz	$W_{d\text{-}HD3}$	—		1.5	1.7	1.9	
NTSC horizontal sync separation level	00	VthH10	—	(Note SY04)	0.219	0.229	0.239	$V_{p\text{-}p}$
	01	VthH11	—		0.199	0.209	0.219	
	10	VthH12	—		0.179	0.189	0.199	
	11	VthH13	—		0.162	0.169	0.179	
NTSC vertical sync separation level	00	VthV10	—	(Note SY05)	0.157	0.172	0.186	$V_{p\text{-}p}$
	01	VthV11	—		0.129	0.143	0.157	
	10	VthV12	—		0.1	0.114	0.129	
	11	VthV13	—		0.072	0.086	0.1	
1125I/60-Hz horizontal sync separation level	00	VthH20	—	(Note SY06)	0.059	0.070	0.081	$V_{p\text{-}p}$
	01	VthH21	—		0.080	0.091	0.102	
	10	VthH22	—		0.109	0.120	0.131	
	11	VthH23	—		0.135	0.146	0.157	
1125I/60-Hz vertical sync separation level	00	VthV20	—	(Note SY07)	0.059	0.070	0.081	$V_{p\text{-}p}$
	01	VthV21	—		0.080	0.091	0.102	
	10	VthV22	—		0.109	0.120	0.131	
	11	VthV23	—		0.135	0.146	0.157	
D-SYNC2 sync separation level	00	VthD20	—	(Note SY08)	0.056	0.067	0.078	$V_{p\text{-}p}$
	01	VthD21	—		0.086	0.097	0.108	
	10	VthD22	—		0.111	0.122	0.133	
	11	VthD23	—		0.134	0.145	0.156	
HD input threshold		V_{thHD}	—	Pin 7	0.6	0.7	0.8	V
Horizontal free-running frequency	15.73 kHz-1	FA000	—	(Note SY09)	15.59	15.73	15.91	kHz
	31.5 kHz	FA001	—		31.19	31.5	31.82	
	33.75 kHz-1	FA010	—		33.41	33.75	34.09	
	45 kHz	FA011	—		44.55	45	45.45	
	15.73 kHz-2	FA100	—		15.59	15.73	15.91	
	15.73 kHz-3	FA101	—		15.59	15.73	15.91	
	33.75 kHz-2	FA110	—		33.41	33.75	34.09	
	33.75 kHz-3	FA111	—		33.41	33.75	34.09	
	15.73 kHz-4	FF000	—		15.59	15.73	15.91	
Horizontal frequency range	15.73 kHz-1	F15MIN	—	(Note SY10)	14.37	14.67	14.97	kHz
		F15MAX	—		16.61	16.94	17.27	
	31.5 kHz	F31MIN	—		28.97	29.56	30.15	
		F31MAX	—		33.23	33.90	34.57	
	33.75 kHz	F33MIN	—		30.91	31.54	32.17	
		F33MAX	—		35.44	36.15	36.86	
	45 kHz	F45MIN	—		41.81	42.62	43.48	
		F45MAX	—		48.27	49.24	50.21	
	15.73 kHz-2	F15nMIN	—		14.80	15.10	15.40	
		F15nMAX	—		16.06	16.36	16.66	

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Horizontal oscillation control sensitivity	15.73 kHz	BH1573	—	Pin 9 voltage vs horizontal oscillation frequency	2.7	3.4	4.1	kHz/V
	31.5 kHz	BH315	—		5.4	6.7	8.0	
	33.75 kHz	BH3375	—		5.6	7.0	8.4	
	45 kHz	BH45	—		7.9	9.7	11.5	
AFC phase detection current	0dB	ID1+	—	(Note SY11)	256	320	400	μA
		ID1–	—		256	320	400	
	–6dB	ID2+	—		56	70	87.5	
		ID2–	—		56	70	87.5	
	–12dB	ID3+	—		536	670	838	
		ID3–	—		536	670	838	
VCO oscillation start voltage		V_{VCO}	—	Pin 1 (V_{CC1})	4.0	4.6	4.9	V
AFC phase detection stop period	Start	TVMASK1	—	NTSC signal, MONITOR OUT (pin 9)	—	1	—	H
	Stop	TVMASK2	—		—	10	—	
HD output phase and width	15.73 kHz Ph	HDS0	—	(Note SY12)	–1.0	–0.8	–0.6	μs
	15.73 kHz W	HDW0	—		4.3	4.5	4.7	
	31.5 kHz Ph	HDS1	—		–0.06	0.04	0.14	
	31.5 kHz W	HDW1	—		2.05	2.25	2.45	
	33.75 kHz Ph	HDS2	—		–0.12	–0.02	0.08	
	33.75 kHz W	HDW2	—		1.9	2.1	2.3	
	45 kHz Ph	HDS3	—		–0.07	0.03	0.13	
	45 kHz W	HDW3	—		1.4	1.6	1.8	
	D5 mode Ph	HDS4	—		0.13	0.23	0.33	
	D5 mode W	HDW4	—		1.9	2.1	2.3	
	RGB mode Ph	HDS5	—		0	0.1	0.2	
	RGB mode W	HDW5	—		2.23	2.35	2.47	
HD output level	High	HDVH	—	Pin 17: High voltage	4.9	5.1	5.3	V
	Low	HDVL	—	Pin 17: Low voltage	0	0.1	0.3	V
HD output phase adjustment range	15.73 kHz	ΔHP0–	—	(Note SY13)	1.31	1.45	1.6	μs
		ΔHP0+	—		1.17	1.30	1.43	
	31.5 kHz	ΔHP1–	—		0.67	0.74	0.81	
		ΔHP1+	—		0.59	0.65	0.72	
	33.75 kHz	ΔHP2–	—		0.64	0.71	0.78	
		ΔHP2+	—		0.54	0.60	0.66	
	45 kHz	ΔHP3–	—		0.46	0.51	0.56	
		ΔHP3+	—		0.41	0.45	0.50	
HD input polarity detection range	(–) → (+)	$HD\text{-}_{DUTY1}$	—	pin 7: HD input pin 17: Monitor	40	45	50	%
	(+) → (–)	$HD\text{-}_{DUTY2}$	—		45	50	55	

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Clamp pulse phase and width	15.73 kHz	CP_{S0}	—	(Note SY14)	6.15	6.35	6.55	μs
		CP_{W0}	—		1.8	2	2.2	
	31.5 kHz	CP_{S1}	—		2.85	2.95	3.05	
		CP_{W1}	—		0.9	1	1.1	
	33.75 kHz	CP_{S2}	—		1.85	1.95	2.05	
		CP_{W2}	—		0.9	1.0	1.1	
	45 kHz	CP_{S3}	—		1.95	2.05	2.15	
		CP_{W3}	—		0.9	1.0	1.1	
	D5 mode	CP_{S4}	—		0.75	0.85	0.95	
		CP_{W4}	—		0.4	0.5	0.6	
	RGB mode	CP_{S5}	—		0.05	0.15	0.25	
		CP_{W5}	—		2.23	2.35	2.47	
Clamp pulse output level	High	CPVH	—	pin 8, SA 02H: 86H	4.7	5.0	5.3	V
	Low	CPVL	—		0	0.1	0.3	
Noise detection	00; 1 → 0	NHi00	—	(Note SY15)	37	50	63	mV_{p-p}
	01; 1 → 0	NHi01	—		26	35	44	
	10; 1 → 0	NHi10	—		20	27	34	
	11; 1 → 0	NHi11	—		17	23	29	
	00; 0 → 1	NLow00	—		17	23	29	
	01; 0 → 1	NLow01	—		13	18	23	
	10; 0 → 1	NLow10	—		9	14	19	
	11; 0 → 1	NLow11	—		8	12	16	
DAC output voltage	High	VDACH1	—	Pin 8, SA02H: 80H	4.8	5	5.2	V
	Low	VDACL0	—	Pin 8, SA02H: 81H	0	0.1	0.3	
VD input threshold		VthVD	—	Pin 5	0.6	0.75	0.9	V
VD output width	525I-1	VDW000	—	(Note SY16)	451	513	575	μs
	525P	VDW001	—		237	270	302	
	1125I	VDW010	—		222	252	282	
	750P	VDW011	—		451	513	575	
	525I-2	VDW100	—		455	517	579	
	525I-3	VDW101	—		222	252	282	
	1125P	VDW110	—		222	252	282	
VD output phase	525I-1	VDPh000	—		14.4	17.5	20.1	μs
	525P	VDPh001	—		6.65	7.85	9.05	
	1125I	VDPh010	—		6.15	7.25	8.35	
	750P	VDPh011	—		4.85	5.72	6.6	
	525I-1b	VDPh000b	—		12	14	16	
VD output level	High	VDVH	—	Pin 15: High voltage	4.7	5.0	5.3	V
	Low	VDVL	—	Pin 15: Low voltage	0	0.1	0.3	

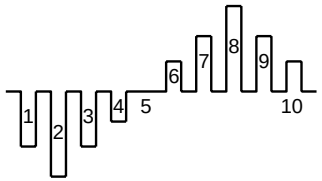
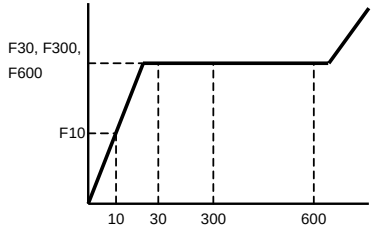
Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Vertical free-running frequency	525I-1	FVF000	—	Pin 15: Quiescent, SA00H: E0H	—	262.5	—	H
	525P	FVF001	—	Pin 15: Quiescent, SA00H: E2H	—	525	—	
	1125I	FVF010	—	Pin 15: Quiescent, SA00H: E4H	—	562.5	—	
	750P	FVF011	—	Pin 15: Quiescent, SA00H: E6H	—	750	—	
	525I-2	FVF100	—	Pin 15: Quiescent, SA00H: E8H	—	262.5	—	
	525I-3	FVF101	—	Pin 15: Quiescent, SA00H: EAH	—	296.5	—	
	1125P	FVF110	—	Pin 15: Quiescent, SA00H: ECH	—	562.5	—	
	RGB	FVF111	—	Pin 15: Quiescent, SA00H: EEH	—	562.5	—	
Vertical pull-in range	525I-1	FVP000	—	Pin 15, SA00H: 80H	224	—	296.5	H
	525P	FVP001	—	Pin 15, SA00H: 82H	48.5	—	612	
	1125I	FVP010	—	Pin 15, SA00H: 84H	48.5	—	636	
	750P	FVP011	—	Pin 15, SA00H: 86H	48.5	—	848	
	525I-2	FVP100	—	Pin 15, SA00H: 88H	—	262.5	—	
	525I-3	FVP101	—	Pin 15, SA00H: 8AH	32	—	296.5	
	1125P	FVP110	—	Pin 15, SA00H: 8CH	48.5	—	636	
	RGB	FVP111	—	Pin 15, SA00H: EEH	48.5	—	740	

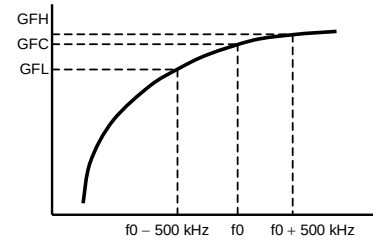
Test Method (unless otherwise specified, V_{CC1} = 9 V, V_{CC2} = 5 V, Ta = 25°C ± 3°C, bus data: preset values)

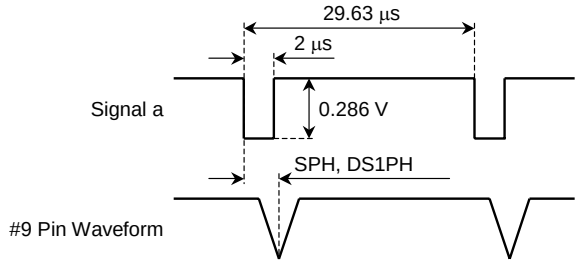
Note No.	Characteristic	SW Mode			Test Method
		SW28	SW29	SW30	
Y/back end block					Y/back end block common test conditions (1) Write data: Transmit PREST DATA. Read data: Read DATA. (2) Set SA 08H/09H/10H to 00H/00H/00H. (3) Set SW2 to A, SW4 to A, SW6 to B, SW9 to On, SW12 to A, SW16 to A, SW19 to A, SW22 to B, SW23 to B, and SW24 to B.
Y1	I/O gain 2 (YPbPr → YCbCr)	C ↓ A	C ↓ A ↓ C	A	(1) Set INPUT SW (SA 00H) to D-SYNC1/Y3/CbCr (PbPr) (C0H). (2) Set MATRIX SW (SA 03H) to MODE-2 (A0H). (3) Input sine wave A (f = 100 kHz) to IN30 and set #30 amplitude to 0.2 V_{p-p}. (4) Measure #24 amplitude VMYC [V] and determine GMYC using the following equation. GMYC = 20 × log (VMYC/0.2) [dB] (5) Set SW29 to A, input sine wave B (f = 100 kHz) to IN29, and set #29 amplitude to 0.2 V_{p-p}. (6) Input sync signal to IN30. (7) Measure #24, #23, #22 amplitudes VMBC1, VMBC2, and VMBC3 [V], and determine GMBC1, GMBC2, and GMBC3 using the following equation. GMBC* = 20 × log (VMBC*/0.2) [dB] (8) Set SW28 to A and SW29 to C, input sine wave B (f = 100 kHz), and set #28 amplitude to 0.2 V_{p-p}. (9) Input sync signal to IN30. (10) Measure #24, #23, #22 amplitudes VMRC1, VMRC2, and VMRC3 [V], and determine GMRC1, GMRC2, and GMRC3 using the following equation. GMRC* = 20 × log (VMRC*/0.2) [dB]

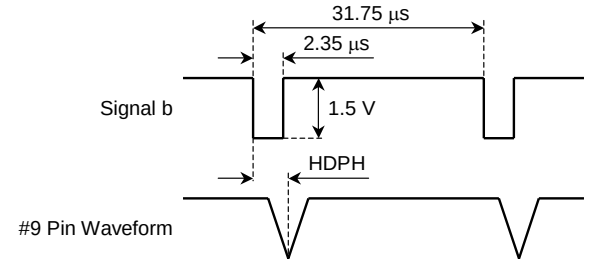
Note No.	Characteristic	SW Mode			Test Method
		SW28	SW29	SW30	
Y2	I/O gain 3 (YCbCr → YPbPr)	C ↓ A	C ↓ A ↓ C	A	(1) Set INPUT SW (SA 00H) to D-SYNC1/Y3/CbCr (PbPr) (C0H). (2) Set MATRIX SW (SA 03H) to MODE-3 (C0H). (3) Input sine wave A (f = 100 kHz) to IN30 and set #30 amplitude to 0.2 V_{p-p}. (4) Measure #24 amplitude VMYP [V] and determine GMYP using the following equation. GMYP = 20 × log (VMYP/0.2) [dB] (5) Set SW29 to A, input sine wave B (f = 100 kHz) to IN29, and set #29 amplitude to 0.2 V_{p-p}. (6) Input sync signal to IN30. (7) Measure #24, #23, #22 amplitudes VMBP1, VMBP2, and VMBP3 [V], and determine GMBP1, GMBP2, and GMBP3 using the following equation. GMBP* = 20 × log (VMBP*/0.2) [dB] (8) Set SW28 to A and SW29 to C, input sine wave B (f = 100 kHz) to IN28, and set #28 amplitude to 0.2 V_{p-p}. (9) Input sync signal to IN30. (10) Measure #24, #23, #22 amplitudes VMRP1, VMRP2, and VMRP3 [V], and determine GMRP1, GMRP2, and GMRP3 using the following equation. GMRP* = 20 × log (VMRP*/0.2) [dB]
Y3	I/O gain 5 (RGB → YCbCr)	C ↓ A	C ↓ A ↓ C	A	(1) Set INPUT SW (SA 00H) to DSYNC1/RGB (D0H). (2) Set MATRIX SW (SA 03H) to MODE-1 (80H). (3) Input sine wave A (f = 100 kHz) to IN30 and set #30 amplitude to 0.2 V_{p-p}. (4) Measure #24, #23, #22 amplitudes VMGA1, VMGA2, and VMGA3 [V], and determine GMGA1, GMGA2, and GMGA3 using the following equation. GMGA* = 20 × log (VMGA*/0.2) [dB] (5) Set SW29 to A, input sine wave B (f = 100 kHz) to IN29, and set #29 amplitude to 0.2 V_{p-p}. (6) Input sync signal to IN30. (7) Measure #24, #23, #22 amplitudes VMBA1, VMBA2, and VMBA3 [V], and determine GMBA1, GMBA2, and GMBA3 using the following equation. GMBA* = 20 × log (VMBA*/0.2) [dB] (8) Set SW28 to A and SW29 to C, input sine wave B (f = 100 kHz) to IN28, and set #28 amplitude to 0.2 V_{p-p}. (9) Input sync signal to IN30. (10) Measure #24, #23, #22 amplitudes VMRA1, VMRA2, and VMRA3 [V], and determine GMRA1, GMRA2, and GMRA3 using the following equation. GMRA* = 20 × log (VMRA*/0.2) [dB]

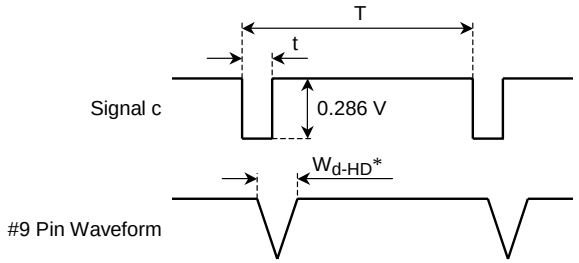
Note No.	Characteristic	SW Mode			Test Method
		SW28	SW29	SW30	
Y4	I/O gain 6 (RGB → YPbPr)	C ↓ A	C ↓ A ↓ C	A	(1) Set INPUT SW (SA 00H) to DSYNC1/RGB (D0H). (2) Set MATRIX SW (SA 03H) to MODE-4 (E0H). (3) Input sine wave A (f = 100 kHz) to IN30 and set #30 amplitude to 0.2 V_{p-p}. (4) Measure #24, #23, #22 amplitudes VMGB1, VMGB2, and VMGB3 [V], and determine GMGB1, GMGB2, and GMGB3 using the following equation. GMGB* = 20 × log (VMGB*/0.2) [dB] (5) Set SW29 to A, input sine wave B (f = 100 kHz) to IN29, and set #29 amplitude to 0.2 V_{p-p}. (6) Input sync signal to IN30. (7) Measure #24, #23, #22 amplitudes VMBB1, VMBB2, and VMBB3 [V], and determine GMBB1, GMBB2, and GMBB3 using the following equation. GMBB* = 20 × log (VMBB*/0.2) [dB] (8) Set SW28 to A and SW29 to C, input sine wave B (f = 100 kHz), and set #28 amplitude to 0.2 V_{p-p}. (9) Input sync signal to IN30. (10) Measure #24, #23, #22 amplitudes VMRB1, VMRB2, and VMRB3 [V], and determine GMRB1, GMRB2, and GMRB3 using the following equation. GMRB* = 20 × log (VMRB*/0.2) [dB]

Note No.	Characteristic	SW Mode		Test Method
		SW2	SW30	
Chroma block				Chroma block common test conditions (1) Write data: Transmit PREST DATA. Read data: Read DATA. (2) Set SW2 to B, SW4 to C, SW6 to B, SW9 to On, SW12 to A, SW16 to A, SW19 to A, SW22 to B, SW23 to B, and SW24 to B, SW28 to C, SW29 to C, and SW30 to C. Input sync signal (15.734 kHz) to TP2.
CH1	ACC characteristic	B	C	(1) Input rainbow signal to the C1 IN pin (burst: chroma = 1:1). (2) Adjust burst phase so that the lower extremity of the TP23A (Cb/Pb OUT) output waveform is at the second bar; the upper extremity, at the 7th bar. (3) Change the chroma input signal amplitudes to 10, 30, 300, and 600 mV_{p-p} and measure the TP23A (Cb/Pb OUT) output amplitudes F11, F31, F301, and F601. (4) Determine A2 = F31/F601 according to the measurement result in (3) above.  TA23A (Cb/Pb OUT) output signal waveform TA23A output signal waveform  C1 IN signal amplitude [mV_{p-p}]
CH2	Identification sensitivity	B	C	(1) Input rainbow signal to the C1 IN pin (burst: chroma = 1:1). (2) Monitor TP26 (CW OUT) DC voltage. (3) Increase input signal amplitude from 0. When TP26 (CW OUT) DC voltage reaches High (3.2 V), measure input signal amplitude VCI. (4) Decrease input signal amplitude from 100 mV_{p-p}. When TP26 (CW OUT) DC voltage drops Low (1.4 V), measure input signal amplitude VBI.
CH3	APC frequency control sensitivity	C	C	(1) Connect #20 (APC FILTER) to external power supply (V20). (2) Change external power supply (V20) voltage. When #26 (CW OUT) output frequency matches 3.579545 MHz, voltage is referred to as Vf. (3) Measure #26 (CW OUT) output frequency Xf (+100) and Xf (−100) in relation to Vf ± ΔVf (±100 mV_{p-p}). Determine free-running sensitivity βf using the following equation. $\beta f = (Xf(+100) - Xf(-100))/200$ [Hz/mV]

Note No.	Characteristic	SW Mode		Test Method
		SW2	SW30	
CH4	TOF characteristic	B	C	(1) Input sine wave C (10 mV_{p-p}) to C1 IN pin. (2) Set TEST (SA 03H) to 82H and TINT (SA 07H) to 30H. (3) Set TOF f0 (SA 05H) to 87H (f0 max) and TOF Q (SA 06H) to 87H (Q max). (4) Set sine wave C frequency to 3.58 MHz, measure TP26 (CW OUT) signal amplitude, and determine input gain GFC. (5) Set sine wave C frequency to 3.58 MHz + 500 kHz, measure TP26 (CW OUT) signal amplitude, and determine input gain GFH. (6) Set sine wave C frequency to 3.58 MHz − 500 kHz, measure TP26 (CW OUT) signal amplitude, and determine input gain GFL. TP output signal waveform  C IN input frequency
CH5	TOF (f0·q) control characteristic	B	C	(1) Input sine wave C (f0 = 3.579545 MHz, amplitude = 10 mV_{p-p}) to C1 IN pin. (2) Set TEST (SA 03H) to 82H and TINT (SA 07H) to 30H. (3) Set TOF f0 (SA 05H) to 87H (f0 = max) and TOF Q (SA 06H) to 80H (Q min), measure CW OUT (TP26) signal amplitude, and determine input gain GFF. (4) Set TOF f0 (SA 05H) to 81H (f0 = min) and TOF Q (SA 06H) to 87H (max). (5) Measure CW OUT (TP26) signal amplitude, and determine input gain GFQ.

Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
Sync block						Sync block common test conditions (1) Write data: Transmit PREST DATA. Read data: Read DATA. (2) Set SW6 to B, SW12 to A, SW16 to B, SW19 to B, SW22 to B, SW23 to B, and SW24 to B, SW28 to B, and SW29 to B.
SY01	SYNC IN sync phase	A or C	A or C	ON	A or C	(1) Set SA 00H data to 80H (or 90H). (2) Set SW2 to A (or C), SW4 to C (or A), and SW30 to C. (3) Input composite video signal of 15.734-kHz horizontal frequency to Y1/SYNC1 IN (or Y2/SYNC2 IN). (4) Monitor #2 (or #4) pin waveform and #9 (AFC FILTER) pin waveform. Measure phase difference SPH. (5) Set SW2 to C, SW4 to C, and SW30 to A. (6) Input signal a to D-SYNC1/Y3 IN. (7) Set SA 00H data to C4H. (8) Monitor #30 pin waveform and #9 (AFC FILTER) pin waveform. Measure phase difference DS1PH. 

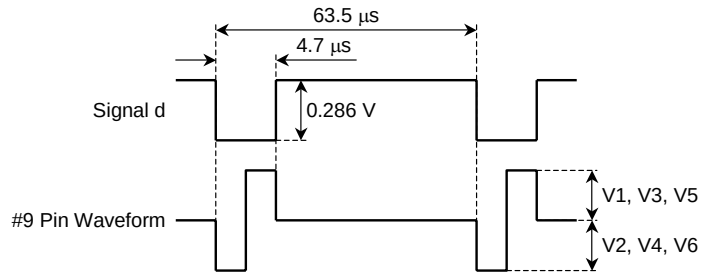
Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY02	HD IN horizontal sync phase	C	C	ON	A	(1) Set SA 00H data to E2H. (2) Input signal b (horizontal frequency 31.5 kHz) to #7 (HD IN). (3) Set SA 02H data to 02H. (4) Monitor #7 and #9 (AFC FILTER) pin waveforms. Measure phase difference HDPH. 

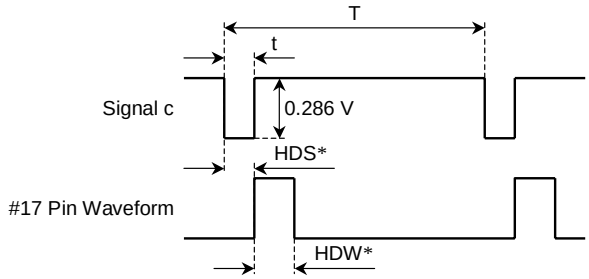
Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY03	Delayed HD pulse width	C	C	ON	A	(1) Set SA 00H data to C0H and input 15.734-kHz composite video signal to D-SYNC1/Y3 IN. (2) Determine pulse width $W_{d\text{-}HD0}$ of delayed HD from #9 (AFC FILTER) pin waveform. (3) Set SA 00H data to C2H and input signal c (T = 31.75 μs, t = 2.35 μs) to D-SYNC1/Y3 IN. (4) Determine pulse width $W_{d\text{-}HD1}$ of delay HD from #9 (AFC FILTER) pin waveform. (5) Set SA 00H data to C4H and input signal c (T = 29.63 μs, t = 2 μs) to D-SYNC1/Y3 IN. (6) Determine pulse width $W_{d\text{-}HD2}$ of delay HD from #9 (AFC FILTER) pin waveform. (7) Set SA 00H data to C6H and input signal c (T = 22.22 μs, t = 1.65 μs) to D-SYNC1/Y3 IN. (8) Determine pulse width $W_{d\text{-}HD3}$ of delay HD from #9 (AFC FILTER) pin waveform. 

Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY04	NTSC horizontal sync separation level	A	C	ON	C	(1) Set SA 00H data to 80H. (2) Input 15.734-kHz composite video signal to Y1/SYNC1 IN. Set sync signal amplitude to 0.286 V_{p-p}. (3) Decrease horizontal sync signal amplitude of line 21 of field 1 in pedestal direction. (4) Monitor #3 (SYNC OUT). When no sync signal on line 21 of field 1 is detected, measure input signal sync amplitude of line 21, and determine sync separation level VthH10. (5) Set SA 01H data to 90H. (6) Repeat steps (3) and (4) above and determine sync separation level VthH11. (7) Set SA 01H data to A0H. (8) Repeat steps (3) and (4) above and determine sync separation level VthH12. (9) Set SA 01H data to B0H. (10) Repeat steps (3) and (4) above and determine sync separation level VthH13.
SY05	NTSC vertical sync separation level	A	C	ON	C	(1) Set SA 00H data to 80H. (2) Input 15.734-kHz composite video signal to Y1/SYNC1 IN. Set sync signal amplitude to 0.286 V_{p-p}. (3) Decrease vertical sync signal amplitude of first half of line 4 of field 1 in pedestal direction. (4) Monitor #15 (VD OUT). When VD pulse start phase shifts to line 5, measure input signal sync amplitude of line 4, and determine sync separation level VthV10. (5) Set SA 01H data to 84H. (6) Repeat steps (3) and (4) above and determine sync separation level VthV11. (7) Set SA 01H data to 88H. (8) Repeat steps (3) and (4) above and determine sync separation level VthV12. (9) Set SA 01H data to 8CH. (10) Repeat steps (3) and (4) above and determine sync separation level VthV13.

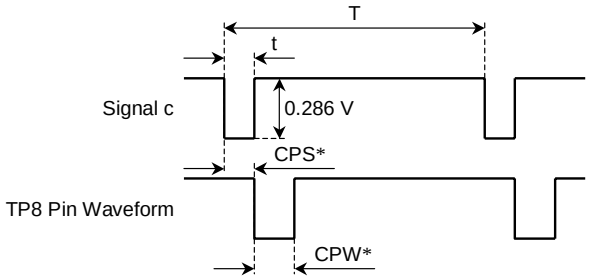
Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY06	1125I/60-Hz horizontal sync separation level	C	C	ON	A	(1) Set SA 00H data to C4H. (2) Input 33.75-kHz (1125I/60-Hz) video signal to D-SYNC1/Y3 IN. Monitor #30 (D-SYNC1/Y3 IN) and measure sync tip DC voltage Vsync30. (3) Apply external voltage to #30 via 100 kΩ. Increase voltage from Vsync30. (4) Monitor #17 (HD OUT). When phase is unlocked from input sync signal, measure #30 sync tip voltage. Determine difference from Vsync30, VthH20. (5) Set SA 01H data to 90H. (6) Repeat steps (3) and (4) above and determine sync separation level VthH21. (7) Set SA 01H data to A0H. (8) Repeat steps (3) and (4) above and determine sync separation level VthH22. (9) Set SA 01H data to B0H. (10) Repeat steps (3) and (4) above and determine sync separation level VthH23.
SY07	1125I/60-Hz vertical sync separation level	C	C	ON	A	(1) SA 00H data to C4H. (2) Input 33.75-kHz (1125I/60-Hz) video signal to D-SYNC1/Y3 IN. Monitor #30 (D-SYNC1/Y3 IN) and measure sync tip DC voltage Vsync30. (3) Apply external voltage to #30 via 100 kΩ. Increase voltage from Vsync30. (4) Monitor #17 (HD OUT). When phase is unlocked from input sync signal, measure #30 sync tip voltage. Determine difference from Vsync30, VthV20. (5) Set SA 01H data to 84H. (6) Repeat steps (3) and (4) above and determine sync separation level VthV21. (7) Set SA 01H data to 88H. (8) Repeat steps (3) and (4) above and determine sync separation level VthV22. (9) Set SA 01H data to 8CH. (10) Repeat steps (3) and (4) above and determine sync separation level VthV23.

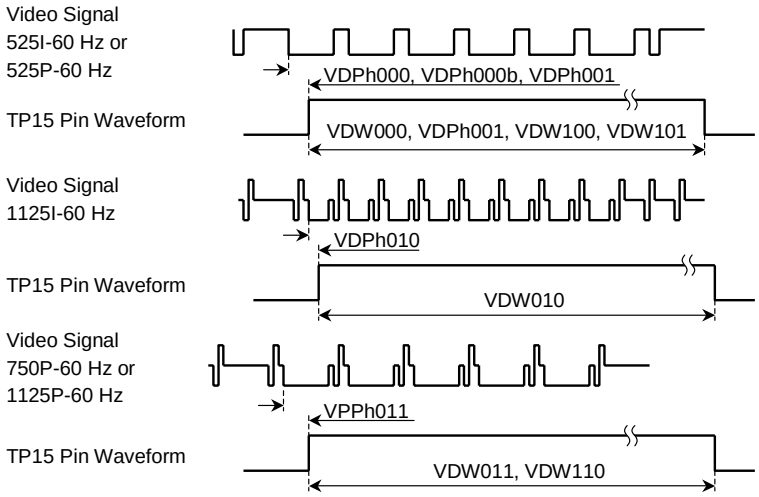
Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY08	DSYNC2 sync separation level	C	C	ON	C	(1) Set SW6 to A and set SA 00H data to 00H. (2) Input 33.75-kHz (1125I/60) video signal to TP6 (D-SYNC2 IN). (3) Monitor #6 (D-SYNC2 IN) and measure sync tip DC voltage Vsync6. (4) Apply external voltage to #30 via 100 kΩ. Increase voltage from Vsyn6. (5) Monitor READ BUS DATA. When H/V FREQ data deviate from approx. 33.75 kHz/60 Hz, measure #6 sync tip voltage. Determine difference from Vsync6, VthD20. (6) Set SA 01H data to 81H. (7) Repeat steps (3) and (4) above and determine sync separation level VthD21. (8) Set SA 01H data to 82H. (9) Repeat steps (3) and (4) above and determine sync separation level VthD22. (10) Set SA 01H data to 83H. (11) Repeat steps (3) and (4) above and determine sync separation level VthD23.
SY09	Horizontal free-running frequency	C	C	OPEN	C	(1) Set SW9 to open and SA 00H data to 80H. (2) Monitor #17 (HD OUT) pin waveform and measure oscillation frequency FA000. (3) As in steps (1) and (2) above, set SA00H data to 82H, 84H, 86H, 88H, and 8AH. Measure respective oscillation frequencies FA001, FA010, FA011, FA100, and FA101. (4) Set SA 00H data to 8CH, SA 02H to 83H, and SA 03H to 82H. (5) Monitor #17 (HD OUT) pin waveform and measure oscillation frequency FA110. (6) Set SA 00H data to 8EH, monitor #17 (HD OUT) pin waveform, and count oscillation frequency FA111. (7) Set SA 00H data to 80H, SA 02H to E0H, and SA 03H to 80H. (8) Monitor #17 (HD OUT) pin waveform and count oscillation frequency FF000.
SY10	Horizontal frequency range	C	C	OPEN	C	(1) Set SW9 to open and SA 00H data to 80H. (2) Apply 9 V to #9 via 10 kΩ. Monitor #17 (HD OUT) pin waveform and count oscillation frequency F1573MIN. (3) Apply 0 V to #9 via 10 kΩ. Monitor #17 (HD OUT) pin waveform and count oscillation frequency F1573MAX. (4) Set SA 00H data to 82H. As in steps (2) and (3) above, count oscillation frequencies F315MIN and F315MAX. (5) Set SA 00H data to 81H. As in steps (2) and (3) above, count oscillation frequencies 1573nMIN and F1573nMAX.

Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY11	AFC phase detection current	C	C	OPEN	C	(1) Set SA 00H to C0H and SA 02H to A0H. (2) Set SW9 to open and measure #9 voltage V9 (6.3 to 6.4 V) (measure #9 voltage at no load). (3) Connect external power supply (PS) to TP9 and apply V9. (4) Set SW30 to A. Input 15.734-kHz sync signal d to D-SYNC1/Y3 IN. Monitor #9. Measure voltages V1 and V2. (5) Set SA 02H data to C0H. Repeat steps (2) to (4) above. Measure voltages V3 and V4. (6) Set SA 02H data to 80H. Connect external power supply (PS) to TP9 and apply V9 − 0.1 V and measure voltage V5. (7) Connect external power supply (PS) to TP9 and apply V9 + 0.1 V and measure voltage V6. (8) Determine ID1 to ID6 using following equations. ID1+ = (V1 [V] ÷ 1 [kΩ]) × 1000 [μA] ID1− = (V2 [V] ÷ 1 [kΩ]) × 1000 [μA] ID2+ = (V3 [V] ÷ 1 [kΩ]) × 1000 [μA] ID2− = (V4 [V] ÷ 1 [kΩ]) × 1000 [μA] ID3+ = (V5 [V] ÷ 1 [kΩ]) × 1000 [μA] ID3− = (V6 [V] ÷ 1 [kΩ]) × 1000 [μA] 

Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY12	HD output phase and width	C	C	ON	A	(1) Set SA 00H data to C0H. (2) Input 15.734-kHz composite video signal to D-SYNC1/Y3 IN. (3) Measure #17 (HD OUT) and #30. Measure phase difference HDS0 and pulse width HDW0. (4) Set SA 00H data to C2H. Input signal c (T = 31.75 μs, t = 2.35 μs) and measure phase difference HDS1 and pulse width HDW1. (5) Set SA 00H data to C4H. Input signal c (T = 29.63 μs, t = 2 μs) to D-SYNC1/Y3 IN and measure phase difference HDS2 and pulse width HDW2. (6) Set SA 00H data to C6H. Input signal c (T = 24.1 μs, t = 1.65 μs) to D-SYNC1/Y3 IN and measure phase difference HDS3 and pulse width HDW3. (7) Set SA 00H data to CCH. Input signal c (T = 14.815 μs, t = 1 μs) to D-SYNC1/Y3 IN and measure phase difference HDS4 and pulse width HDW4. (8) Set SA 00H data to FEH. Input signal c (T = 31.75 μs, t = 2.35 μs, amplitude = 1.5 V) to D-SYNC1/Y3 IN and measure phase difference HDS5 and pulse width HDW5. 

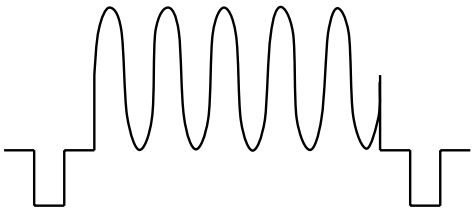
Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY13	HD output phase adjustment range	C	C	ON	C	(1) While monitoring #17 (HD OUT), change SA 04H data from 80H to 88H, and measure #17 pin waveform phase amount ΔHP0–. (2) While monitoring #17 (HD OUT), change SA 04H data from 88H to 8FH, and measure #17 pin waveform phase amount ΔHP0+. (3) Set SA 00H data to 82H. While monitoring #17 (HD OUT), change SA 04H data from 80H to 88H, and measure #17 pin waveform phase amount ΔHP1–. (4) While monitoring #17 (HD OUT), change SA 04H data from 88H to 8FH, and measure #17 pin waveform phase amount ΔHP1+. (5) Set SA 00H data to 84H. While monitoring #17 (HD OUT), change SA 04H data from 80H to 88H, and measure #17 pin waveform phase amount ΔHP2–. (6) While monitoring #17 (HD OUT), change SA 04H data from 88H to 8FH, and measure #17 pin waveform phase amount ΔHP2+. (7) Set SA 00H data to 86H. While monitoring #17 (HD OUT), change SA 04H data from 80H to 88H, and measure #17 pin waveform phase amount ΔHP3–. (8) While monitoring #17 (HD OUT), change SA 04H data from 88H to 8FH, and measure #17 pin waveform phase amount ΔHP3+.

Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY14	Clamp pulse phase and width	C	C	ON	A	(1) Set SA 00H data to C0H. Input 15.734-kHz composite video signal to D-SYNC1/Y3 IN. (2) Set SA 02H data to 86H. (3) Monitor TP8 (MONITOR OUT) and #30 pin waveforms. Measure clamp pulse phase CPS0 and width CPW0. (4) Set SA 00H data to C2H. Input signal c (T = 31.75 μs, t = 2.35 μs) to D-SYNC1/Y3 IN. (5) Monitor TP8 (MONITOR OUT) and #30 pin waveforms. Measure clamp pulse phase CPS1 and width CPW1. (6) Set SA 00H data to C4H. Input signal c (T = 29.63 μs, t = 2 μs) to D-SYNC1/Y3 IN. (7) Monitor TP8 (MONITOR OUT) and #30 pin waveforms. Measure clamp pulse phase CPS2 and width CPW2. (8) Set SA 00H data to C6H. Input signal c (T = 22.22 μs, t = 1.65 μs) to D-SYNC1/Y3 IN. (9) Monitor TP8 (MONITOR OUT) and #30 pin waveforms. Measure clamp pulse phase CPS3 and width CPW3. (10) Set SA 00H data to CCH. Input signal c (T = 14.815 μs, t = 1.15 μs) to D-SYNC1/Y3 IN. (11) Monitor TP8 (MONITOR OUT) and #30 pin waveforms. Measure clamp pulse phase CPS4 and width CPW4. (12) Set SA 00H data to FEH. Input signal c (T = 31.75 μs, t = 2.35 μs, amplitude = 1.5 V) to D-SYNC1/Y3 IN. (13) Monitor TP8 (MONITOR OUT) and #30 pin waveforms. Measure clamp pulse phase CPS5 and width CPW5. 
SY15	Noise detection	A	C	ON	C	(1) Set SA 00H data to 80H. (2) Input 500-kHz sine wave to Y1/SYNC2 IN. Increase sine wave amplitude from 0 V_{p-p}. When READ MODE 1 N-DET changes from 0 to 1, measure amplitude NHi00. (3) Input 500-kHz sine wave to Y1/SYNC2 IN. Decrease sine wave amplitude from 1.0 V_{p-p}. When READ MODE 1 N-DET changes from 1 to 0, measure amplitude NLow00. (4) As in steps (1) and (2) above, set SA 02H (NOISE LVL) data to 88H, 90H, and 98H, and measure respective amplitudes NHi01, NLow01, NHi0, NLow10, NHi11, and Nlow11.

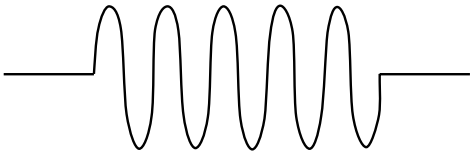
Note No.	Characteristic	SW Mode				Test Method
		SW2	SW4	SW9	SW30	
SY16	VD output width VD output phase	C	C	ON	A	(1) Set SA 00H data to C0H. Input 15.734-kHz composite video signal (525I/60-Hz) to D-SYNC1/Y3 IN. (2) Monitor #30 and TP15 (VP OUT). Measure VD output width VDW000 and phase difference VDPh000. (3) Set SA 00H data to C8H. Monitor #30 and TP15 (VP OUT). Measure VD output width VDW100. (4) Set SA 00H data to CAH. Monitor #30 and TP15 (VP OUT). Measure VD output width VDW101. (5) Set SA 00H data to C0H and SA 03H data to 84H. Monitor #30 and TP15 (VP OUT). Measure VD output phase difference VDPh000b. (6) Set SA 00H data to C2H. Input 525P/60-Hz composite video signal to D-SYNC1/Y3 IN. (7) Monitor #30 and TP15 (VP OUT). Measure VD output phase difference VDPh001 and width VDW001. (8) Set SA 00H data to C4H. Input 1125I/60-Hz composite video signal to D-SYNC1/Y3 IN. (9) Monitor #30 and TP15 (VP OUT). Measure VD output phase difference VDPh010 and width VDW010. (10) Set SA 00H data to C6H. Input 750P/60-Hz composite video signal to D-SYNC1/Y3 IN. (11) Monitor #30 and TP15 (VP OUT). Measure VD output phase difference VDPh110 and width VDW110. (12) Set SA 00H data to CCH. Input 1125P/60-Hz composite video signal to D-SYNC1/Y3 IN. (13) Monitor #30 and TP15 (VP OUT). Measure VD output width VDW110. 

Signals Used for Testing

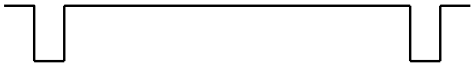
- Sine wave A



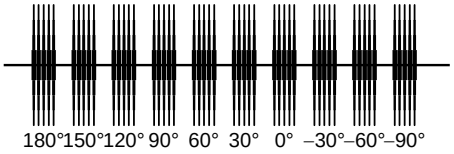
- Sine wave B



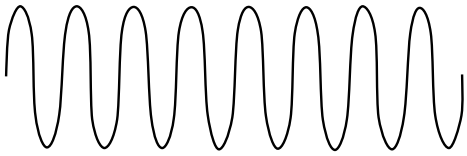
- Sync signal



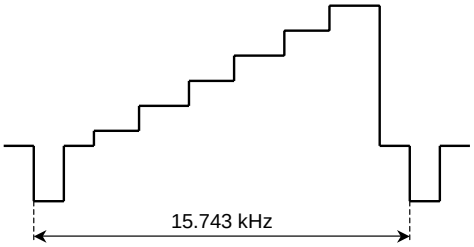
- Rainbow signal



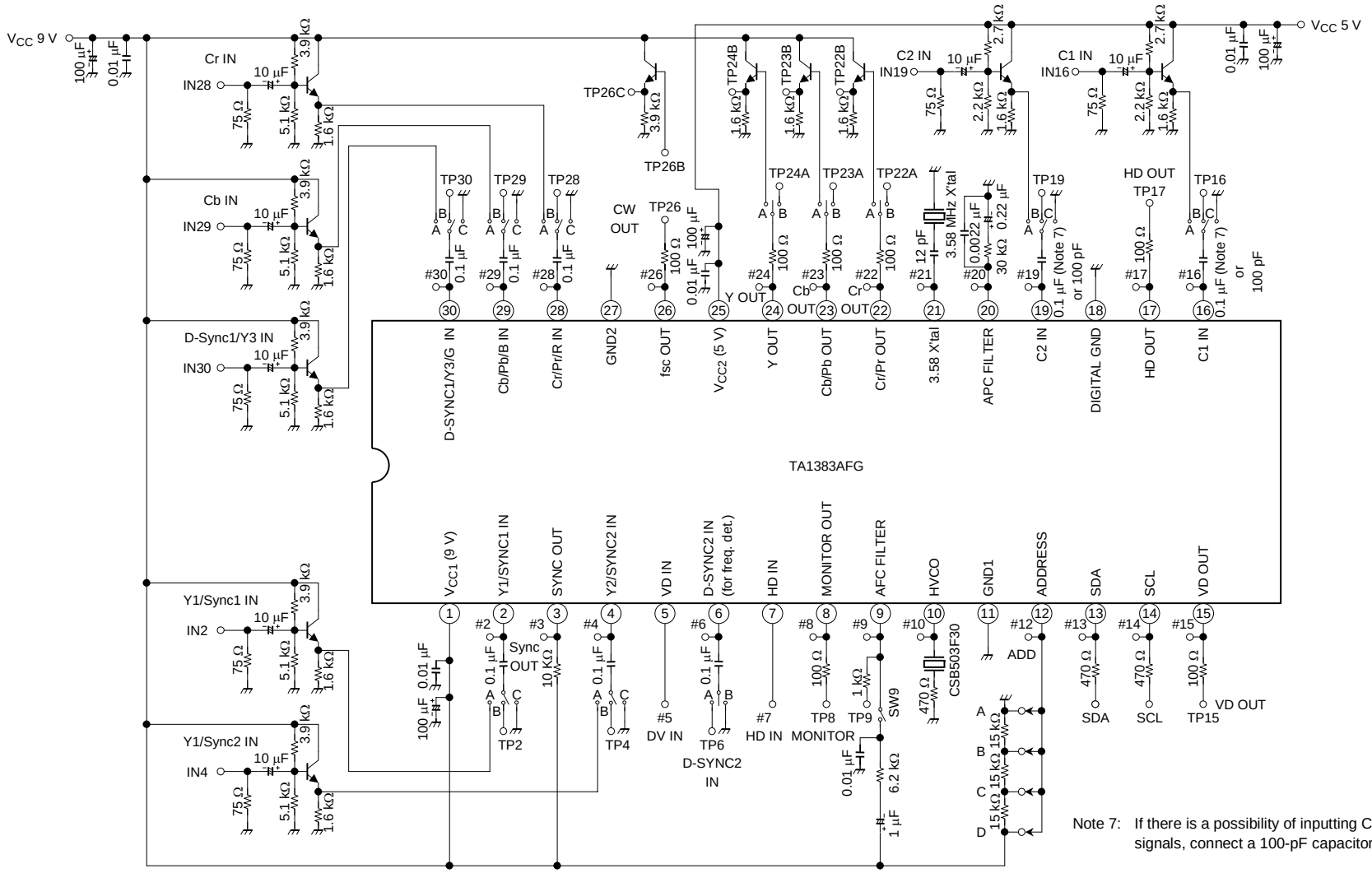
- Sine wave C



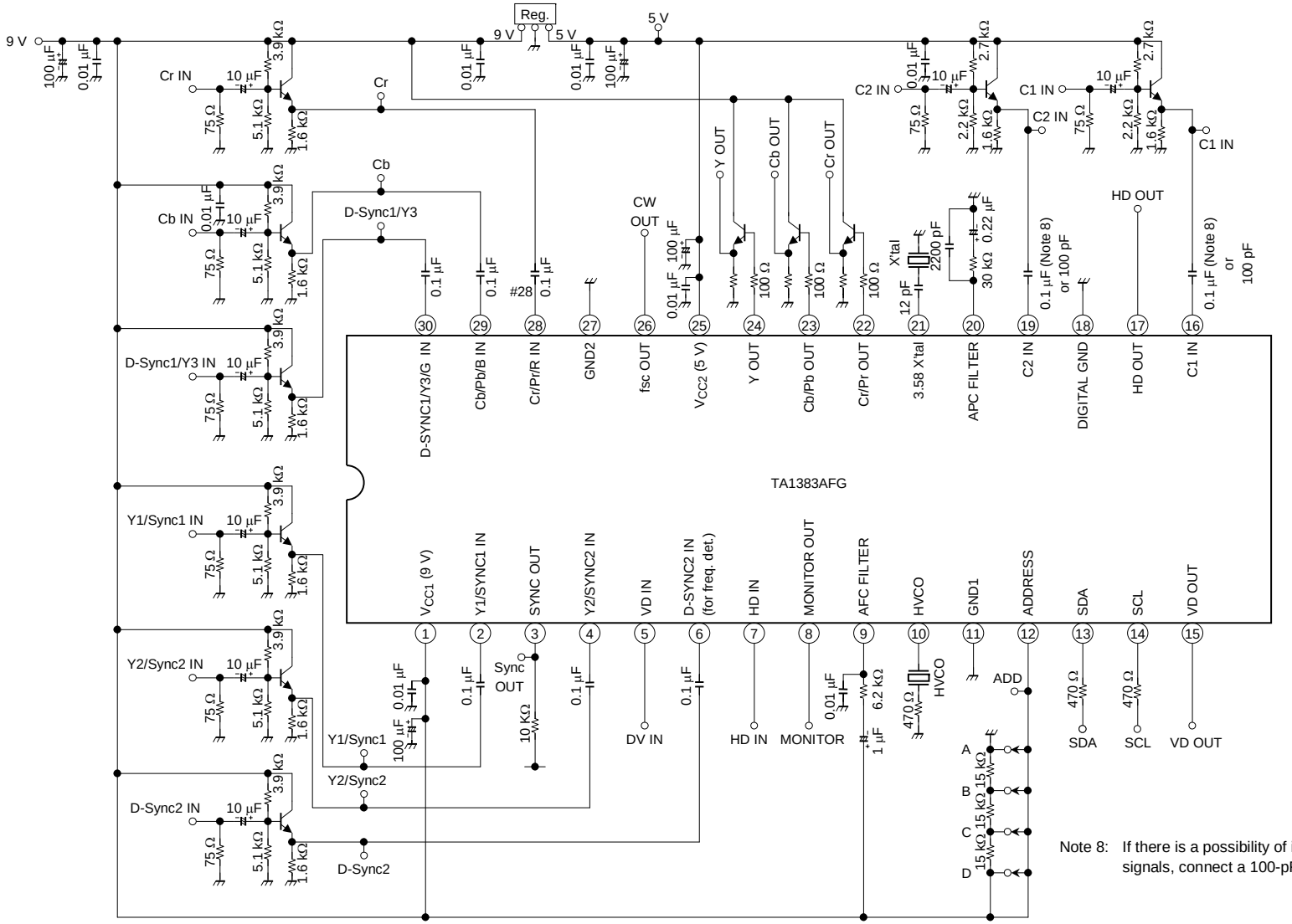
- Composite video signal



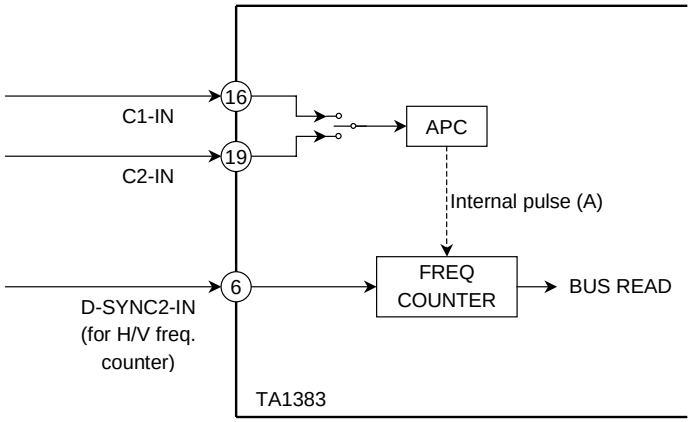
Test Circuit Diagram



Application Circuit 1 (Typical values)



Application Circuit 2 (How to measure H/V frequency)

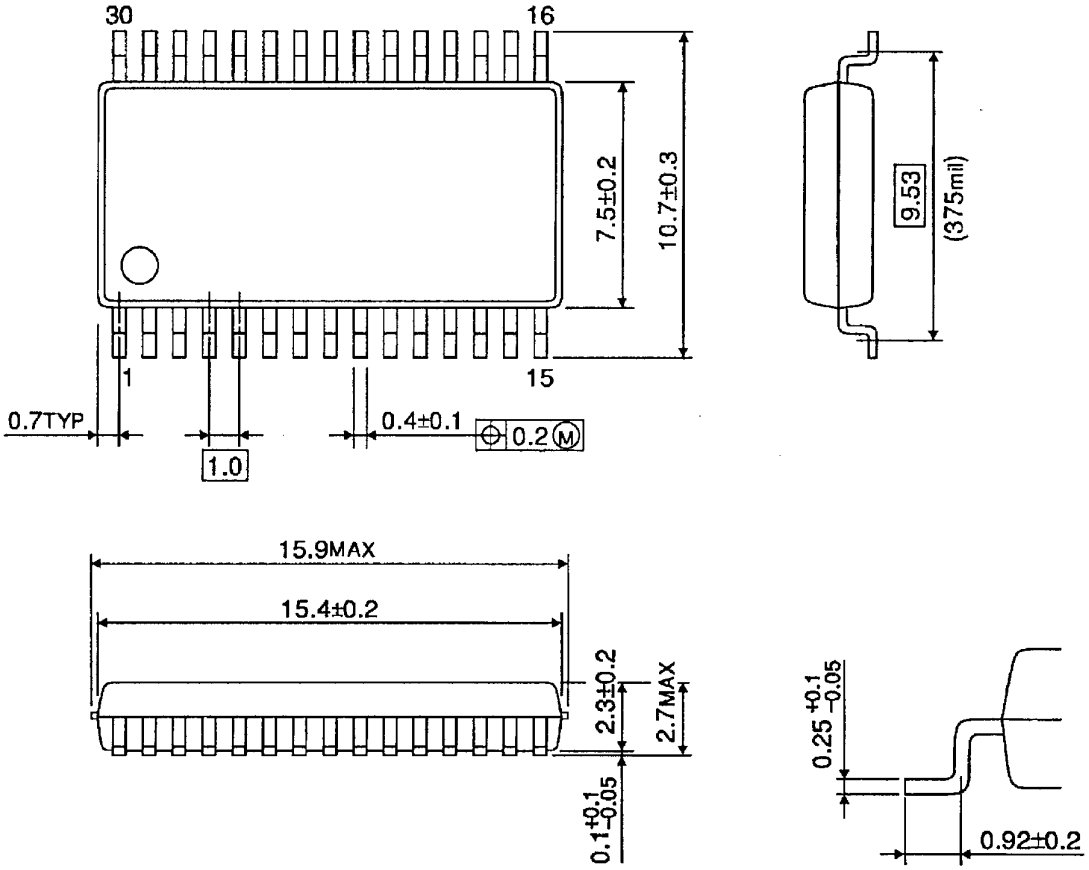


This IC's H/V frequency counting is done by internal pulse (A) which is made in APC circuit. So, if APC circuit doesn't lock in the regular frequency, the frequency of pulse (A) will not be correct and the H/V frequency data will not be showed correct data.

Decision algorithm of H/V frequency detection (detection range, detection times and so on) should be determined under consideration the factors such as signal strength, existence of ghost signal, APC stability, I^2C BUS data transmission and so on via prototype TV set evaluation.

Package Dimensions

SSOP30-P-375-1.00 Unit : mm



Weight: 0.63 g (typ.)

About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-63Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

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