TOSHIBA Transistor Silicon NPN Epitaxial Type

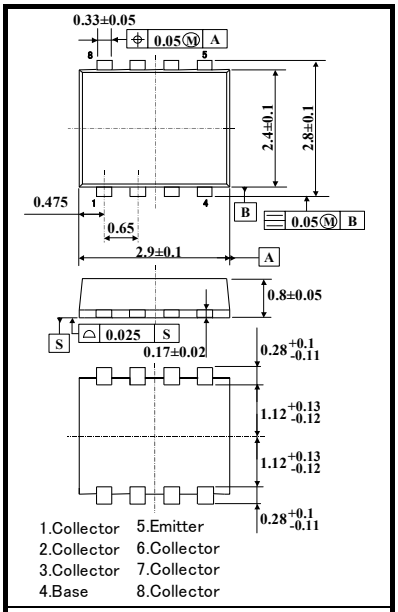
TPCP8501

Switching Applications

DC-DC Converter Applications

- High DC current gain : h_{FE} = 100 to 300 (I_C = 0.3 A)
- Low collector-emitter saturation : $V_{CE\ (sat)}$ = 0.2 V (max)
- High-speed switching : t_f = 100 ns (typ.)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-3V1A

Weight: 0.017 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Collector-base voltage		V_{CBO}	180	V
Collector-emitter voltage		V_{CEX}	150	V
		V_{CEO}	100	
Emitter-base voltage		V_{EBO}	7	V
Collector current	DC (Note 1)	I_C	2.0	A
	Pulse (Note 1)	I_{CP}	4.0	
Base current		I_B	0.2	A
Collector power dissipation (t = 10s)	t = 10s	P_C (Note 2)	3.3	W
	DC		1.3	
Junction temperature		T_j	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note 1: Please use devices on condition that the junction temperature is below 150°C.

Note 2: Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 mm^2)

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Figure 1. Circuit configuration (top view)

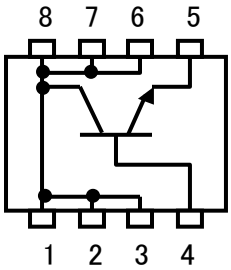
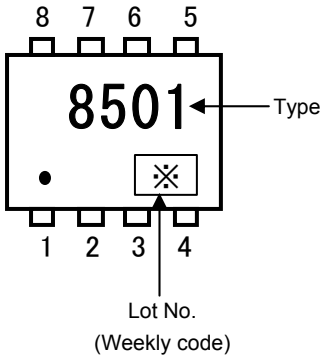
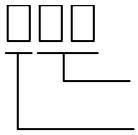


Figure 2. Marking (Note 4)



Note 4: ● on lower left on the marking indicates Pin 1.

※ Weekly code: (Three digits)



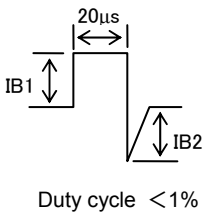
Week of manufacture
(01 for first week of year, continues up to 52 or 53)

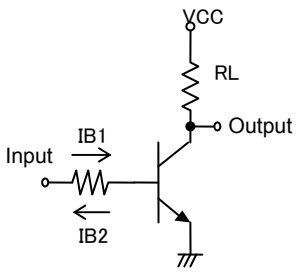
Year of manufacture
(One low-order digits of calendar year)

Electrical Characteristics (Ta = 25°C)

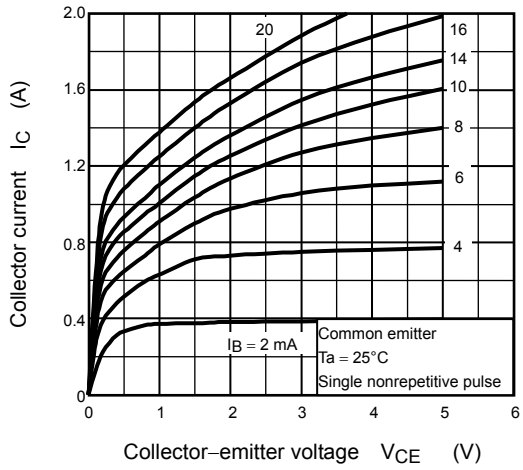
Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Collector cut-off current		I_{CBO}	V_{CB} = 180 V, I_E = 0	—	—	100	nA
Emitter cut-off current		I_{EBO}	V_{EB} = 7 V, I_C = 0	—	—	100	nA
Collector-base breakdown voltage		$V_{(BR)\ CBO}$	I_C = 1 mA, I_B = 0	180	—	—	V
Collector-emitter breakdown voltage		$V_{(BR)\ CEO}$	I_C = 10 mA, I_B = 0	100	—	—	V
DC current gain		h_{FE} (1)	V_{CE} = 2 V, I_C = 0.3 A	100	—	300	
		h_{FE} (2)	V_{CE} = 2 V, I_C = 1.0 A	80	—	—	
Collector-emitter saturation voltage		$V_{CE\ (sat)}$	I_C = 1 A, I_B = 33 mA	—	—	0.2	V
Base-emitter saturation voltage		$V_{BE\ (sat)}$	I_C = 1 A, I_B = 33 mA	—	—	1.1	V
Collector output capacitance		C_{ob}	V_{CB} = 10 V, I_E = 0, f = 1MHz	—	23	—	pF
Switching time	Rise time	t_r	See Figure 3 circuit diagram $V_{CC} \simeq$ 50 V, R_L = 50 Ω $I_{B1} = -I_{B2}$ = 33 mA	—	65	—	ns
	Storage time	t_{stg}		—	1.4	—	μs
	Fall time	t_f		—	100	—	ns

Figure 3. Switching Time Test Circuit & Timing Chart

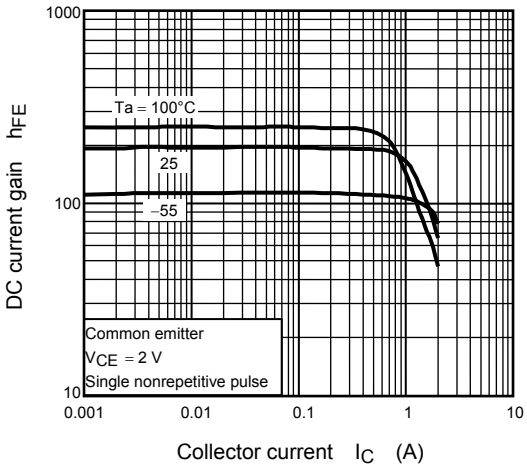




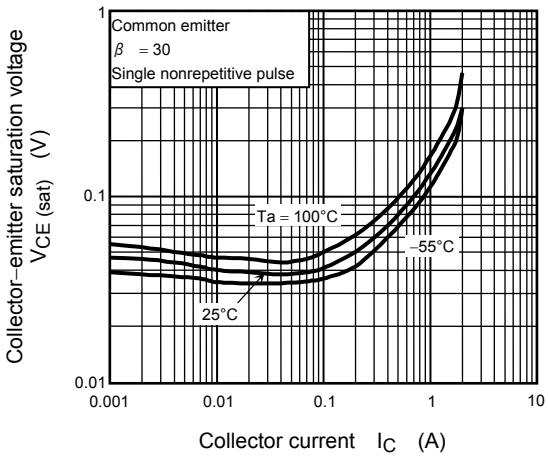
$I_C - V_{CE}$



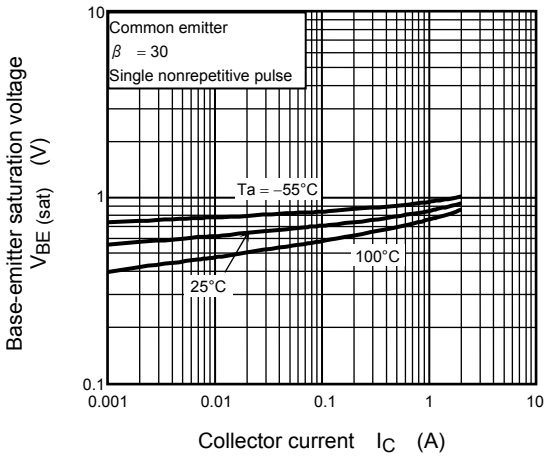
$h_{FE} - I_C$



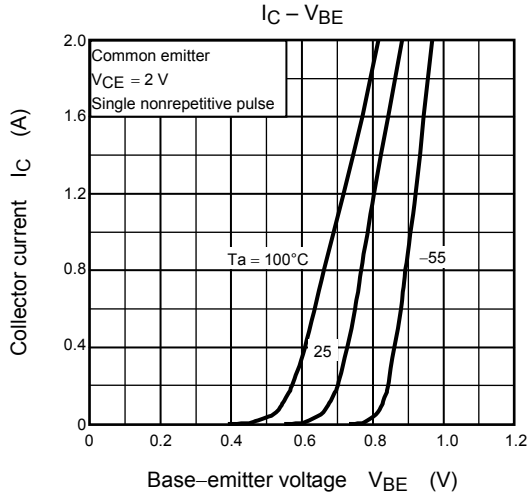
$V_{CE\ (sat)} - I_C$



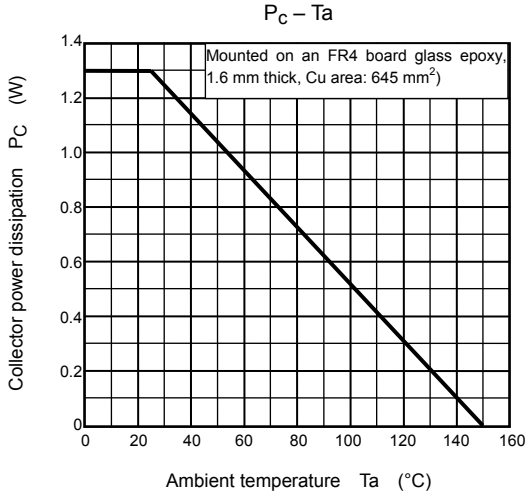
$V_{BE\ (sat)} - I_C$



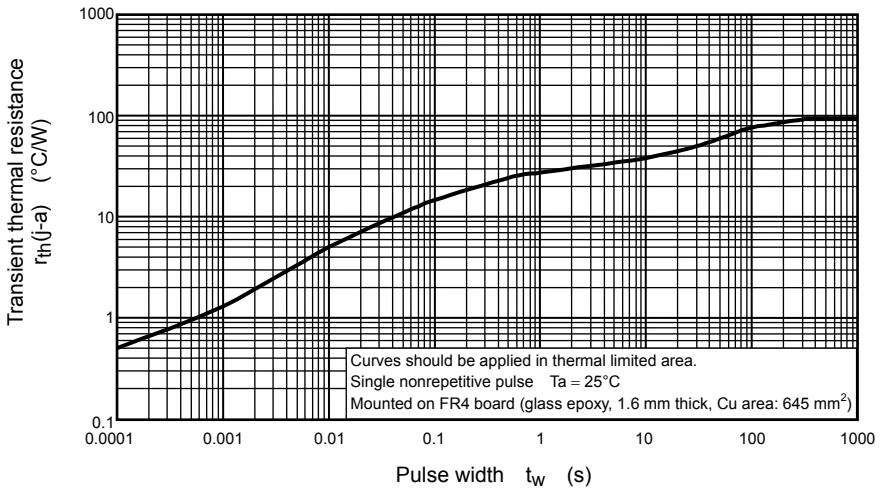
$I_C - V_{BE}$



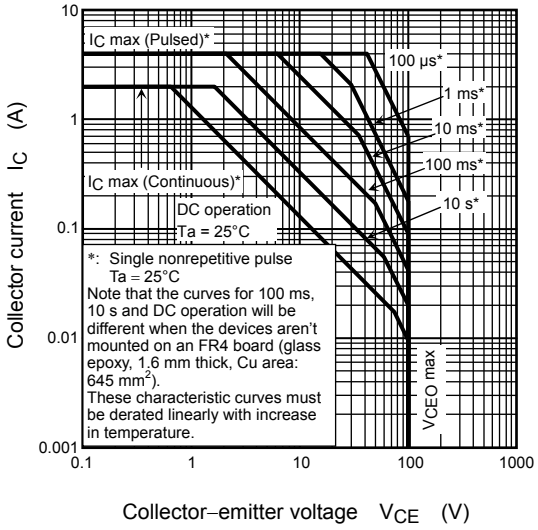
$P_c - Ta$



$r_{th} - t_w$



Safe operating area



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