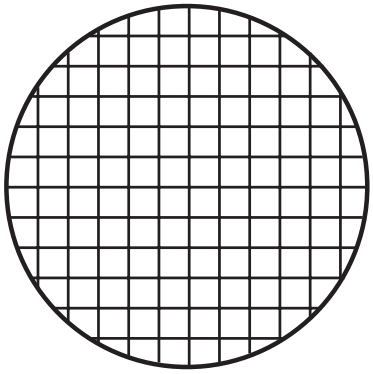
M65KG256AB

256Mbit (4 Banks x 4M x 16)
1.8V Supply, 133MHz Clock Rate, DDR Low Power SDRAM

PRELIMINARY DATA

Features summary

- 256Mbit SYNCHRONOUS DYNAMIC RAM
  - Organized as 4 Banks of 4MWords, each 16 bits wide
- DOUBLE DATA RATE (DDR)
  - 2 Data Transfers/Clock Cycle
  - Data Rate: 266Mbit/s (max.)
- SUPPLY VOLTAGE
  - V_{DD} = 1.7 to 1.9V (1.8V typical in accordance with JEDEC standard)
  - V_{DDQ} = 1.7 to 1.9V for Inputs/Outputs
- SYNCHRONOUS BURST READ AND WRITE
  - Fixed Burst Lengths: 2, 4, 8, 16 Words
  - Burst Types: Sequential and Interleaved.
  - Clock Frequency: 133MHz (7.5ns speed class)
  - Clock Valid to Output Delay ($\overline{CAS}$ Latency): 3 at 133MHz
  - Burst Read Control by Burst Read Terminate and Precharge Commands
- AUTOMATIC PRECHARGE
- BYTE WRITE CONTROLLED BY LDQM AND UDQM
- LOW-POWER FEATURES:
  - Partial Array Self Refresh (PASR)
  - Automatic Temperature Compensated Self Refresh (ATCSR)
  - Driver Strength (DS)
  - Deep Power-Down Mode
  - Auto Refresh and Self Refresh
- LVCMOS Interface Compatible with Multiplexed Addressing
- OPERATING TEMPERATURE
  - - 30 to 85°C



Wafer

The M65KG256AB is only available as part of a multi-chip package Product.

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1 Summary description

The M65KG256AB is a 256Mbit Double Data Rate (DDR) Low Power Synchronous DRAM (LPSDRAM). The memory array is organized as 4 Banks of 4,194,304 Words of 16 bits each.

The device achieves low power consumption and very high-speed data transfer using the 2-bit prefetch pipeline architecture that allows doubling the data input/output rate. Command and address inputs are synchronized with the rising edge of the clock while data inputs/outputs are transferred on both edges of the system clock. The M65KG256AB is well suited for handheld battery powered applications like PDAs, 2.5 and 3G mobile phones and handheld computers.

The device architecture is illustrated in *Figure 2: Functional Block Diagram*. It uses Burst mode to read and write data. It is capable of two, four, eight or sixteen-Word, sequential and interleaved burst.

To minimize current consumption during self refresh operations, the M65KG256AB includes three mechanisms configured via the Extended Mode Register:

- Automatic Temperature Compensated Self Refresh (ATCSR) adapts the refresh frequency according to the operating temperature provided by a built-in temperature sensor.
- Partial Array Self Refresh (PASR) performs a limited refresh of a half bank, a quarter of bank, one bank, two banks or all banks.
- The Deep Power-Down (DPD) mode completely halts the refresh operation and achieves minimum current consumption by cutting off the supply voltage from the whole memory array.

The device is programmable through two registers, the Mode Register and the Extended Mode Register:

- The Mode Register is used to select the $\overline{\text{CAS}}$ Latency, the Burst Type (sequential, interleaved) and the Burst Length. For more details, refer to *Table 7: Mode Register Definition*, and to *3.1: Mode Register Set command (MRS)* in *Section 3: Commands*.
- Partial Array Self Refresh (PASR) performs a limited refresh of a half bank, a quarter of bank, one bank, two banks or all banks.
- The Extended Mode Register is used to configure the low-power features (PASR, ATCSR and Driver Strength) to reduce the current consumption during the Self Refresh operations. For more details, refer to *Table 8: Extended Mode Register Definition*, and to *Section 3.2: Extended Mode Register Set command (EMRS)* in *Section 3: Commands*.

Figure 1. Logic Diagram

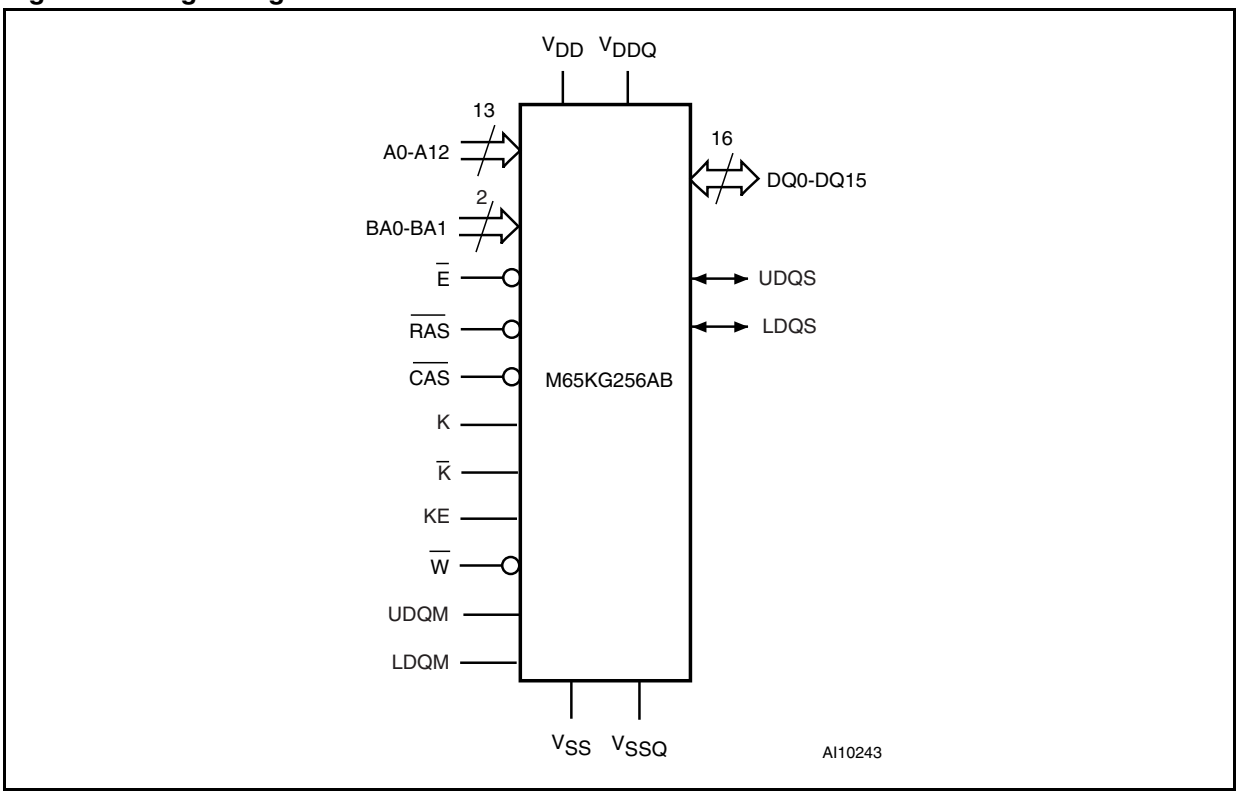
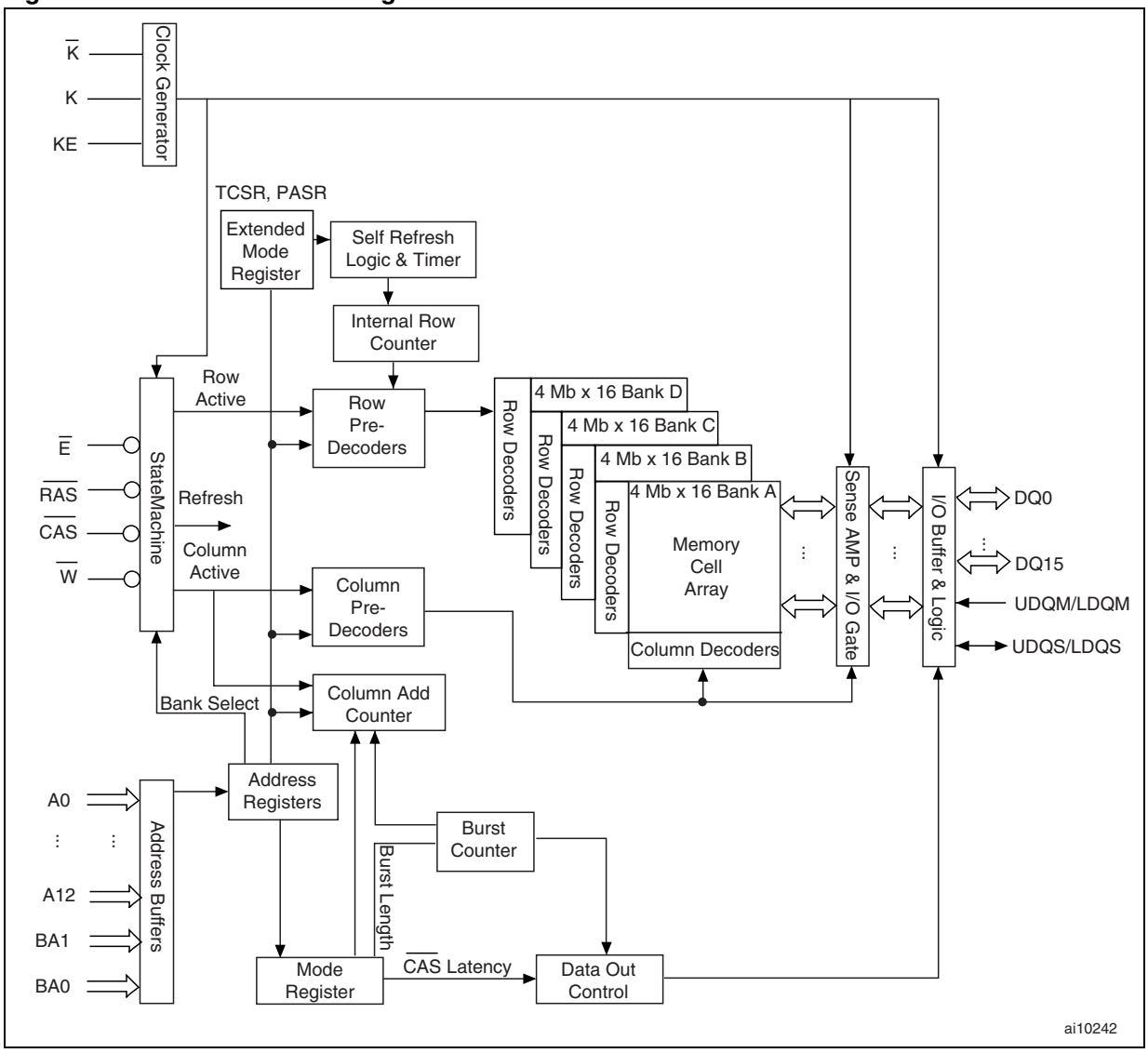


Table 1. Signal Names

A0-A12	Address Inputs
BA0-BA1	Bank Select Inputs
DQ0-DQ15	Data Inputs/Outputs
K, $\overline{K}$	Clock Inputs
KE	Clock Enable Input
$\overline{E}$	Chip Enable Input
$\overline{W}$	Write Enable Input
$\overline{RAS}$	Row Address Strobe Input
$\overline{CAS}$	Column Address Strobe Input
UDQM	Upper Data Input Mask
LDQM	Lower Data Input Mask
UDQS	Upper Data Read/ Write Strobe I/O
LDQS	Lower Data Read/Write Strobe I/O
V_{DD}	Supply Voltage
V_{DDQ}	Input/Output Supply Voltage
V_{SS}	Ground
V_{SSQ}	Input/Output Ground

Figure 2. Functional Block Diagram



2 Signal descriptions

See *Figure 1: Logic Diagram*, and *Table 1: Signal Names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-A12)

The A0-A12 Address Inputs are used to select the row or column to be made active. If a row is selected, all thirteen, A0-A12 Address Inputs are used. If a column is selected, only the nine least significant Address Inputs, A0-A8, are used. In this latter case, A10 determines whether Auto Precharge is used:

- During a Read or Write operation:
  - If A10 is High (set to '1'), the Read or Write operation includes an Auto Precharge cycle.
  - If A10 is Low (set to '0'), the Read or Write cycle does not include an Auto Precharge cycle.
- When issuing a Precharge command:
  - If A10 is Low, only the bank selected by BA1-BA0 will be precharged.
  - If A10 is High, all the banks will be precharged.

The address inputs are latched at the cross point of K rising edge and $\overline{K}$ falling edge.

2.2 Bank Select Address Inputs (BA0-BA1)

The Banks Select Address Inputs, BA0 and BA1, are used to select the bank to be made active (see *Table 2: Bank Selection using BA0-BA1*).

When selecting the addresses, the device must be enabled, the Row Address Strobe, $\overline{RAS}$, must be Low, V_{IL}, the Column Address Strobe, $\overline{CAS}$, and $\overline{W}$ must be High, V_{IH}.

2.3 Data Inputs/Outputs (DQ0-DQ15)

The Data Inputs/Outputs output the data stored at the selected address during a Read operation, or to input the data during a write operation.

2.4 Chip Enable ($\overline{E}$)

The Chip Enable input, $\overline{E}$, activates the memory state machine, address buffers and decoders when driven Low, V_{IL}. When $\overline{E}$ is High, V_{IH}, the device is not selected.

2.5 Column Address Strobe ($\overline{CAS}$)

The Column Address Strobe, $\overline{CAS}$, is used in conjunction with Address Inputs A8-A0 and BA1-BA0, to select the starting column location prior to a read or write operation.

2.6 Row Address Strobe ($\overline{RAS}$)

The Row Address Strobe, $\overline{RAS}$, is used in conjunction with Address Inputs A11-A0 and BA1-BA0, to select the starting address location prior to a Read or Write.

2.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing.

2.8 Clock Inputs (K, $\overline{K}$)

The Clock signals, K and $\overline{K}$, are the master clock inputs. All input signals except UDQM/LDQM, UDQS/LDQS and DQ0-DQ15 are referred to the cross point of K rising edge and $\overline{K}$ falling edge. During read operations, UDQS/LDQS and DQ0-DQ15 are referred to the cross point of K rising edge and $\overline{K}$ falling edge. During write operations, UDQM/LDQM and DQ0-DQ15 are referred to the cross point of UDQS/LDQS and $V_{REF,}$ and UDQS/LDQS to the cross point of K rising edge and $\overline{K}$ falling edge.

2.9 Clock Enable (KE)

When driven Low, V_{IL}, the Clock Enable input, KE, is used to suspend the Clock K, to switch the device to Self Refresh, Power-Down or Deep Power-Down mode.

The Clock Enable, KE, must be stable for at least one clock cycle. This means that, if KE level changes on K rising edge and $\overline{K}$ falling edge with a setup time of t_{AS}, it must be at the same level by the next K rising edge with a hold time of t_{AH}.

2.10 Lower/Upper Data Input Mask (LDQM, UDQM)

Lower Data Input Mask and Upper Data Input Mask are input signals used to mask the written data. UDQM and LDQM are sampled when UDQS/LDQS level crosses $V_{REF.}$ When LDQM is Low, V_{IL}, DQ0 to DQ7 Inputs/Outputs are selected. When UDQM is Low, V_{IL}, DQ8 to DQ15 Inputs/Outputs are selected.

2.11 Lower/Upper Data Read/Write Strobe Input/Output (LDQS, UDQS)

LDQS and UDQS can be either input or output signals and act as write data strobe and read data strobe respectively. LDQS and UDQS are the strobe signals for DQ0 to DQ7 and DQ8 to DQ15, respectively.

2.12 V_{DD} Supply Voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read and Write).

2.13 V_{DDQ} Supply Voltage

V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently of V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply. It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid certain conditions that would result in data corruption.

2.14 V_{SS} Ground

Ground, $V_{SS,}$ is the reference for the core power supply. It must be connected to the system ground.

2.15 V_{SSQ} Ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package).

Table 2. Bank Selection using BA0-BA1

Selected Bank	BA0	BA1
Bank A	V_{IL}	V_{IL}
Bank B	V_{IH}	V_{IL}
Bank C	V_{IL}	V_{IH}
Bank D	V_{IH}	V_{IH}

3 Commands

The M65KG256AB recognizes a set of commands that are obtained by specific statuses of Chip Enable, $\overline{E}$, Column Address Strobe, $\overline{CAS}$, Row Address Strobe, $\overline{RAS}$, Write Enable, $\overline{W}$, and address inputs. Refer to *Table 3: Commands*, in conjunction with the text descriptions below.

Figure 3: Simplified Command State Diagram shows the operations that are performed when each command is issued at each state of the DDR LPSDRAM.

3.1 Mode Register Set command (MRS)

The Mode Register Set command is used to configure the Burst Length, Burst Type and $\overline{CAS}$ Latency of the device by programming the Mode Register.

The command is issued with KE held High, with BA0, BA1 and A10 set to '0', and $\overline{E}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ driven Low, V_{IL}. The value of address inputs A0 to A7 determines the Burst Length, Burst Type and $\overline{CAS}$ Latency of the device (see *Table 7: Mode Register Definition* and *Figure 19: Mode Register/Extended Mode Register Set Commands AC Waveforms*):

- The Burst Length (2, 4, 8, 16 Words) is programmed using the address inputs A2-A0
- The Burst Type (sequential or interleaved) is programmed using A3.
- The $\overline{CAS}$ Latency (3 Clock cycles) is programmed using A6-A4.

It is required to execute a Mode Register Set command at the end of the Power-up sequence. Once the command has been issued, it is necessary to wait for at least two clock cycles before issuing another command.

3.2 Extended Mode Register Set command (EMRS)

The Extended Mode Register Set command is used to configure the low-power features of the device by programming the Extended Mode Register.

The command is issued with KE held High, BA0 at '0', BA1 at '1', A10 at '0', by driving $\overline{E}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$, Low, V_{IL}. The value of address inputs A0 to A9 determines the Driver Strength, the part of the array that is refreshed during Self Refresh and the Automatic Temperature Compensated Self Refresh feature (see *Table 8: Extended Mode Register Definition* and *Figure 19: Mode Register/Extended Mode Register Set Commands AC Waveforms*):

- The part of the array to be refreshed (all banks, Bank A and B, Bank A only) during Self Refresh is set using A2-A0.
- The Driver Strength (full, 1/2 strength, 1/4 strength, 1/8 strength) is set using bits A6-A5
- The Automatic temperature Compensated Self Refresh feature is always enabled (A9 set to '0').

It is required to execute an Extended Mode Register Set command at the end of the Power-up sequence. Once the command has been issued, it is necessary to wait for at least two clock cycles before issuing another command.

3.3 Bank(Row) Activate command (ACT)

The Bank(Row) Activate command is used to switch a row in a specific bank of the device from the Idle to the active mode. The bank is selected by BA0 and BA1 and the row by A0 to A12 (see *Table 2: Bank Selection using BA0-BA1*).

This command is initiated by driving KE High, V_{IH}, with $\overline{E}$ and $\overline{RAS}$ Low, $V_{IL,}$ and $\overline{CAS}$ and $\overline{W}$ High.

A minimum delay of t_{RC} is required after issuing the Bank (Row) Activate command prior to initiating Read and Write operations from and to the active bank.

A minimum time of t_{RC} is required between two Bank(Row) Activate commands to the same bank (see *Figure 6: Consecutive Bank(Row) Activate Command*).

3.4 Read command (READ)

The Read command is used to read from the memory array in Burst Read mode. In this mode, data is output in bursts synchronized with the cross points of the clock signals, K and $\overline{K}$.

The start address of the Burst Read is determined by the column address, A0 to A12, and the bank address, BA0-BA1, at the beginning of the Burst Read operation. A valid Read command is initiated by driving $\overline{E}$ and $\overline{CAS}$ Low, V_{IL}, and $\overline{W}$ and $\overline{RAS}$ High, V_{IH}.

3.5 Read with Auto Precharge (READA)

This command is identical to the Read command except that a precharge is automatically performed at the end of the Read operation. The precharge starts t_{RPD} (Burst Length/2 clock periods) after the Read with Auto Precharge command is input.

A $t_{RAS(min)}$ delay elapses between the Bank (Row) Activate and the Auto Precharge commands. This lock-out mechanism allows a Read with auto Precharge command to be issued to a bank that has been activated (opened) but has not yet satisfied the $t_{RAS(min)}$ requirement.

The DDR LPSDRAM supports the Concurrent Auto Precharge mode: a Read with auto-precharge can be followed by any command to another active bank, as long as that command does not interrupt the read data transfer, and that all other related limitations apply (e.g. contention between read data and written data must be avoided). *Table 4: Minimum Delay Between two Commands in Concurrent Auto Precharge Mode* shows the minimum delays between a Read with Auto Precharge command to one bank and a command to a different bank.

Refer to *Figure 10* for a description of Read operation with Auto Precharge.

3.6 Burst Read Terminate command (BST)

The Burst Read Terminate command is used to terminate a Burst Read operation.

It is issued with KE held High, by driving $\overline{E}$ and $\overline{W}$ Low and $\overline{CAS}$ and $\overline{RAS}$ High. t_{BSTZ} after issuing the Burst Read Terminate command, DQ0-DQ15 and LDQS, UDQS revert to the high impedance state (see *Figure 12: Burst Terminate During Read Operation*).

There is no such command for Burst Write operations.

3.7 Write command (WRIT)

This Write command is used to write to the memory array in Burst Write mode. In this mode, data is input synchronized with the cross points of the clock signals, K and $\overline{K}$.

The start address of the Burst Write is determined by the column address, A0 to A12, and the address of the selected bank, BA0-BA1, at the beginning of the Burst Read operation. A valid Write command is initiated by driving $\overline{E}$, $\overline{CAS}$ and $\overline{W}$ Low, V_{IL}, and $\overline{RAS}$ High, V_{IH}.

3.8 Write with Auto Precharge command (WRITA)

This command is identical to the Write command except that a precharge is automatically performed at the end of the Write operation. The precharge starts t_{WPD} (Burst Length/2 +3 clock periods) after the Write with Auto Precharge command is input.

Refer to *Figure 16* for a description of Write operation with Auto Precharge.

3.9 Precharge Selected Bank/Precharge All Banks command (PRE/PALL)

The Precharge Selected Bank and Precharge All Banks are used to place the bank selected by BA0 and BA1 (see *Table 2: Bank Selection using BA0-BA1*) and all banks in idle mode, respectively.

The precharge commands are issued by driving $\overline{E}$, $\overline{RAS}$ and $\overline{W}$ Low, with $\overline{CAS}$ and KE held High. The value on A10 determines whether either the selected bank or all the banks will be precharged:

- If A10 is High, BA0-BA1 are Don't Care and all the banks are precharged.
- If A10 is Low when, only the bank selected by BA0-BA1 is precharged.

The bank(s) is/are placed in the Idle mode t_{RP} after issuing the Precharge command. Once the bank is in Idle mode, the Bank (Row) Activate command has to be issued to switch the bank back to active mode.

The precharge commands can be issued during Burst Read or Burst Write in which case the Burst Read or Write operation is terminated and the selected bank placed in Idle mode.

The device needs to be in Idle mode before entering Self Refresh, Auto Refresh, Power-Down and Deep Power-Down.

3.10 Self Refresh Entry command (SELF)

The Self Refresh Entry command is used to start a Self Refresh operation. Before starting a Self Refresh, the device must be idle. The Self Refresh Entry command is issued by driving KE Low, with $\overline{E}$, $\overline{RAS}$, and $\overline{CAS}$ Low, and $\overline{W}$ High (see *Figure 25: Self Refresh Entry and Exit Commands AC Waveforms*).

During the Self Refresh operation, the internal memory controller generated the addresses of the row to be refreshed.

The Self Refresh operation goes on as long as the Clock Enable signal, KE, is held Low.

3.11 Self Refresh Exit command (SELFX)

The Self Refresh Exit command is used to exit from Self Refresh mode.

There are two ways to exit from Self Refresh mode:

- Driving KE Low to High, with $\overline{E}$ High, $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ Don't Care,
- Driving $\overline{E}$ Low and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ High.

Non-read commands can be executed $3t_{CK} + t_{RC}$ after the end of the Self Refresh operation, where t_{CK} is the Clock period and t_{RC} the $\overline{RAS}$ Cycle time.

See *Figure 25* for a description of Self Refresh Exit AC waveforms.

3.12 Auto Refresh command (REF)

This command performs an Auto Refresh. The device is placed in Auto refresh mode from Idle by holding KE High, V_{IH}, driving $\overline{E}$, $\overline{RAS}$ and $\overline{CAS}$ Low and driving $\overline{W}$ High. The address bits are "Don't Care" because the addresses of the bank and row to be refreshed are internally determined by the internal refresh controller. The output buffer becomes High-Z after the Auto Refresh has started. Precharge operations are automatically completed after the Auto Refresh. A Bank(Row) Activate, a Mode Register Set or an Extended Mode Register Set command can be issued t_{RFC} after the last Auto Refresh command (see *Figure 24: Auto Refresh Command AC Waveforms*).

The average refresh cycle is t_{REF} (see *Table 15: AC Characteristics*). To optimize the operation scheduling, a flexibility in the absolute refresh interval is provided.

A maximum of eight Auto Refresh commands can be issued to the DDR LPSDRAM and the maximum absolute interval between two Auto Refresh commands $9t_{REF}$.

3.13 Power-Down Entry command (PDEN)

The DDR LPSDRAM is caused to enter Power-Down mode from Idle by driving either:

- KE Low and $\overline{E}$ High (other signals are Don't Care),
- KE Low and $\overline{RAS}$, $\overline{CAS}$ and $\overline{W}$ High with $\overline{E}$ Low.

The Power-Down mode continues as long as KE remains Low.

3.14 Power-Down Exit command (PDEX)

The DDR LPSDRAM exits from Power-Down mode by driving KE High.

3.15 Deep Power-Down Entry command (DPDEN)

The device is placed in Deep Power-Down mode by driving KE Low, with $\overline{E}$ and $\overline{W}$ Low and $\overline{RAS}$ and $\overline{CAS}$ High (see *Figure 26: Deep Power-Down Entry Command AC Waveforms*). All banks must be precharged or in idle state before entering the Deep Power-Down mode.

After the command execution, the device remains in Deep Power-Down mode while KE is low.

Deep Power-Down Exit (DPDEX)

The M65KG256AB exits Deep Power-Down mode by asserting KE High. A special sequence is then required before the device can take any new command into account:

1. Maintain No Operation status conditions for a minimum of 200µs,
2. Issue a Precharge All Banks command (see *Section 3.9: Precharge Selected Bank/ Precharge All Banks command (PRE/PALL)* for details),
3. Once all banks are precharged and after the minimum t_{RP} delay is satisfied, issue 2 or more Auto Refresh commands,
4. Issue a Mode Register Set command to initialize the Mode Register bits,
5. Issue an Extended Mode Register Set command to initialize the Extended Mode Register bits.

The Deep Power-Down mode exit sequence is illustrated in *Figure 27: Deep Power-Down Exit AC Waveforms*.

3.16 Device Deselect command (DESL)

When the Chip Enable, $\overline{E}$, is High at the cross point of the Clock K rising edge with V_{REF}, all input signals are ignored and the device internal status is held.

3.17 No Operation command (NOP)

The device is placed in the No Operation mode, by driving $\overline{CAS}$, $\overline{RAS}$ and $\overline{W}$ High, with $\overline{E}$ Low and KE High.

As long as this command is input at the cross point of the Clock K rising edge with the V_{REF} level, address and data input are ignored and the device internal status is held.

Table 3. Commands

Command[1]	Symbol	KE_{n-1}[2]	KE_n (2)	$\overline{E}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	BA1	BA0	A0-A9, A11-A12	A10
Mode Register Set	MRS	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	MR/EMR Data[3]	V_{IL}
Extended Mode Register Set	EMRS							V_{IH}		MR/EMR Data[3]	
Bank (Row) Activate	ACT	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V	V	Row Address	
Read	READ	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V	V	Column Address	V_{IL}[4]
Read with Auto Precharge	READA										V_{IH}[5]
Burst Read Terminate	BST	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	X	
Write	WRIT	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V	V	Column Address	V_{IL}[4]
Write with Auto Precharge	WRITA										V_{IH}[5]
Precharge Selected Bank	PRE	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V[6]	V[6]	X	V_{IL}[6]
Precharge All Banks	PALL							X[7]	X[7]	X	V_{IH}[7]
Self-Refresh Entry[8]	SELF	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	X	X
Self Refresh Exit	SELFX	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	X		X
				V_{IL}	V_{IH}	V_{IH}	V_{IH}				
Auto Refresh[8]	REF	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X		X
Power-Down Entry[8]	PDEN	V_{IH}	V_{IL}	V_{IH}	X	X	X	X	X		X
				V_{IL}	V_{IH}	V_{IH}	V_{IH}				
Power-Down Exit	PDEX	V_{IL}	V_{IH}	V_{IH}	X	X	X	X	X		X
				V_{IL}	V_{IH}	V_{IH}	V_{IH}				
Deep Power-down Entry[8]	DPDEN	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X		X
Deep Power-down Exit	DPDEX	V_{IL}	V_{IH}	X	X	X	X	X	X		X

1. X = Don't Care (V_{IL} or V_{IH}); V = Valid Address Input.
2. Clock Enable KE must be stable at least for one clock cycle.
3. MR and EMR data is the value to be written in the Mode Register and Extended Mode Register, respectively.
4. If A10 is Low, V_{IL}, when issuing the command, the row remains active at the end of the operation.
5. If A10 is High, V_{IH}, when issuing the command, an automatic precharge cycle is performed at the end of the operation and the row reverts to the Idle mode.
6. If A10 is Low, V_{IL}, when issuing the command, only the bank selected by BA0-BA1 is precharged (BA0-BA1 should be valid).
7. If A10 is High, V_{IH}, when issuing the command, all the banks are precharged and BA0-BA1 are Don't Care.
8. All the banks must be idle before executing this command.

Table 4. Minimum Delay Between two Commands in Concurrent Auto Precharge Mode

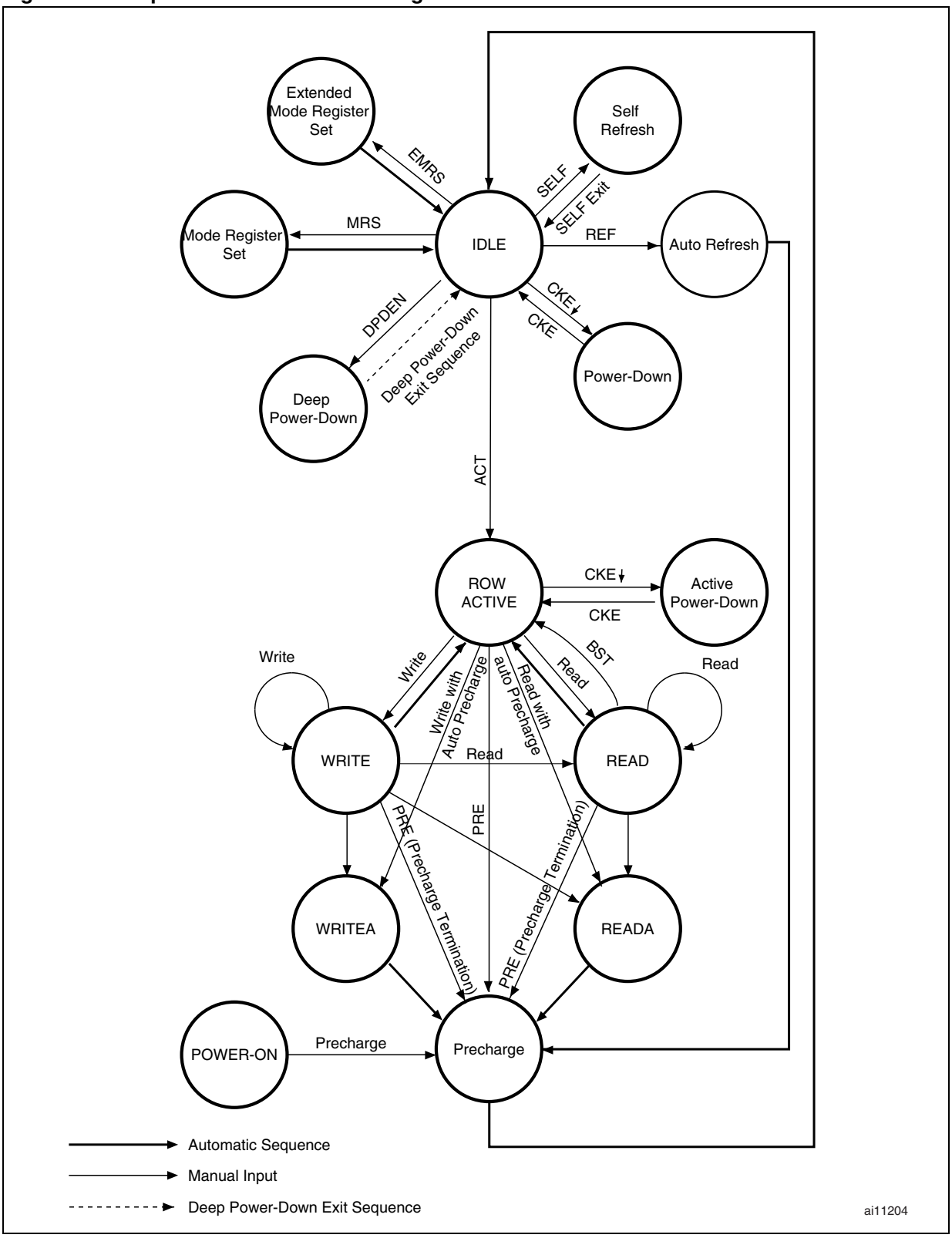
From Command	To Command[1]	Minimum Delay Between the 2 Commands in Concurrent auto Precharge Mode[2]	Unit
READA	READ or READA	BL/2	t_{CK}
	WRITE or WRITEA	$\overline{CAS}$ Latency (rounded up) + BL/2	t_{CK}
	PRE, PALL or ACT	1	t_{CK}
WRITEA	READ or READA	1 + BL/2 + t_{WTR}	t_{CK}
	WRITE or WRITEA	BL/2	t_{CK}
	PRE, PALL or ACT	1	t_{CK}

1. This command must be issued to a different Bank from the initial command and must not interrupt it.
2. BL = Burst Length.

Table 5. Burst Type Definition

Start Addr. (A0-A3)	Burst Length = 2 Words		Burst Length = 4 Words		Burst Length = 8 Words		Burst Length = 16 Words	
	Sequen-tial	Inter-leaved	Sequen-tial	Inter-leaved	Sequential	Interleaved	Sequential	Interleaved
00h	0-1	0-1	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-..D-E-F	0-1-2-..D-E-F
01h	1-0	1-0	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3..D-E-F-0	1-0-3-..C-F-E
02h			2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4..E-F-0-1	2-3-0- ..F-C-D
03h			3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5..F-0-1-2	3-2-1-..E-D-C
04h					4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6..0-1-2-3	4-5-6-..9-A-B
05h					5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7..1-2-3-4	5-4-7..8-B-A
06h					6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8..2-3-4-5	6-7-4-..B-8-9
07h					7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9..3-4-5-6	7-6-5-..A-9-8
08h							8-9-A..4-5-6-7	8-9-A..5-6-7
09h							9-A-B..5-6-7-8	9-8-A..4-7-6
0Ah							A-B-C..6-7-8-9	A-B-8..7-4-5
0Bh							B-C-D..7-8-9-A	B-A-9..6-5-4
0Ch							C-D-E..8-9-A-B	C-D-E..1-2-3
0Dh							D-E-F..9-A-B-C	D-C-F..0-3-2
0Eh							E-F-0..A-B-C-D	E-F-C..3-0-1
0Fh							F-0-1..B-C-D-E	F-E-D..2-1-0

Figure 3. Simplified Command State Diagram



4 Operating modes

There are 7 operating modes that control the memory. Each of these is composed by a sequence of commands (see *Table 6: Operating Modes* for a summary).

4.1 Power-Up

The DDR LPSDRAM has to be powered up and initialized in a well determined manner:

1. After applying power to V_{DD} and V_{DDQ} an initial pause of at least 200µs is required before the signals can be toggled.
2. The Precharge command must then be issued to all banks. Until the command is issued KE and $\overline{UDQM}$/$\overline{LDQM}$ must be held High to make sure that DQ0-DQ15 remain high impedance.
3. t_{RP} after precharging all the banks, the Mode Register and the Extended Mode Register must be set by issuing a Mode Register Set command and an Extended Mode Register Set command, respectively. A minimum pause of t_{MRD} must be respected after each register set command.
4. After the two registers are configured, two or more auto Refresh cycles must be executed before the device is ready for normal operation.

The third and fourth steps can be swapped.

Refer to *Figure 23* for a detailed description of the Power-Up AC waveforms.

4.2 Burst Read

The M65KG256AB is switched in Burst Read mode by issuing a Bank (Row) Activate command to set the bank and column addresses to be read from, followed by a Read command (see sections *3.3: Bank(Row) Activate command (ACT)* and *3.4: Read command (READ)* for details).

Burst Read can be accompanied by an Auto Precharge cycle depending on the state of the A10 Address Input. If A10 is High (set to '1') when the Burst Read command is issued, the Burst Read operation will be followed by an Auto Precharge cycle. If A10 is Low (set to '0'), the row will remain active for subsequent accesses.

Burst Read operations are performed at Word level only. Different Burst Types (sequential or interleaved), Burst Lengths (2, 4, 8 or 16 Words) can be programmed using the Mode Register bits. Only a $\overline{CAS}$ Latency of 3 clock cycles is available. Refer to *Section 5.1: Mode Register description*, and to *Section 3.1: Mode Register Set command (MRS)*, for details on the Mode Register bits and how to program them.

The Burst Read starts $3t_{CK} + t_{AC}$ after the Clock K rising edge where the Read command is latched, where t_{CK} is the Clock period and t_{AC} is the access time from K or $\overline{K}$. Data Strobe, UDQS/LDQS, are output simultaneously with data. t_{RPRE} prior to the first rising edge of the data strobe, the UDQS/LDQS signals go from High-Z to Low state. This Low pulse is referred to as the Read Preamble. The burst data are then output synchronized with the rising and falling edge of the data strobe. UDQS/LDQS become High-Z on the next clock cycle after the Burst

Read is completed. t_{RPST} from the last falling edge of the data strobe, the DQS pins become High-Z. This low period of DQS is referred as Read Postamble.

See *Table 5: Burst Type Definition*, *Table 15: AC Characteristics*, *Table 16: AC Characteristics Measured in Clock Period*, and Figures *9* and *11*, for a detailed description of Burst Read operation and characteristics.

Burst Read can be terminated by issuing a Burst Read Terminate command (see *Section 3.6: Burst Read Terminate command (BST)* and *Figure 12: Burst Terminate During Read Operation*).

The interval between Burst Read to Burst Read and Burst Read to Burst Write commands are described in Figures *7*, *8* and *20*.

4.3 Burst Write

The M65KG256AB is switched in Burst Write mode by issuing a Bank (Row) Activate command to set the bank and column addresses to be written to, followed by a Write command (see sections *3.3: Bank(Row) Activate command (ACT)* and *3.7: Write command (WRIT)* for details).

Burst Write can be accompanied by an Auto Precharge cycle depending on the state of the A10 Address Input. If A10 is High (set to '1') when the Write command is issued, the Write operation will be followed by an Auto Precharge cycle. If A10 is Low (set to '0'), Auto Precharge is not selected and the row will remain active for subsequent accesses.

Burst Write operations can be performed either at Byte or at Word level. The $\overline{CAS}$ Latency for Burst Write operations is fixed to 1 clock cycle.

UDQS/LDQS input act as the strobe for the input data and UDQM/LDQM select the Byte to be written. UDQS/LDQS must be Low t_{WPRE} prior to their first rising edge; and can be changed to High-Z t_{WPST} after their last falling edge. These two periods of time are referred to as Write Preamble and Write Postamble, respectively.

See *Table 15: AC Characteristics*, *Table 16: AC Characteristics Measured in Clock Period*, and Figures *15*, *17*, and *18*, for a detailed description of Burst Write AC waveforms and characteristics.

The interval between Burst Write to Burst Write commands are described in Figures *13*, *14*, *21* and *22*.

4.4 Self Refresh

In the Self Refresh mode, the data contained in the DDR LPSDRAM memory array is retained and refreshed. The size of the memory array to be refreshed is programmed in the Extended Mode Register. Only the data contained in the part of the array selected for Self Refresh will be retained and refreshed. In this respect, this is a power saving feature.

The Self Refresh mode is entered and exited by issuing a Self Refresh Entry and Self Refresh Exit command, respectively (see *Section 3: Commands*). When in this mode, the device is not clocked any more.

4.5 Auto Refresh

The Automatic Temperature Compensated Self Refresh mode (ATCSR) is used to refresh the whole DDR RAM array in normal operation mode whenever needed.

The device is placed in the Auto Refresh mode by issuing an Auto Refresh command (see *Section 3: Commands*).

4.6 Power-Down

In Power-Down mode, the current is reduced to the active standby current (I_{DD3P}).

The Power-Down mode is initiated by issuing a Power-Down Entry command. t_{PDEN} (1 clock cycle) after the cycle when this command was issued, the DDR LPSDRAM enters into Power-Down mode. In Power-Down mode, power consumption is reduced by deactivating the input initial circuit. There is no internal refresh when the device is in the Power-Down mode.

The device can exit from Power-Down t_{PDEX} (1 cycle minimum) after issuing a Power-Down Exit command.

See *Section 3: Commands* for details on the Power-Down Entry and Exit commands.

4.7 Deep Power-Down

In Deep Power-Down mode, the power consumption is reduced to the standby current (I_{DD7}).

Before putting the device in the Deep Power-Down mode all the banks must be Idle or have been precharged.

The Deep Power-Down mode is entered and exited by issuing a Deep Power-Down Entry and a Deep Power-Down Exit command.

See *Section 3: Commands* for details on the Power-Down Entry and Exit commands.

Table 6. Operating Modes

Operating Mode(1)	KEn-1	KEn	$\overline{E}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	A10	A9, A11	A0-A8	BA0-BA1
Burst Read	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}(2)	X	Start Column Address	Bank Select
Burst Write	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}(2)	X	Start Column Address	Bank Select
Self Refresh	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X			X
Auto Refresh	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X			X
Power-Down	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X			X
			V_{IH}	X	X	X				
Deep Power-Down	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X			X

1. X = Don't Care V_{IL} or V_{IH}.
2. If A10 = V_{IL} the Burst Read or Write operation is not followed by an Auto Precharge cycle. If A10 = V_{IH}, the Burst Read or Write operation is followed by an Auto Precharge cycle to the bank selected by BA0-BA1.

5 Registers description

The DDR Mobile RAM has the two mode registers, the Mode Register and the Extended Mode register.

5.1 Mode Register description

The Mode Register is used to select the $\overline{CAS}$ Latency, Burst Type, and Burst Length of the device:

- The $\overline{CAS}$ Latency defines the number of clock cycles after which the first data will be output during a Burst Read operation.
- The Burst Type specifies the order in which the burst data will be addressed. This order is programmable either to sequential or interleaved (see *Table 5: Burst Type Definition*).
- The Burst Length is the number of Words that will be output or input during a Burst Read or Write operation. It can be configured as 2, 4, 8 or 16 Words.

The Mode Register must be programmed at the end of the Power-Up sequence prior to issuing any command. It is loaded by issuing a *Mode Register Set command (MRS)*, with BA0-BA1 are set to '00' to select the Mode Register.

Table 7: Mode Register Definition, shows the available Mode Register configurations.

Table 7. Mode Register Definition

Address Bits	Mode Register Bit	Register Description	Value	Description
A12-A7	-	-	000000	
A6-A4	MR6-MR4	$\overline{CAS}$ Latency Bits (Read Operations)	011	3 Clock Cycles
			Other configurations reserved	
A3	MR3	Burst Type Bit	0	Sequential
			1	Interleaved
A2-A0	MR2-MR0	Burst Length Bit	001	2 Words
			010	4 Words
			011	8 Words
			100	16 Words
			Other configurations reserved	
BA1-BA0	-	-	00	

5.2 Extended Mode Register description

The Extended Mode Register is used to program the low-power Self Refresh operation of the device:

- Partial Array Self Refresh
- Driver Strength
- Automatic Temperature Compensated Self Refresh.

It is loaded by issuing a *Extended Mode Register Set command (EMRS)* with BA0-BA1 set to '01' to select the Extended Mode Register.

Table 8: Extended Mode Register Definition, shows the available Extended Mode Register configurations.

Table 8. Extended Mode Register Definition

Address Bits	Mode Register Bit	Description	Value	Description
A12-A10	-	-	000	
A9	EMR9	Automatic Temperature Compensated Self Refresh Bits	0	Enabled
			1	Reserved
A8-A7	-	-	00	
A6-A5	EMR6-EMR5	Driver Strength Bits	00	Full Strength
			01	1/2 Strength
			10	1/4 Strength
			11	1/8 Strength
A4-A3	-	-	00	
A2-A0	EMR2-EMR0	Partial Array Self Refresh Bits	000	All Banks
			001	Bank A and Bank B (BA1=0)
			010	Bank A (BA0 and BA1 =0)
			Other configurations reserved	
BA1-BA0	-	-	10	

6 Maximum rating

Stressing the device above the ratings listed in *Table 9: Absolute Maximum Ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_J	Junction Temperature	-30	85	°C
T_{STG}	Storage Temperature	-55	125	°C
V_{IO}	Input or Output Voltage	-0.5	2.3	V
V_{DD}, V_{DDQ}	Supply Voltage	-0.5	2.3	V
I_{OS}	Short Circuit Output Current	50		mA
PD	Power Dissipation	1.0		W

7 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 10*. AC characteristics are measured with driver strength set to “Full Strength” (EMR5-EMR6 set to ‘00’). Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 10. Operating and AC Measurement Conditions

Symbol	Parameter(1)	M65KG256AB			Units
		Min	Typ	Max	
V_{DD}	Supply Voltage	1.7	1.8	1.9	V
V_{DDQ}(2)	Input/Output Supply Voltage	1.7	1.8	1.9	V
T_J	Ambient Temperature	-30		85	°C
C_L	Load Capacitance		15		pF
V_{IL}	Input Pulses Voltages		0.2		V
V_{IH}	Input Pulses Voltages		1.6		V
V_{REF}	Input and Output Timing Ref. Voltages		0.9		V
V_{ID}	Input Differential Voltage (K and $\overline{K}$)		1.4		V
V_{IX}	Input differential Cross Point Voltage (K and $\overline{K}$)		$V_{DDQ}/2$(2)		V
$\Delta V_I/\Delta t_R$	Input Signal Slew Rate		1		V/ns

1. All voltages are referenced to V_{SS}.
2. V_{DD} must be equal to V_{DDQ}.

Figure 4. AC Measurement I/O Waveform

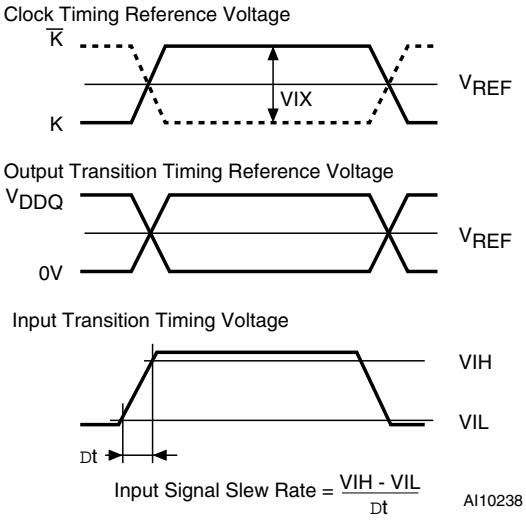


Figure 5. AC Measurement Load Circuit

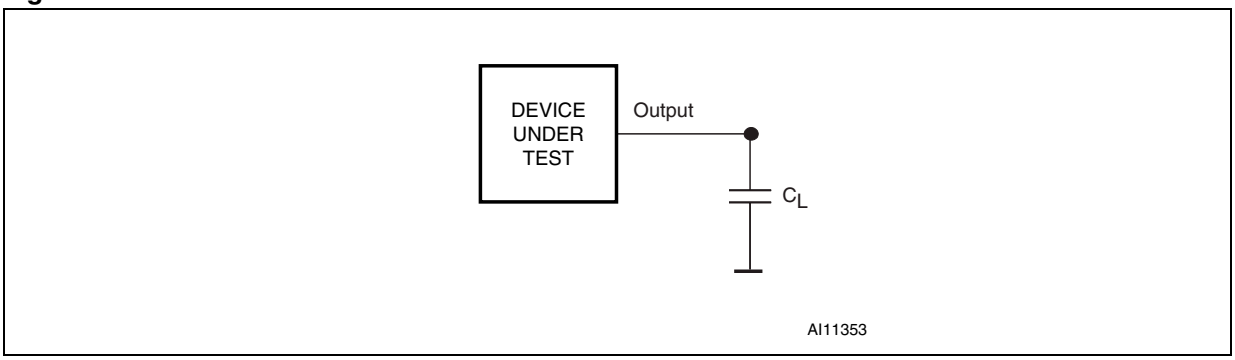


Table 11. Capacitance

Symbol	Parameter	Signal	M65KG256AB		Unit
			Min	Max	
$CI1^{(1)}$	Input Capacitance	K, $\overline{K}$	2.0	3.0	pF
$CI2^{(1)}$		All other input pins	2.0	3.0	pF
$C_{IO}{}^{(1)(2)}$	Data I/O Capacitance	DQ0-DQ15, UDQS/LDQS, LDQM/UDQM	3.0	4.0	pF

1. T_J = 25°C; V_{DD} and V_{DDQ} = 1.7 to 1.9V; f = 133MHz; $V_{OUT} = V_{DDQ}/2$; V_{OUT} = 0.2V.
2. Data Output are disabled.

Table 12. DC Characteristics 1

Symbol	Parameter	Test Condition	M65KG256AB			Unit
			Min	Typ.	Max	
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$	-1.0		1.0	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$, DQ0-DQ15 disabled.	-1.5		1.5	µA
$V_{IH}{}^{(1)}$	Input High Voltage	V_{IN} = 0V	$0.8V_{DDQ}$		V_{DDQ}+0.3	V
$V_{IL}{}^{(2)}$	Input Low Voltage	V_{IN} = 0V	-0.3		0.3	V
V_{OL}	Output Low Voltage	I_{OUT} = 100µA			0.2	V
V_{OH}	Output High Voltage	I_{OUT} = -100µA	V_{DDQ}-0.2			V
V_{IN}	Input Voltage Level for K/$\overline{K}$ inputs		-0.3		V_{DDQ}+0.3	
V_{IX}	Input Differential Cross Point Voltage for K / $\overline{K}$ inputs		$0.5V_{DDQ}$-0.2	$0.5V_{DDQ}$	$0.5V_{DDQ}$+0.2	V
V_{ID}	Input Differential Voltage for K/ $\overline{K}$ inputs		1.0		V_{DDQ}+0.6	V

1. V_{IH} maximum value = 2.6V (pulse width 5ns).
2. V_{IL} minimum value = 1.0V (pulse width 5ns).

Table 13. DC Characteristics 2

Symbol	Parameter	Test Condition(1)(2)	M65KG256AB	Unit
I_{DD1}(2)	Operating Current	Burst length = 4, one bank active $t_{RC} \geq t_{RC}$(min), I_{OL} = 0mA	60	mA
I_{DD2P}	Precharge Standby Current in Power-Down Mode	KE $\leq V_{IL}$(max), t_{CK} = 15ns	0.8	mA
I_{DD2PS}		KE $\leq V_{IL}$(max), $t_{CK} = \infty$	0.6	
I_{DD2N}	Precharge Standby Current in Non Power-Down Mode	KE $\geq V_{IH}$ (min), $\overline{E} \geq V_{IH}$ (min), t_{CK} = 15ns, Input signals changed once in 2 clock cycles.	3	mA
I_{DD2NS}		KE $\geq V_{IH}$ (min), $t_{CK} = \infty$ Input signals are stable	2	
I_{DD3P}	Active Standby Current in Power-Down Mode	KE $\leq V_{IL}$(max), t_{CK} = 15ns	1.5	mA
I_{DD3PS}		KE $\leq V_{IL}$(max), $t_{CK} = \infty$	1.2	
I_{DD3N}	Active Standby Current in Non Power-Down Mode	KE $\geq V_{IH}$ (min), $\overline{E} \geq V_{IH}$ (min), t_{CK} = 15ns, Input signals are changed once in 2 clock cycles.	10	mA
I_{DD3NS}		KE $\geq V_{IH}$ (min), $t_{CK} = \infty$ Input signals are stable	7	
I_{DD4}(2)	Burst Mode Current	$t_{CK} \geq t_{CK}$ (min), I_{OL} = 0mA All banks active Burst Length = 4	130	mA
I_{DD5}(3)	Auto Refresh Current	$t_{RRC} \geq t_{RRC}$ (min)	60	mA
I_{DD6}	Self Refresh Current	KE $\leq$0.2V	See *Table 14*	µA
I_{DD7}	Standby Current in Deep Power-down Mode	KE $\leq$0.2V (see *Deep Power-Down* mode description)	10	µA

1. V_{DD} and V_{DDQ} = 1.7 to 1.9V, V_{SS} = V_{SSQ} = 0V.
2. I_{DD1} and I_{DD4} depend on output loading and cycle rates. Specified values are measured with the output open.
3. Addresses change only once during t_{CK}.

Table 14. Self Refresh Current (I_{DD6}) in Normal Operating Mode

Temperature in °C	Memory Array(1)						Unit
	All Banks		2 Banks		1 Bank		
	Typ	Max	Typ	Max	Typ	Max	
-30 $\leq T_J \leq$40		200		160		160	µA
40 $\leq T_J \leq$65		350		270		220	µA
65 $\leq T_J \leq$85		550		400		320	µA

1. T_J = –30 to 85°C, V_{DD} and V_{DDQ} = 1.7 to 1.9V, V_{SS} = V_{SSQ} = 0V; KE $\leq$0.2V.

Table 15. AC Characteristics

Symbol	Alt	Parameter	M65KG256AB(1)		Unit
			Min	Max	
t_{AC}(2)		Data Output Access Time from K and $\overline{K}$	1.5	6.0	ns
t_{AS}(3)	t_{IS}	Address and Control Input Setup Time	1.4		ns
t_{AH}(3)	t_{IH}	Address Control Input Hold Time	1.4		ns
t_{CK}		Clock Cycle Time	7.5		ns
t_{DQSCK}(2)		UDQS/LDQS Access Time from K and $\overline{K}$	1.5	6.0	ns
t_{DQSHZ}(5)		UDQS/LDQS High-Z Time from K and $\overline{K}$	1.5	6.0	ns
t_{DQSLZ}(6)		UDQS/LDQS Low-Z Time from K and $\overline{K}$	1.5	6.0	ns
t_{DQSQ}(3)		UDQS/LDQS to Data Output Skew		0.65	ns
t_{DV}(4)		Data Output Valid to Data Output Transition Time	2		ns
t_{DS}(3)		Data Input and UDQM/LDQM Setup Time	0.9		ns
t_{DH}(3)		Data Input and UDQM/LDQM Hold Time	0.9		ns
t_{OHZ}(5)	t_{HZ}	Data Output High-Z Time from K and $\overline{K}$	1.5	6.0	ns
t_{OLZ}(6)	t_{LZ}	Data Output Low-Z Time from K and $\overline{K}$	1.5	6.0	ns
t_{RAS}		$\overline{RAS}$ Active Time (Bank (Row) Activate to Bank Precharge)	45	120000	ns
t_{RC}		$\overline{RAS}$ Cycle Time (Bank (Row) Activate to Bank Activate in Auto Refresh mode)	75		ns
t_{RCD}		Delay Time, from $\overline{RAS}$ Active to $\overline{CAS}$ Active	30		ns
t_{RRD}		Delay Time, from $\overline{RAS}$ Active to $\overline{RAS}$ Bank Active	15		ns
t_{RP}		$\overline{RAS}$ Precharge Time	22.5		ns
t_{REF}		Average Periodic Refresh Time		7.8	µs
t_{SRE}	t_{SREX}	Self Refresh Exit Time	16		ns
t_{WPRES}		Write Preamble Setup Time	0		ns

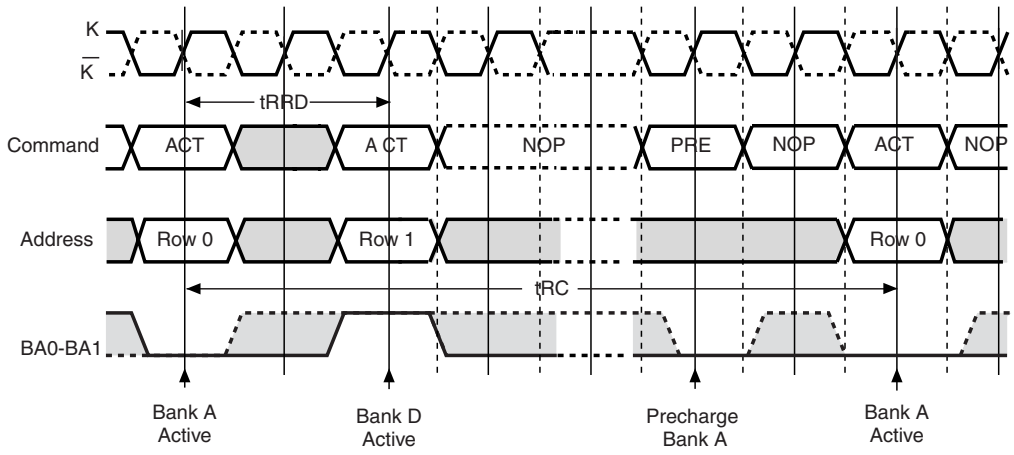
1. The above timings are measured according to the test conditions shown in *Table 10: Operating and AC Measurement Conditions*.
2. These timings define the signal transition delays from K or $\overline{K}$ cross point, that is when K or $\overline{K}$ signal crosses V_{REF}.
3. The timing reference level is V_{REF}.
4. t_{DV} defines the delay between two successive transitions of the data output signals, that is when DQ0-DQ15 cross V_{REF}.
5. t_{OHZ} and t_{DQSHZ} define the transition time from Low-Z to High-Z of DQ0-DQ15 and UDQS/LDQS, at the end of a Burst Read operation, respectively. They specify when data outputs stop being driven.
6. t_{OLZ} and t_{DQSLZ} define the transition time from High-Z to Low-Z of DQ0-DQ15 and UDQS/LDQS, at the end of a Burst Read operation. They specify when data outputs begin to be driven.

Table 16. AC Characteristics Measured in Clock Period

Symbol	Alt	Parameter	M65KG256AB		Unit
			Min	Max	
t_{BSTW}(1)		Burst Read Terminate Command to Write Command Delay Time	3		t_{CK}
t_{BSTZ}(1)		Burst Read Terminate Command to Data Output Hi-Z	3		t_{CK}
t_{CHW}	t_{CH}	Clock High Pulse Width	0.45	0.55	t_{CK}
t_{CLW}	t_{CL}	Clock Low Pulse Width	0.45	0.55	t_{CK}
t_{DAL}		Autoprecharge write recovery and precharge time	$2t_{CK}$ + 22.5		ns
t_{DMD}		UDQM/LDQM to Data Input Latency	0		t_{CK}
t_{DQSS}		Write Command to First UDQS/LDQS Latching Transition	0.75	1.25	t_{CK}
t_{DSS}(2)		UDQS/LDQS Falling Edge to K Setup Time	0.2		t_{CK}
t_{DSH}(2)		UDQS/LDQS Falling Edge Hold Time from K	0.2		t_{CK}
t_{DQSH}		UDQS/LDQS High Pulse Width	0.35		t_{CK}
t_{DQSL}		UDQS/LDQS Low Pulse Width	0.35		t_{CK}
t_{DPE}	t_{PDEN}	Power-Down Entry Time	1		t_{CK}
t_{DPX}	t_{PDEX}	Power-Down Exit Time	1		t_{CK}
t_{MRD}		Mode Register Set Cycle Time	2		t_{CK}
t_{PROZ}(1)	t_{HZP}	Precharge Command to Data Output High-Z	3		t_{CK}
t_{RPRE}		Read Preamble Time	0.9	1.1	t_{CK}
t_{RPST}		Read Postamble Time	0.4	0.6	t_{CK}
t_{RFC}		$\overline{RAS}$ Cycle Time (Auto Refresh to Bank Active in Auto Refresh mode)	15		t_{CK}
t_{RPD}		Delay Time from Read to Precharge Command (same Bank)	BL/2(3)		t_{CK}
t_{RWD}		Delay Time from Read to Write Command (all data output)	3+BL/2(3)		t_{CK}
t_{WTR}		Write to Read command Delay	1		t_{CK}
t_{WPRE}		Write Preamble	0.25		t_{CK}
t_{WPST}(2)		Data Strobe Low Pulse Width (Write Postamble)	0.4	0.6	t_{CK}
t_{WRD}		Delay Time from Write to Read Command (all data input)	2+BL/2(3)		t_{CK}
t_{WPD}		Delay Time from Write to Precharge Command (same Bank)	3+BL/2(3)		t_{CK}
t_{WCD}		Write Command to Data Input Latency	1		t_{CK}
t_{WR}		Write Recovery Time	2		t_{CK}

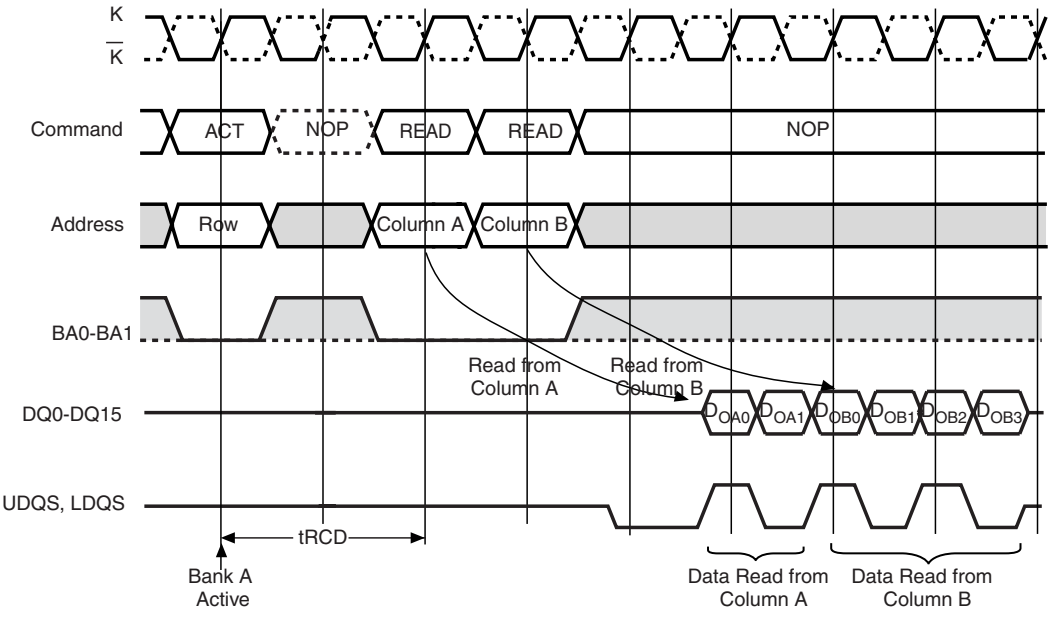
1. $\overline{CAS}$ Latency equals 3 clock cycles.
2. The transition for Low-Z to High-Z occur when the device outputs become floating. No specific reference voltage is given in this document.
3. BL stands for Burst Length.

Figure 6. Consecutive Bank(Row) Activate Command



1. The above figure shows consecutive Bank(Row) Activate commands issued to different banks. A t_{RRD} delay must be respected between two consecutive Bank(Row) Activate commands (ACT) to different banks. If the destination row is already active, the bank must be precharged to close the row; the ACT command can then be issued t_{RP} after the PRE command.
2. Consecutive ACT commands to the same bank must be issued at a t_{RC} interval and separated by a Precharge command (PRE).

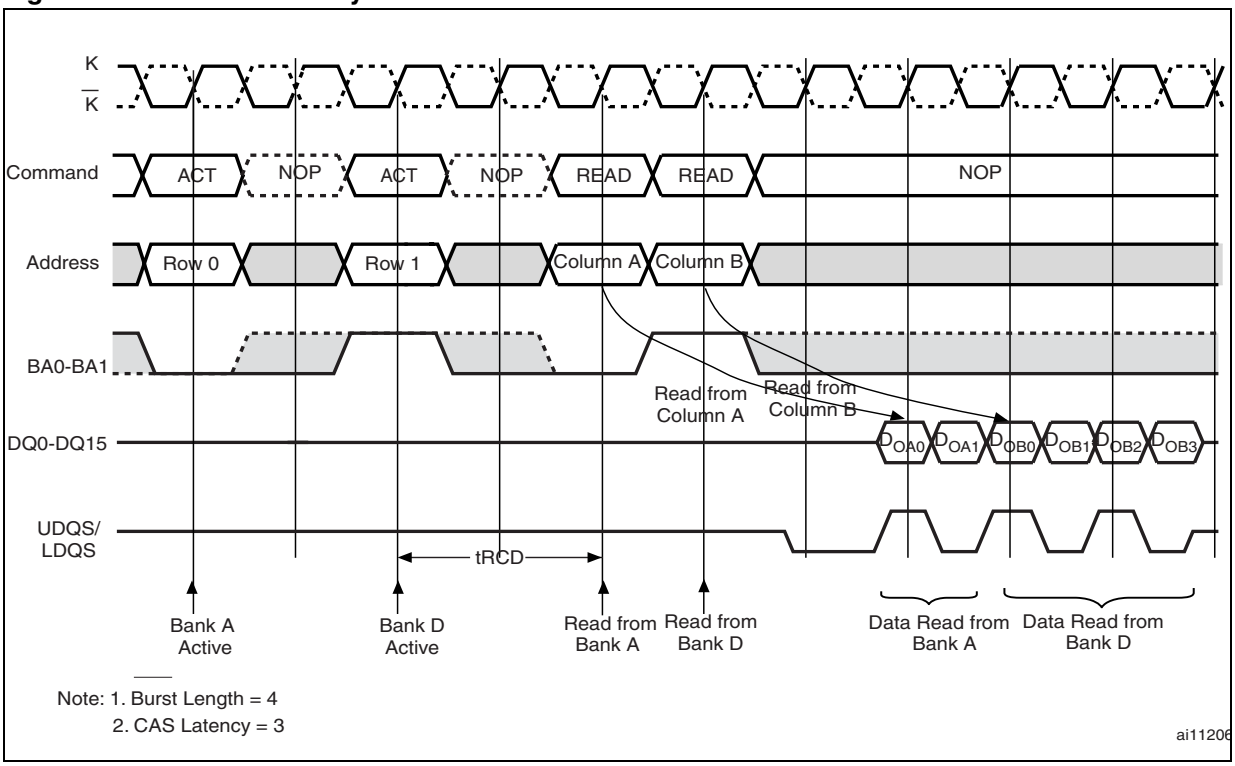
Figure 7. Read followed by Read in Same Bank and Row



Note: 1. Burst Length = 4
2. $\overline{CAS}$ Latency = 3
3. Bank = Bank A

1. The consecutive READ command must be issued after a minimum delay of t_{CK} to interrupt the previous Read operation.
2. To issue the consecutive READ to a different row, precharge the bank (PRE) to interrupt the previous Read operation. t_{RP} after the PRE command, issue the ACT command. The consecutive READ command can be issued t_{RCD} after the ACT command.

Figure 8. Read followed by Read in a Different Bank



1. If the consecutive Read operation targets an active row, the second READ command must be issued after a minimum delay of t_{CK} to interrupt the previous Read operation.
2. If the consecutive Read operation targets an idle row, precharge the bank (PRE) without interrupting the previous Read operation. t_{RP} after the PRE command, issue the ACT command. The consecutive READ command can be issued t_{RCD} after the ACT command.

Figure 9. Read with Auto Precharge

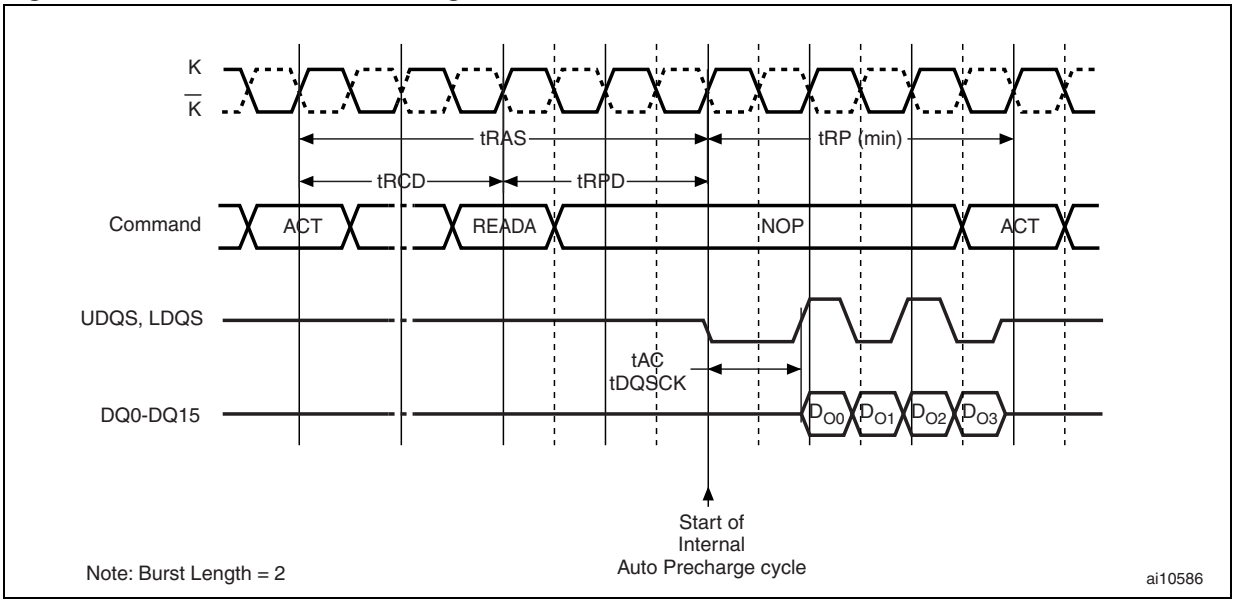
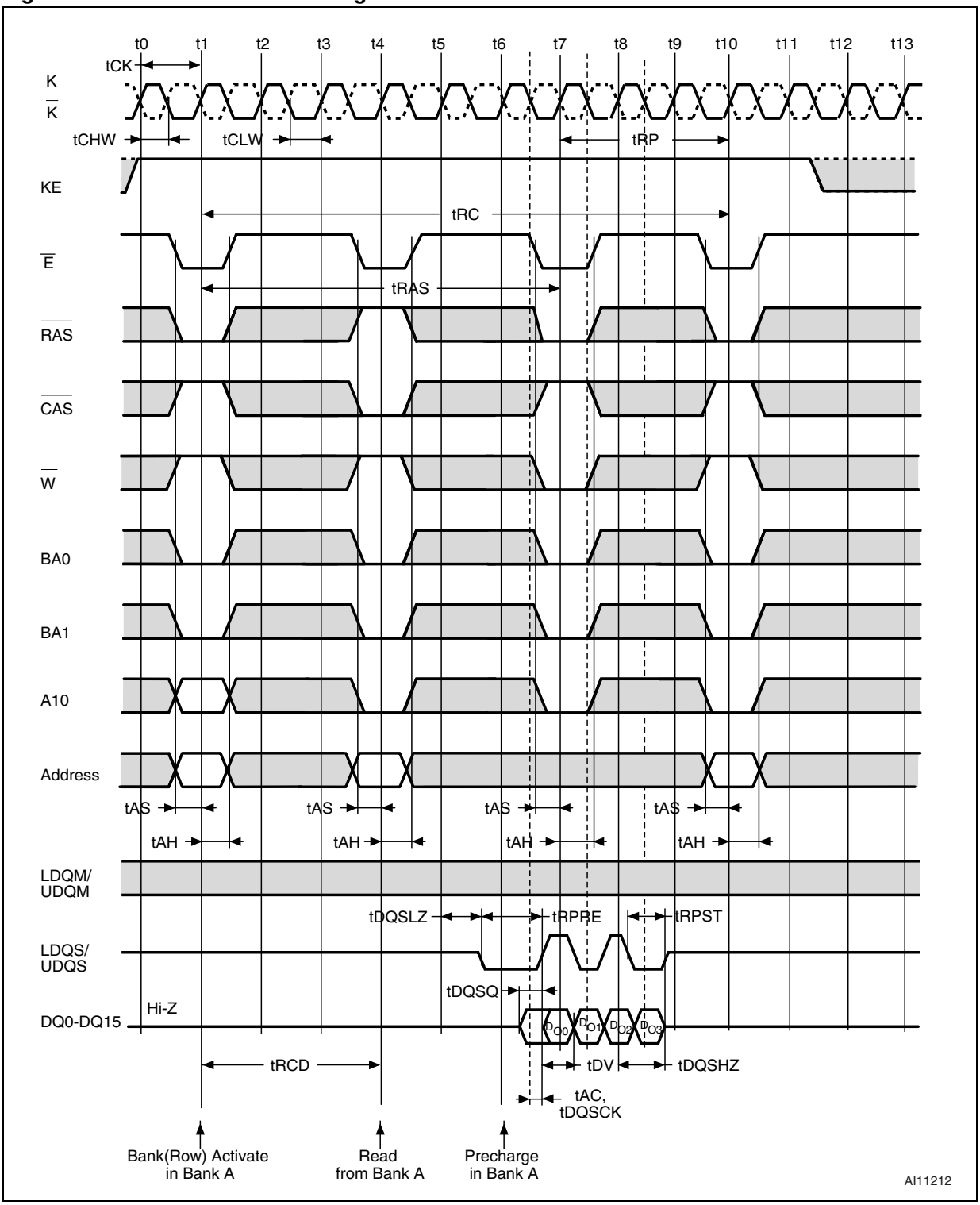


Figure 10. Read with Auto Precharge AC Waveforms



1. Burst Length = 4 Words, $\overline{CAS}$ Latency = 3 clock cycles.

Figure 11. Read Operation (Burst Lengths = 2, 4 and 8, $\overline{CAS}$ Latency = 3)

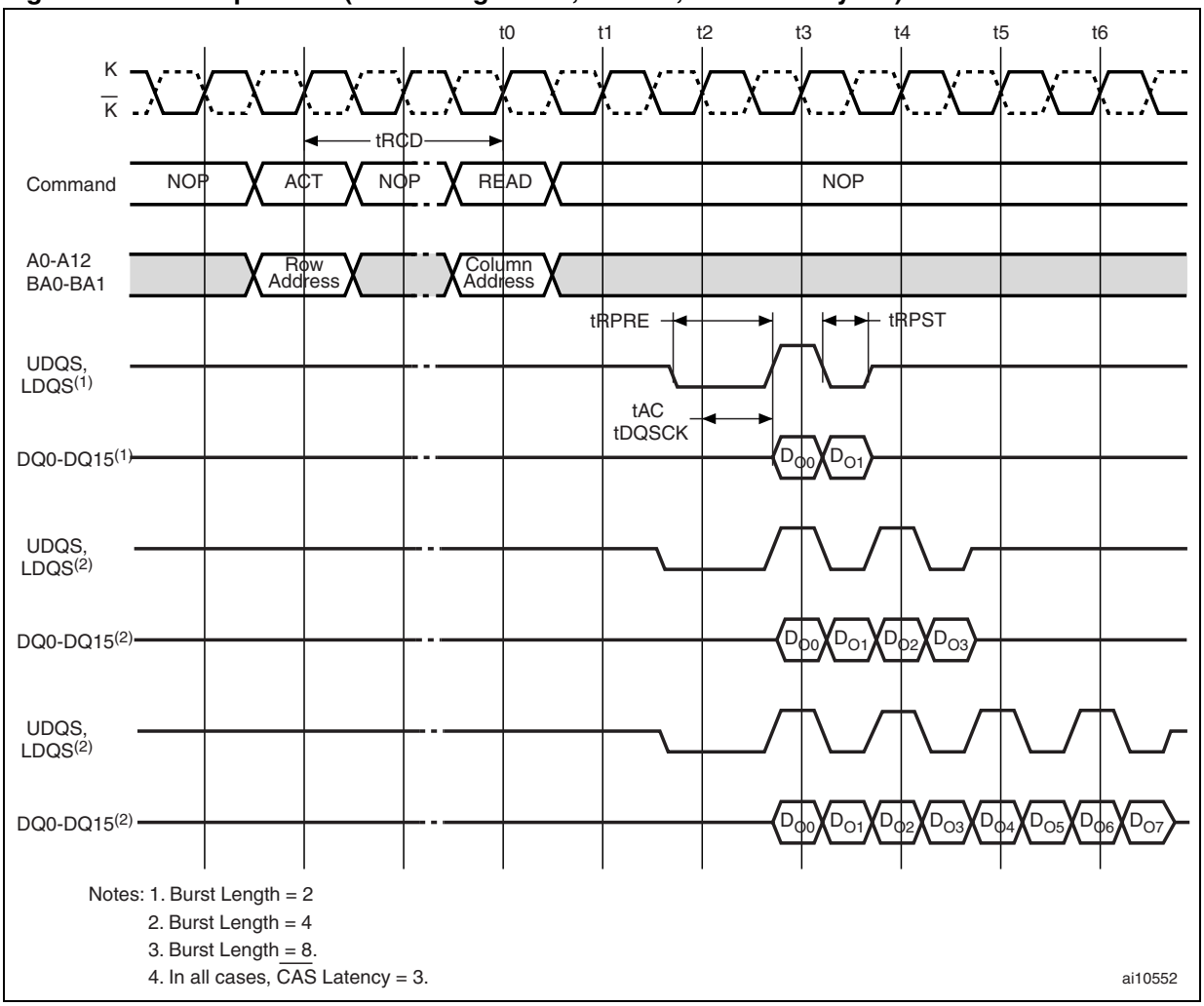


Figure 12. Burst Terminate During Read Operation

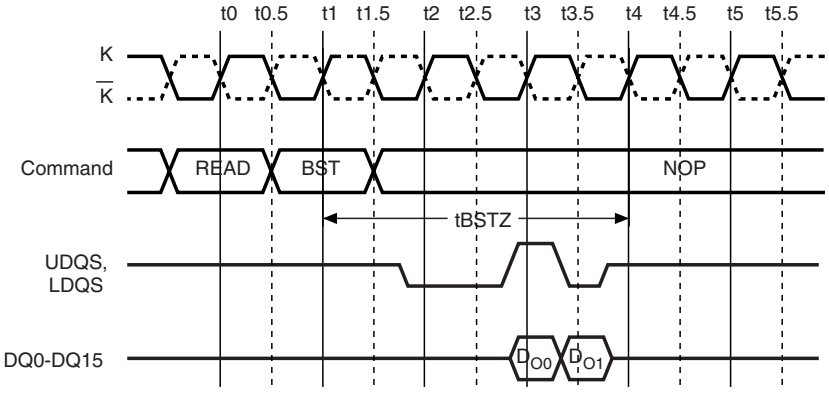
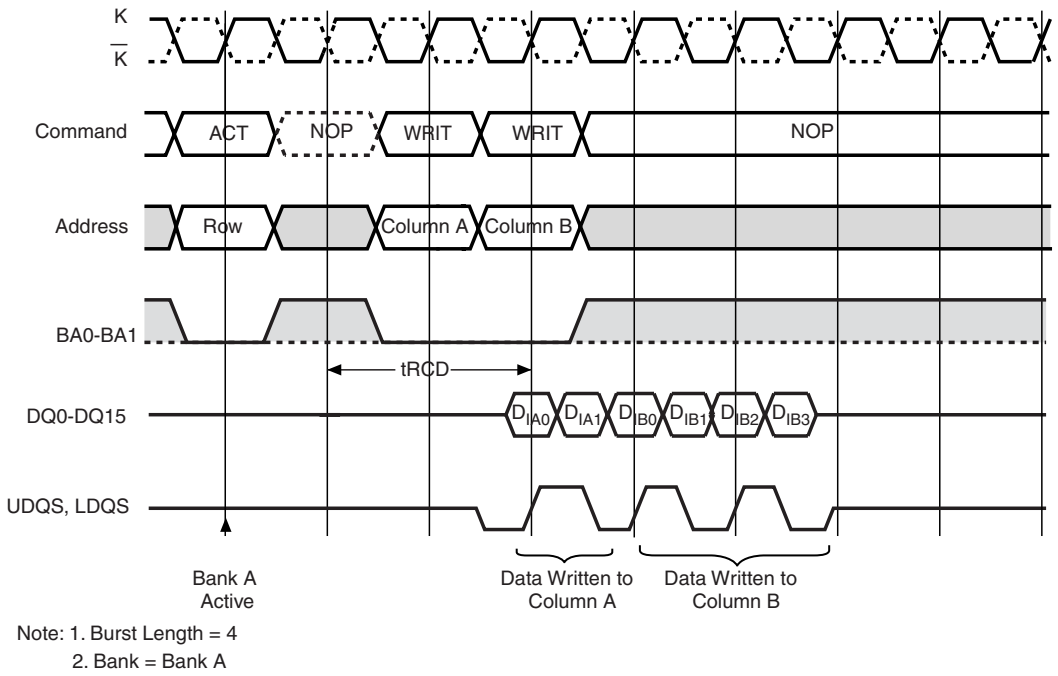
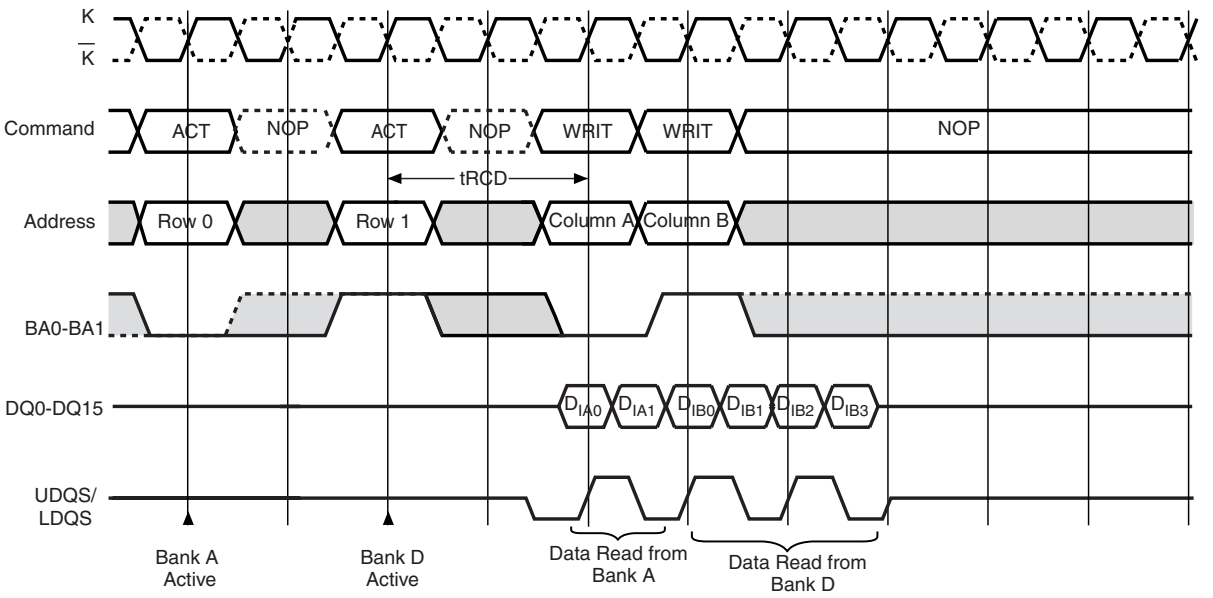


Figure 13. Write followed by Write in Same Bank and Row



1. The consecutive WRIT command must be issued after a minimum delay of t_{CK} to interrupt the previous Write operation.
2. To issue the consecutive WRITE to a different row, precharge the bank (PRE) to interrupt the previous Write operation. t_{RP} after the PRE command, issue the ACT command. The consecutive WRIT command can be issued t_{RCD} after the ACT command.

Figure 14. Write followed by Write in a Different Bank



1. If the consecutive Write operation targets an active row, the second WRIT command must be issued after a minimum delay of t_{CK} to interrupt the previous Write operation.
2. If the consecutive Write operation targets an idle row, precharge the bank (PRE) without interrupting the previous Write operation. t_{RP} after the PRE command, issue the ACT command. The consecutive WRIT command can be issued t_{RCD} after the ACT command.

Figure 15. Write operation with Auto Precharge

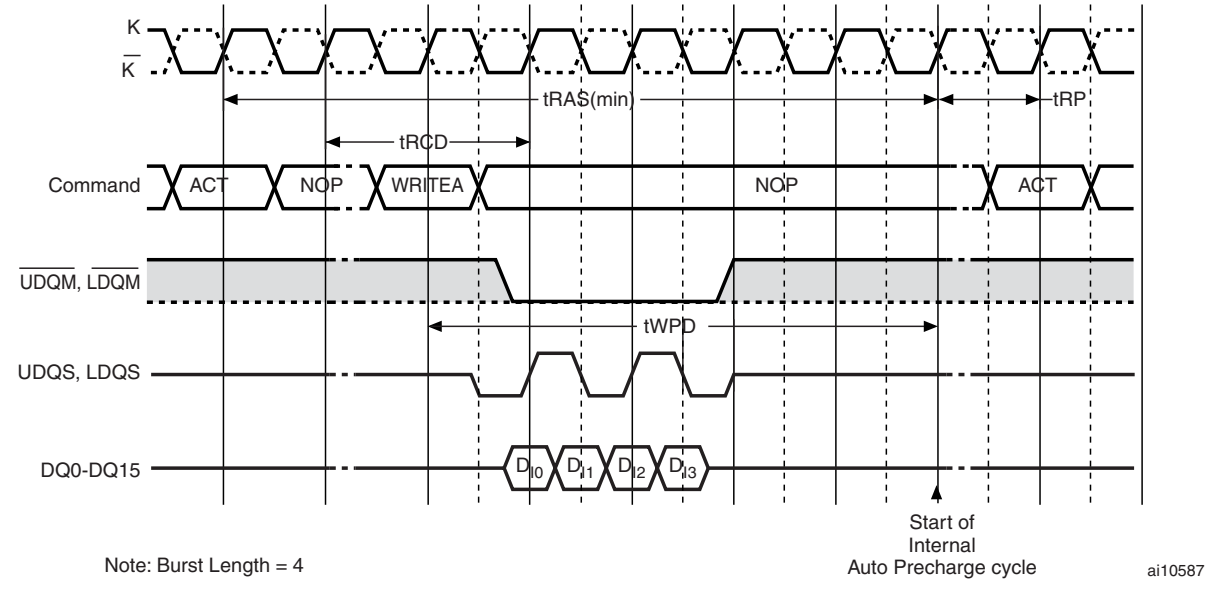
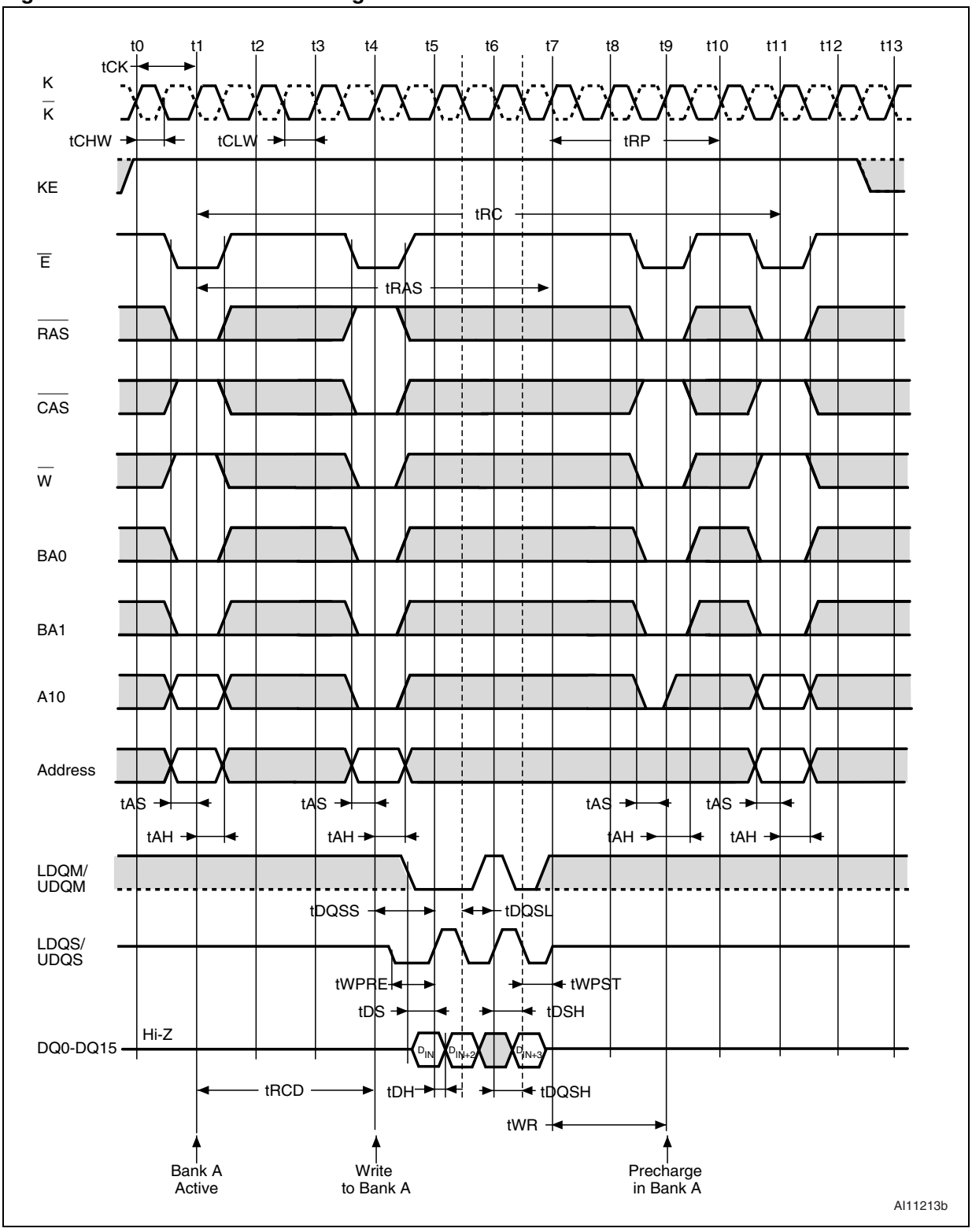


Figure 16. Write with Auto Precharge AC Waveforms



1. Burst Length = 4 Words, $\overline{CAS}$ Latency = 1 clock cycle.

Figure 17. Write Operation (Burst Lengths = 2, 4 and 8, $\overline{CAS}$ Latency = 1)

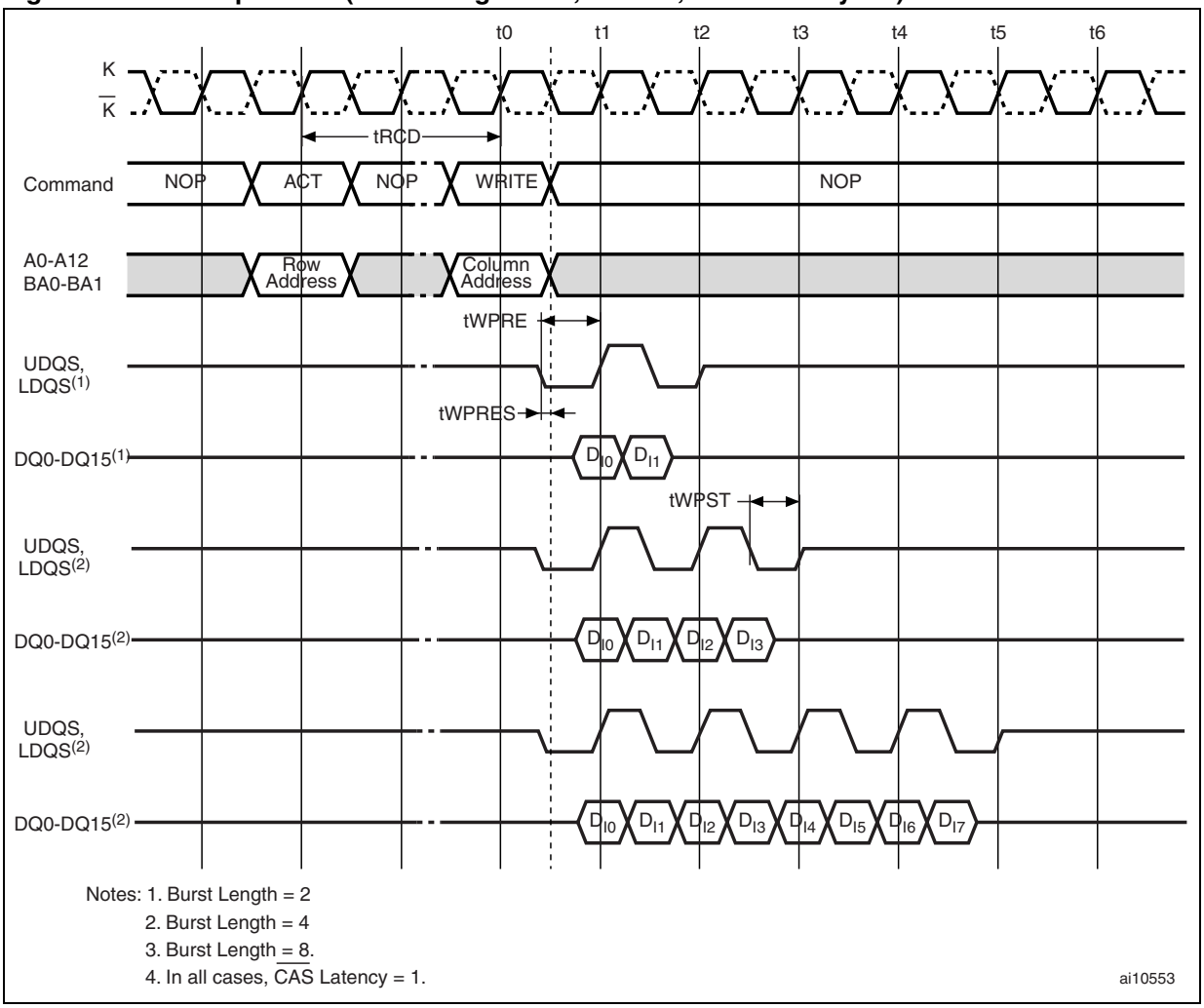
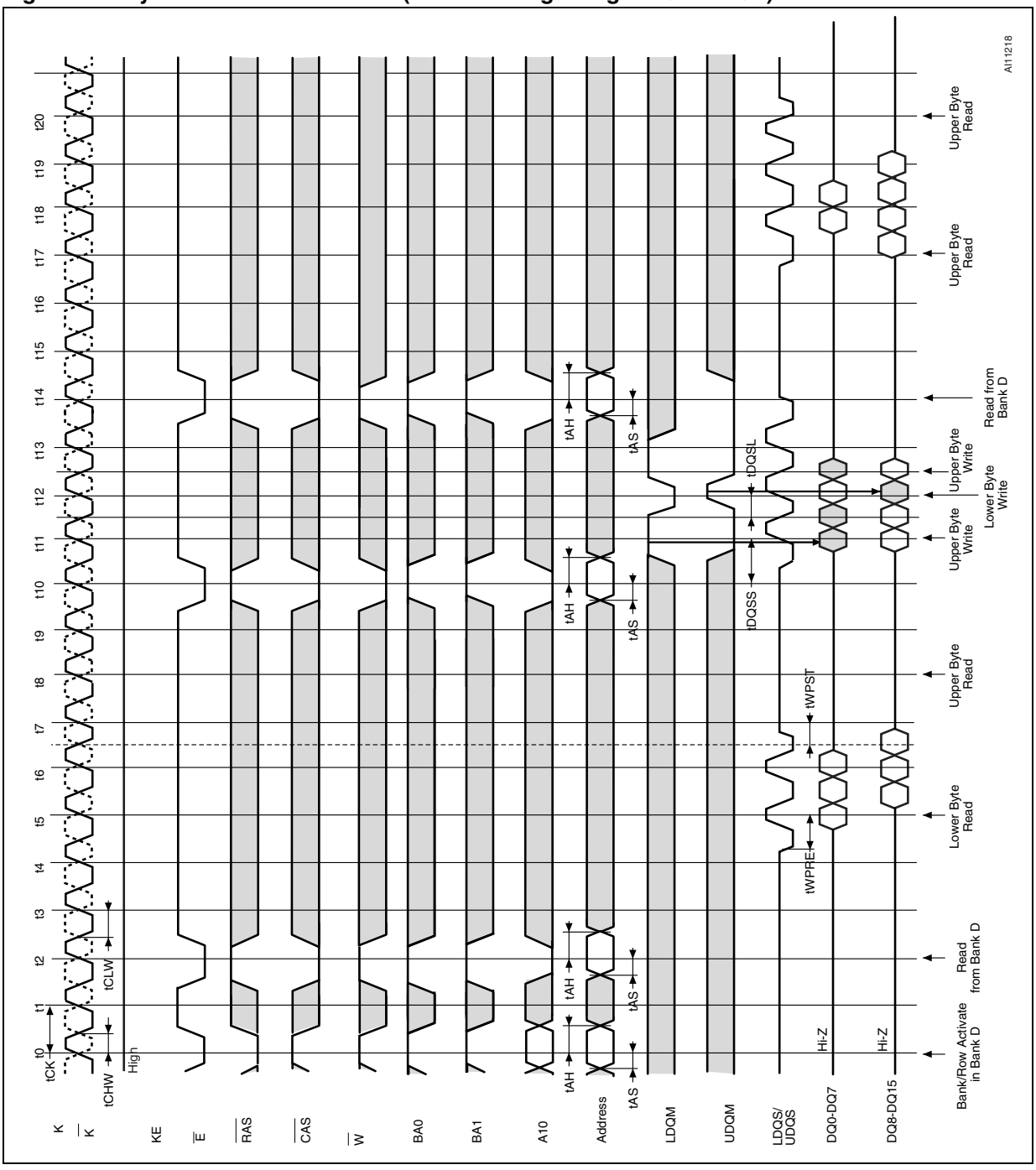
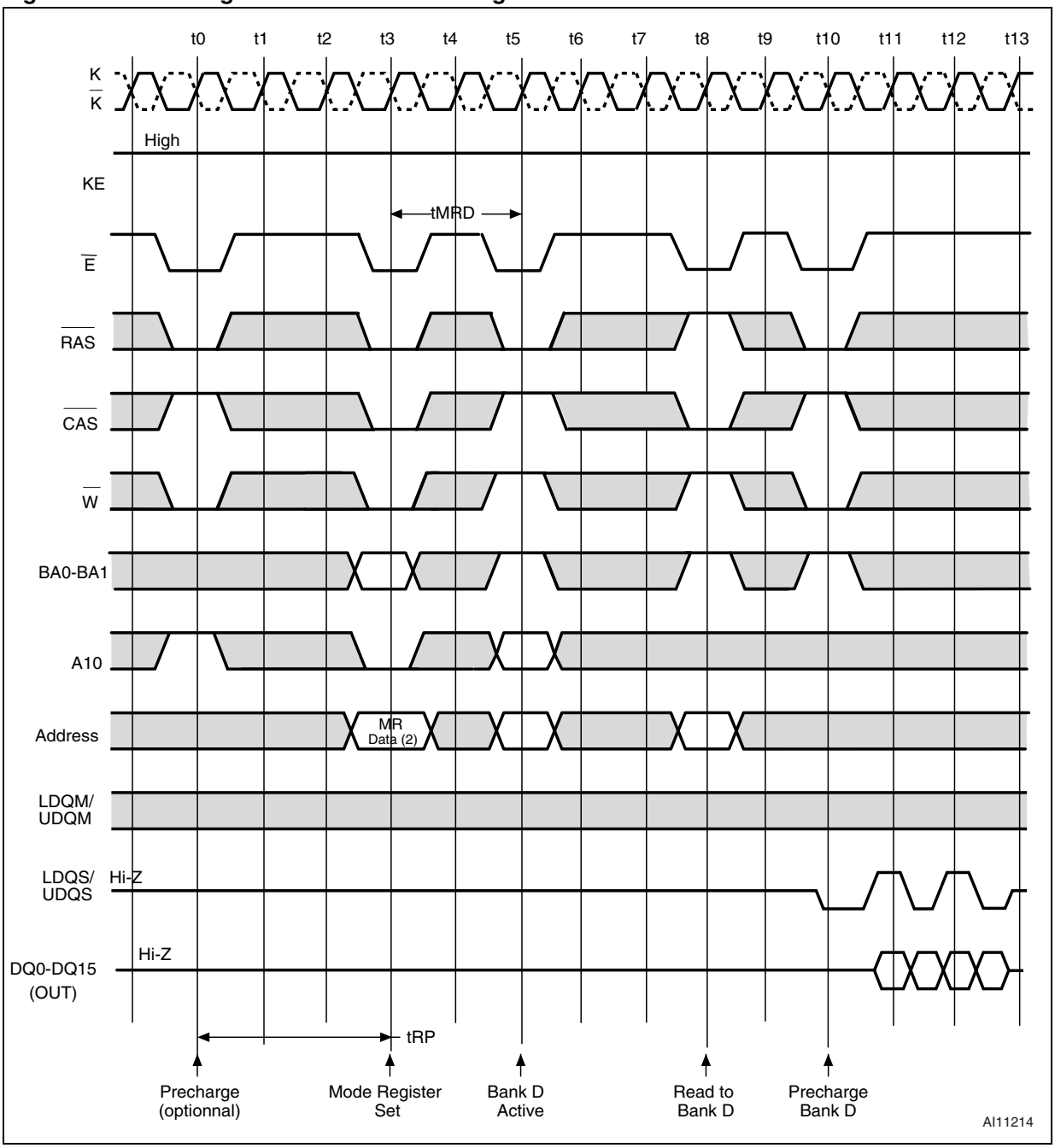


Figure 18. Byte Write AC Waveforms (Data Masking using LDQM/UDQM)



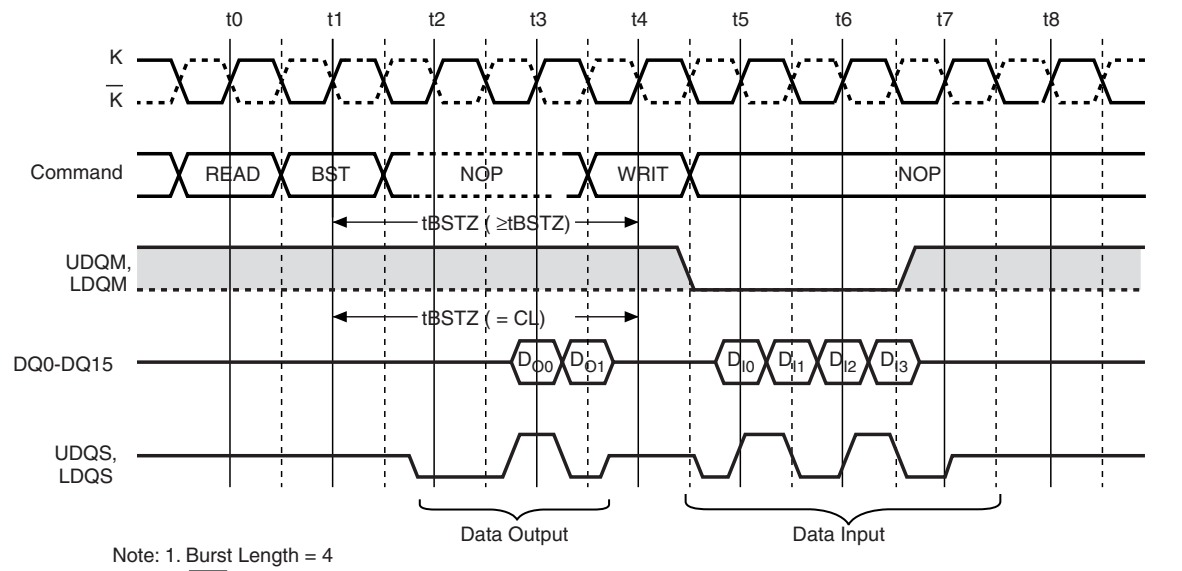
1. Burst Length = 4 Words.

Figure 19. Mode Register/Extended Mode Register Set Commands AC Waveforms



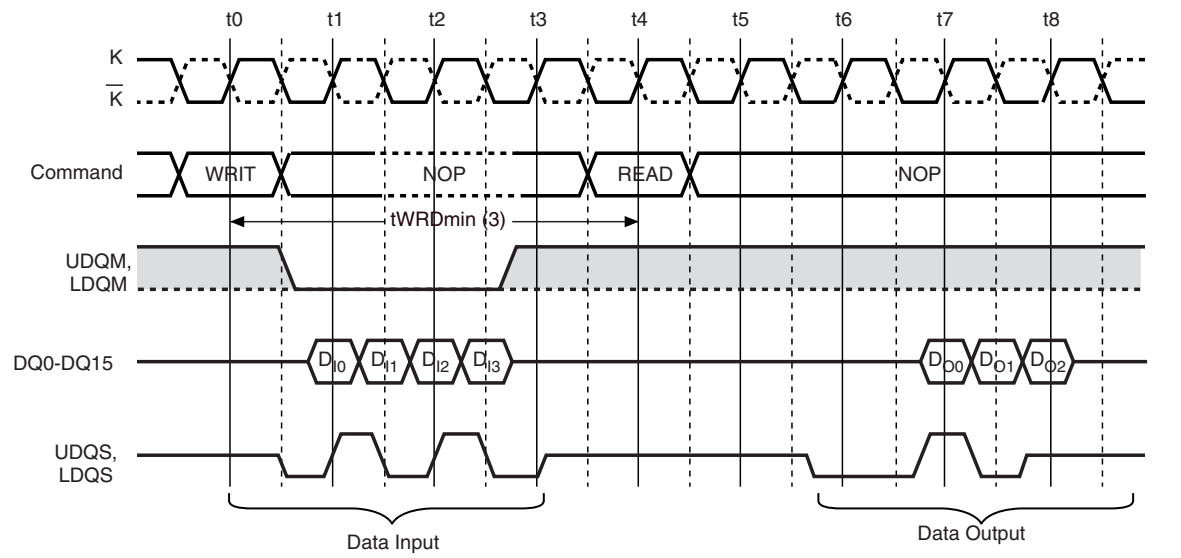
1. To program the Extended Mode Register, BA0 and BA1 must be set to '0' and '1' respectively, and A0 to A11 to the Extended Mode Register Data.
2. MR Data is the value to be written to the Mode Register.

Figure 20. Read followed by Write using the Burst Read Terminate Command (BST)



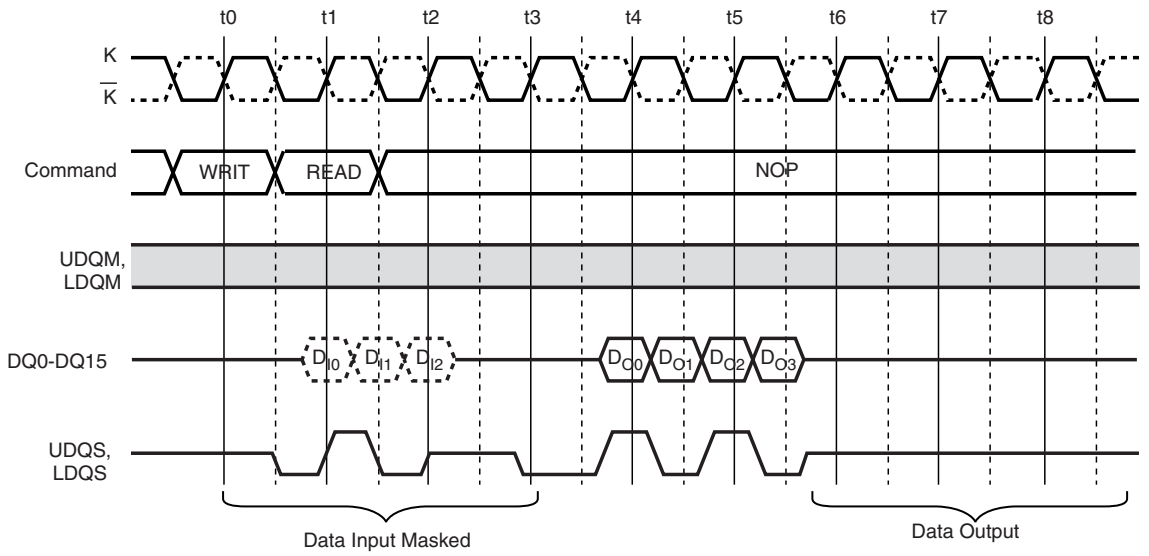
1. If the Write operation is performed to the same bank and row than the Read operation, the Burst Read Terminate command (BST) must be issued to terminate the Read operation.The WRIT command can then be issued t_{BSTW} ($\check{S}t_{BSTW}$) after the BST command.
2. If the Write operation is performed to the same bank but to a different row, the bank must be precharged to interrupt the Read operation. t_{RP} after the Precharge command, issue the ACT command. The WRIT command can then be issued t_{RCD} after the ACT command.
3. If the Write operation is performed to a different bank and to an active row, the sequence is identical to the one described in *Note 1*
4. If the Write operation is performed to a different bank and to an idle row, the bank must be precharged independently from the Read operation. t_{RP} after the Precharge command, issue the ACT command. The WRIT command can then be issued t_{RCD} after the ACT command.

Figure 21. Write followed by Read (Write Completed)



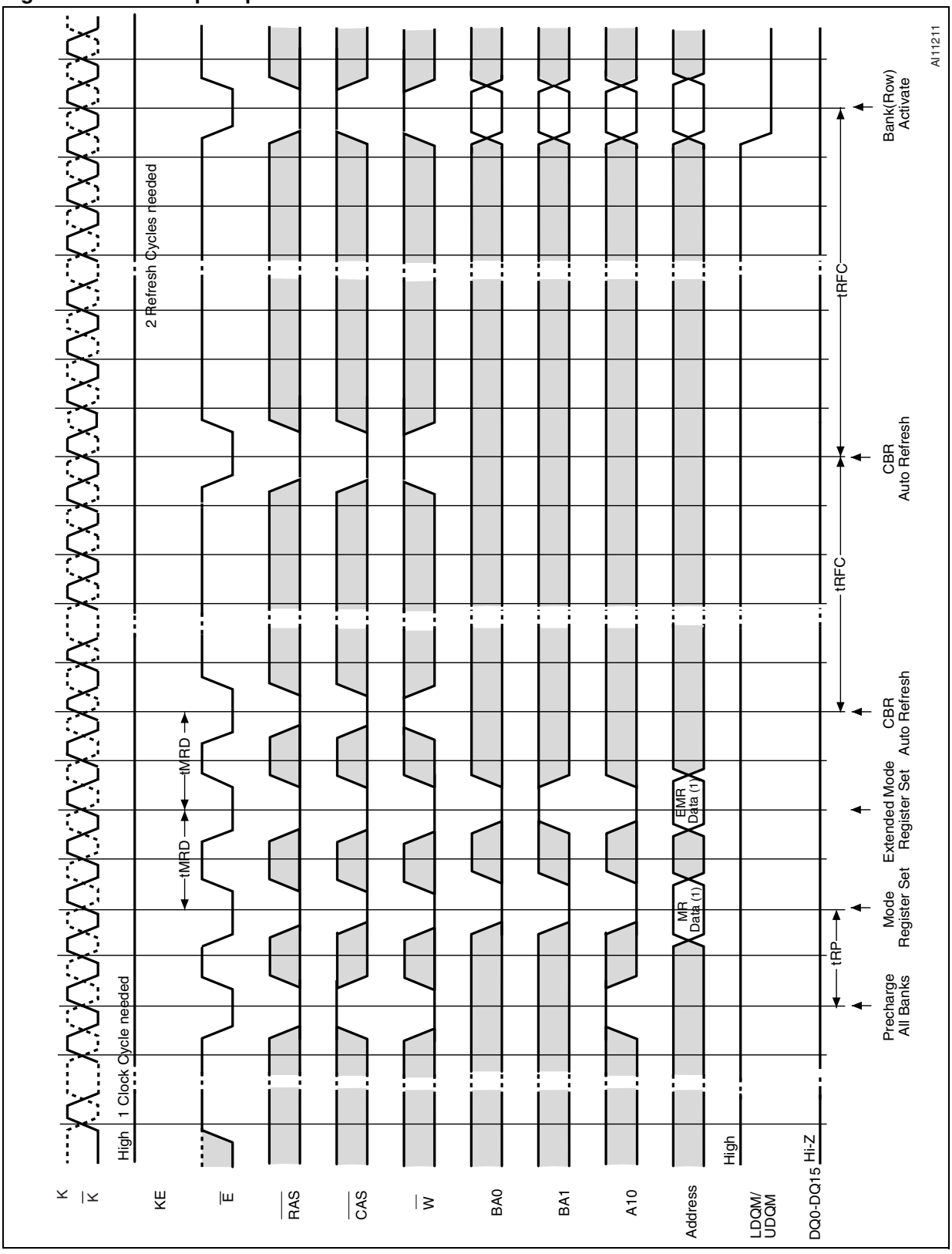
1. If the Read operation is performed to the same bank and row than the Write operation, the READ command should be performed t_{WRD} after the WRIT command to complete the Write operation.
2. If the Read operation is performed to the same bank but to a different row, the bank must be precharged t_{WPD} after the Write operation. t_{RP} after the Precharge command, issue the ACT command. The READ command can then be issued t_{RCD} after the ACT command.
3. If the Read operation is performed to a different bank and to an active row, the sequence is identical to the one described in *Note 1*
4. If the Read operation is performed to a different bank and to an idle row, the bank must be precharged independently from the Write operation. t_{RP} after the Precharge command, issue the ACT command. The WRIT command can then be issued t_{RCD} after the ACT command.

Figure 22. Write followed by Read in the same Bank and Row (Write Interrupted)



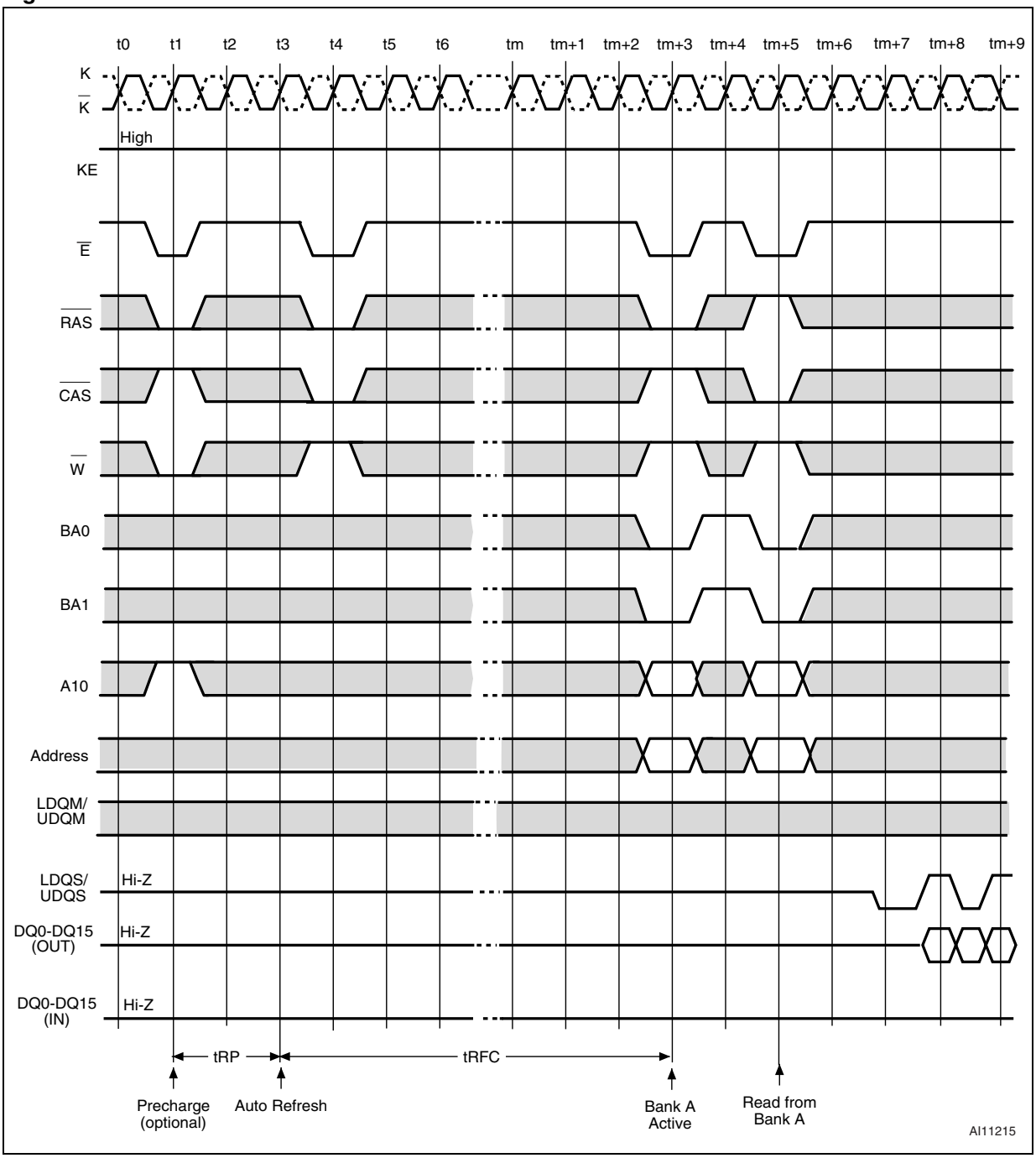
1. UDQM/LDQM must be input 1 clock cycle prior to the READ command to prevent invalid data from being written. If the READ command is input on the next cycle after the WRIT command, UDQM/LDQM are not necessary.
2. If the Read operation is issued to a different row in the same bank, or to an idle row in a different bank, a Precharge command (PRE) must be issued before the READ command. In this case, the Read operation does not interrupt the Write operation.
3. If the Read operation is issued to a different bank, and to an active row, the sequence is identical to the one described in *Note 1*

Figure 23. Power-Up Sequence



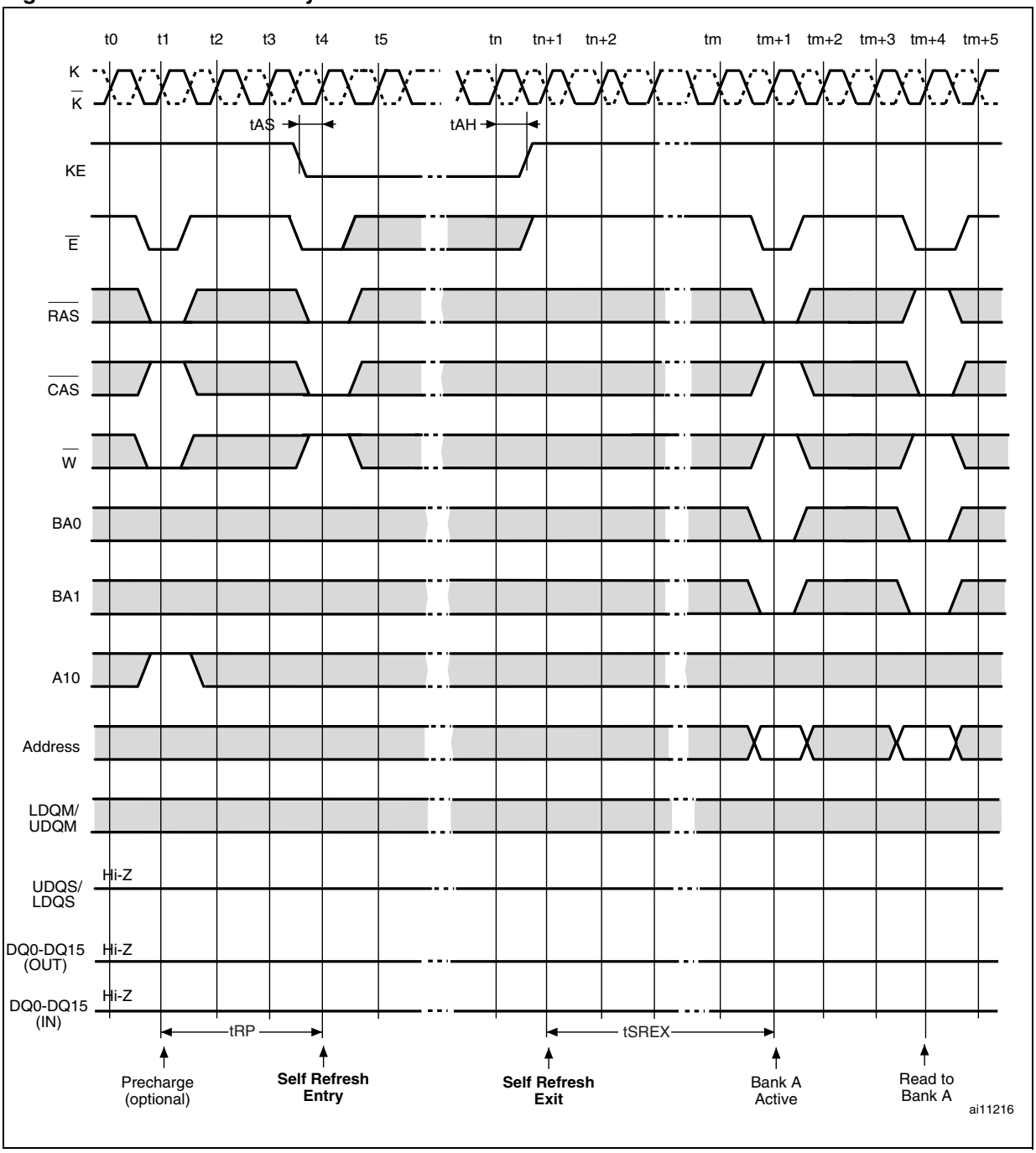
1. MR Data and EMR data are the values to be written to the Mode Register and the Extended Mode Register, respectively.

Figure 24. Auto Refresh Command AC Waveforms



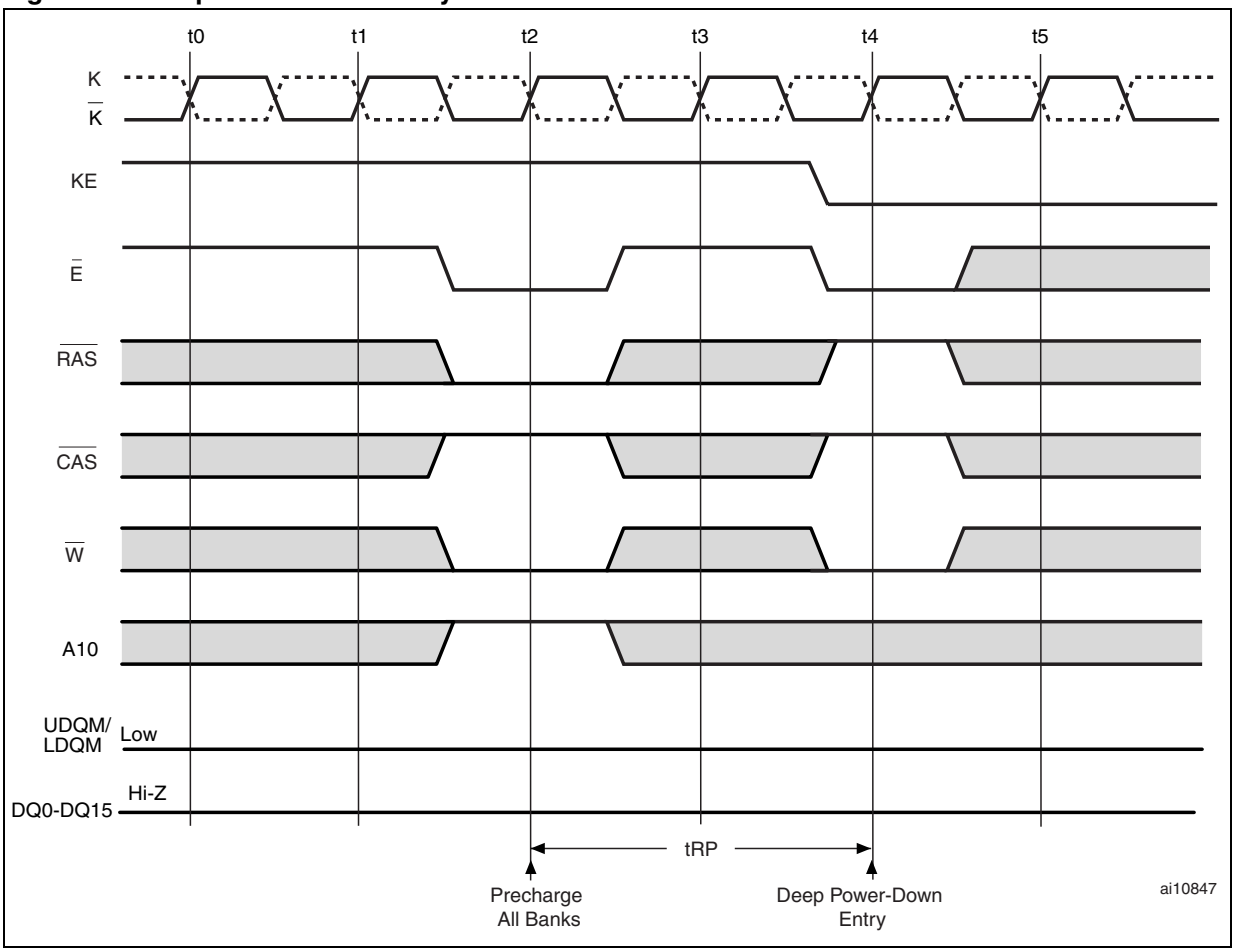
1. Burst Length = 4 Words, $\overline{CAS}$ Latency = 3 clock cycles.

Figure 25. Self Refresh Entry and Exit Commands AC Waveforms



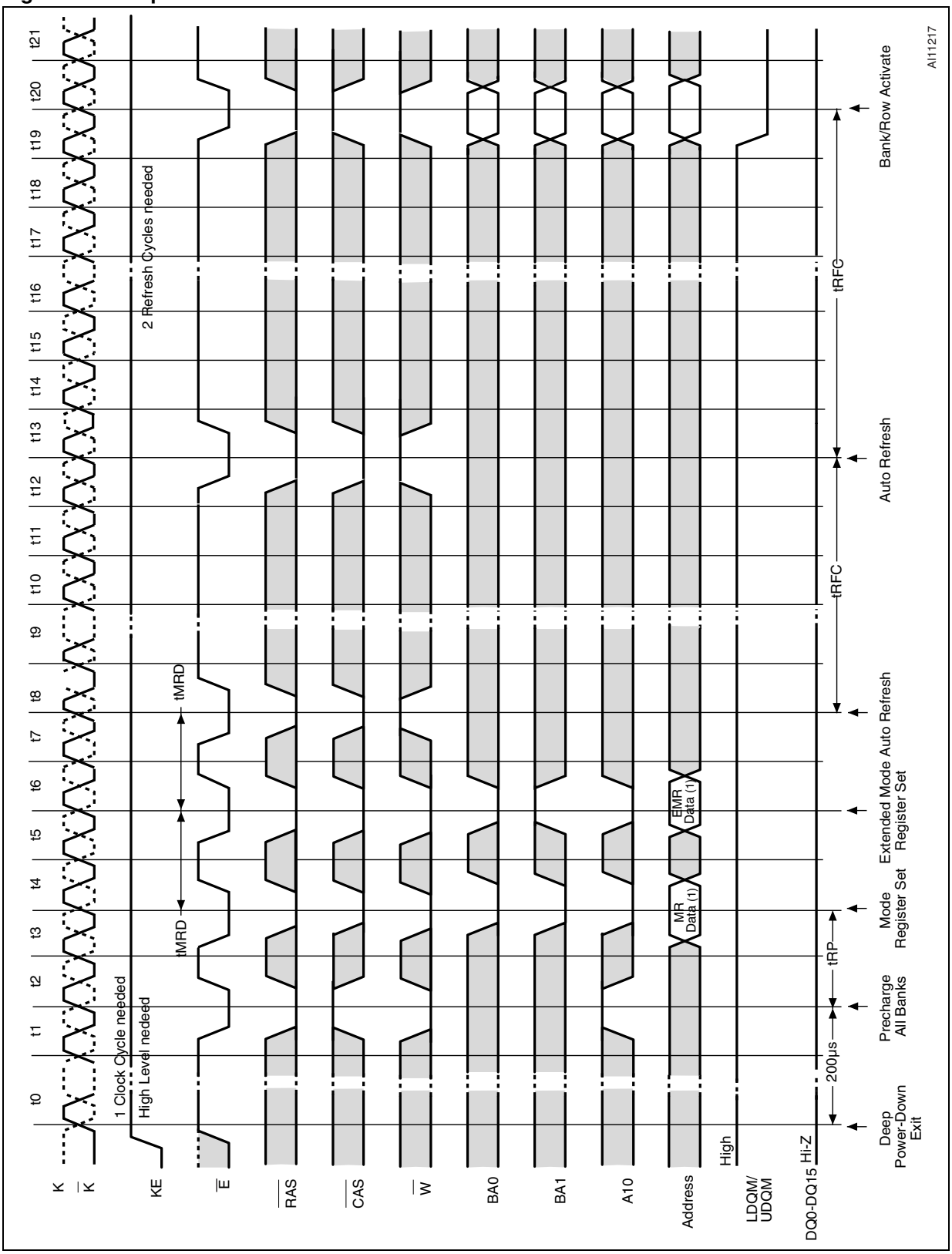
1. Burst Length = 4 Words.

Figure 26. Deep Power-Down Entry Command AC Waveforms



1. BA0, BA1 and address bits A0 to A11 (except A10) are 'Don't Care'. Upper and Lower Data Input Mask signals, UDQM and LDQM are Low, V_{IL}.

Figure 27. Deep Power-Down Exit AC Waveforms



1. MR Data and EMR data are the values to be written to the Mode Register and the Extended Mode Register, respectively.

8 Part numbering

Table 17. Ordering Information Scheme

Example: M65KG256AB 8 W 8

Device Type

M65 = Low-Power SDRAM

Mode

K = Wafer Form

Operating Voltage

G = V_{DD} = V_{DDQ} = 1.8V, DDR LPSDRAM, x16

Array Organization

256 = 4 Banks x 4Mbit x 16

Number of Chip Enable Inputs

A = One Chip Enable

Die Version

B = B-Die

Speed

8 = 7.5ns

Delivery Form

W = Wafer Form

Temperature Range

8 = 30 to 85°C

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

9 Revision history

Date	Revision	Changes
09-Feb-2006	1.0	First Issue.

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