USB 2.0 High/Full Speed Multiplexer

The Intersil ISL54200 dual 2:1 multiplexer IC is a single supply part that can operate from a single 2.7V to 5.5V supply. It contains two SPDT (Single Pole/Double Throw) switches configured as a DPDT. The part was designed for switching between USB High-Speed and USB Full-Speed sources in portable battery powered products.

The 7Ω normally-closed (NC) FSx switches can swing rail-to-rail and were specifically designed to pass USB full speed data signals (12Mbps) that range from 0V to 3.6V. The 4.5Ω normally-open (NO) HSx switches have high bandwidth and low capacitance and were specifically designed to pass USB high speed data signals (480Mbps) with minimal distortion.

The part can be used in Personal Media Players and other portable battery powered devices that need to switch between a high-speed transceiver and a full-speed transceiver while connected to a single USB host (computer).

The digital logic inputs are 1.8V logic compatible when operated with a 2.7V to 3.6V supply. The part has an enable pin to open all switches. It can be used to facilitate proper bus disconnect and connection when switching between the USB sources.

The ISL54200 is available in a 10 Ld 3mmx3mm TDFN and a small 10 Ld 2.1mmx1.6mm µTQFN packages. It operates over a temperature range of -40 to +85°C.

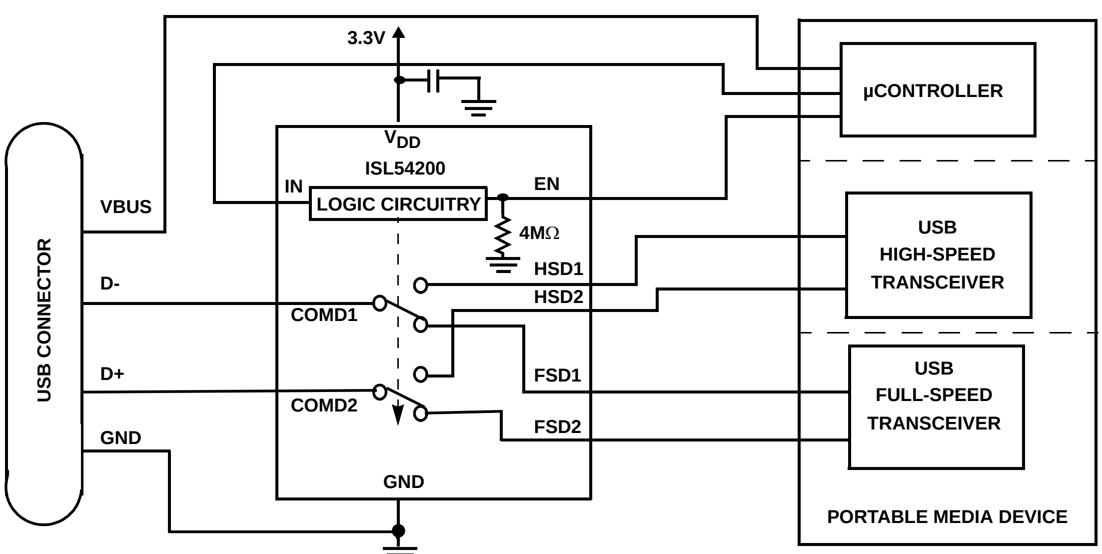
Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- 1.8V Logic Compatible (2.7V to +3.6V supply)
- Enable Pin to Open all Switches
- -3dB Frequency
  - HSx Switches. 880MHz
  - FSx Switches 550MHz
- Crosstalk @ 1MHz. . . . . -70dB
- Off Isolation @ 100kHz . . . . -98dB
- Single Supply Operation (V_{DD}) . . . . 2.7V to 5.5V
- Available in Ultra-thin µTQFN and TDFN Packages
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

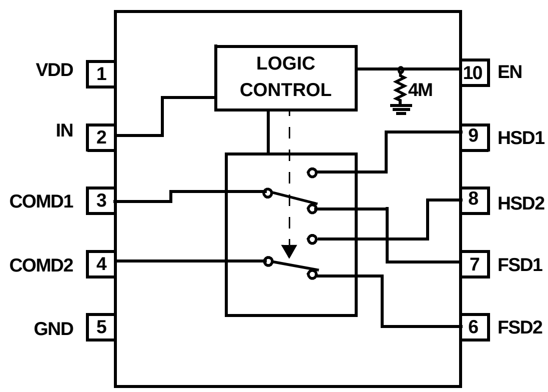
- MP3 and other Personal Media Players
- Cellular/Mobile Phones
- PDA's
- Digital Cameras and Camcorders

Application Block Diagram

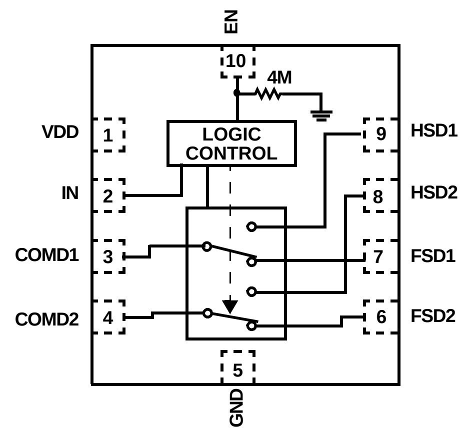


Pinouts

ISL54200
(10 LD TDFN)
TOP VIEW



ISL54200
(10 LD µTQFN)
TOP VIEW



NOTE:

1. ISL54200 Switches Shown for IN = Logic “0” and EN = Logic “1”.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54200IRZ	200Z	-40 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL54200IRZ-T	200Z	-40 to +85	10 Ld 3x3 TDFN Tape and Reel	L10.3x3A
ISL54200IRUZ-T	FM	-40 to +85	10 Ld 2.1mmx1.6mm µTQFN Tape and Reel	L10.2.1x1.6A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Truth Table

ISL54200			
EN	**IN**	**FSD1, FSD2**	**HSD1, HSD2**
1	0	ON	OFF
1	1	OFF	ON
0	X	OFF	OFF
Logic “0” when ≤0.5V, Logic “1” when ≥1.4V with a 2.7V to 3.6V Supply. X = Don’t Care			

Pin Descriptions

ISL54200		
PIN NO.	**NAME**	**FUNCTION**
1	VDD	Power Supply
2	IN	Select Logic Control Input
3	COMD1	USB Common Port
4	COMD2	USB Common Port
5	GND	Ground Connection
6	FSD2	Full Speed USB Differential Port
7	FSD1	Full Speed USB Differential Port
8	HSD2	High Speed USB Differential Port
9	HSD1	High Speed USB Differential Port
10	EN	Bus Switch Enable

Absolute Maximum Ratings

VDD to GND . . . . -0.3V to 6.0V
Input Voltages
FSD2, FSD1, HSD2, HSD1 (Note 2) . . . . . - 1V to ((V_{DD}) +0.3V)
IN, EN (Note 2). . . . . -0.3V to ((V_{DD}) +0.3V)
Output Voltages
COMD1, COMD2 (Note 2) . . . . -1V to 5V
Continuous Current (HSD2, HSD1, FSD2, FSD1). . . . . ±40mA
Peak Current (HSD2, HSD1, FSD2, FSD1)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . ±100mA
ESD Rating:
HBM . . . .>7kV
MM . . . .>400V
CDM . . . . >1.4kV

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
10 Ld 3x3 TDFN Package 55
10 Ld µTQFN Package 140
Maximum Junction Temperature (Plastic Package). . . . . . . +150°C
Maximum Storage Temperature Range . . . . -65°C to +150°C
Pb-free reflow profile . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range
ISL54200IRZ and ISL54200IRUZ . . . . -40°C to +85°C
V_{DD} Supply Voltage Range . . . . 2.7V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. Signals on FSD1, FSD2, HSD1, HSD2, COMD1, COMD2, EN, IN exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{ENH} = 1.4V, V_{ENL} = 0.5V, (Note 4), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
ANALOG SWITCH CHARACTERISTICS						
NC Switches (FSD1, FSD2)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.3V, IN = 0V, EN = 3.3V	Full	0	-	V_{DD}	V
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 0.5V, EN = 1.4V, I_{COMx} = 40mA, V_{FSD1} or V_{FSD2} = 0V to 3.3V, (See Figure 4)	+25	-	7	10	Ω
		Full	-	-	15	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3V, IN = 0.5V, EN = 1.4V, I_{COMx} = 40mA, V_{FSD1} or V_{FSD2} = Voltage at max r_{ON} over signal range of 0V to 3.3V, (Note 8)	+25	-	0.1	0.35	Ω
		Full	-	-	0.4	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.3V, IN = 0.5V, EN = 1.4V, I_{COMx} = 40mA, V_{FSD1} or V_{FSD2} = 0V to 3.3V, (Note 7)	+25	-	4	6	Ω
		Full	-	-	8	Ω
OFF Leakage Current, $I_{FSX(OFF)}$	V+ = 3.6V, IN = 3.6V, EN = 0V and 3.6V, V_{COMx} = 0.3V, 3V, V_{FSX} = 3V, 0.3V	+25	-20	2	20	nA
		Full	-70	-	70	nA
ON Leakage Current, $I_{FSX(ON)}$	V+ = 3.6V, IN = 0V, EN = 3.6V, V_{COMx} = 0.3V, 3V, V_{FSX} = 0.3V, 3V	+25	-20	2	20	nA
		Full	-70	-	70	nA
NO Switches (HSD1, HSD2)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V	Full	0	-	V_{DD}	V
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 1.4V, EN = 1.4V, I_{COMx} = 1mA, V_{HSD2} or V_{HSD1} = 3.3V (See Figure 3)	+25	-	20	30	Ω
		Full	-	-	35	Ω
ON-Resistance, r_{ON}	V_{DD} = 3.3V, IN = 1.4V, EN = 1.4V, I_{COMx} = 40mA, V_{HSD2} or V_{HSD1} = 0V to 400mV (See Figure 3)	+25	-	4.5	6	Ω
		Full	-	-	8	Ω
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.3V, IN = 1.4V, EN = 1.4V, I_{COMx} = 40mA, V_{HSD2} or V_{HSD1} = Voltage at max r_{ON}, Voltage at max r_{ON} over signal range of 0V to 400mV (Note 8)	+25	-	0.01	0.1	Ω
		Full	-	-	0.5	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.3V, IN = 1.4V, EN = 1.4V, I_{COMx} = 40mA, V_{HSD2} or V_{HSD1} = 0V to 400mV, (Note 7)	+25	-	0.4	1	Ω
		Full	-	-	1.5	Ω

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{ENH} = 1.4V, V_{ENL} = 0.5V, (Note 4), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
OFF Leakage Current, $I_{HSD2(OFF)}$ or $I_{HSD1(OFF)}$	V_{DD} = 3.6V, IN = 0V, EN = 0 and 3.6V, V_{COMD1} or V_{COMD2} = 3V, 0.3V, V_{HSD2} or V_{HSD1} = 0.3V, 3V	+25	-20	2	20	nA
		Full	-70	-	70	nA
ON Leakage Current, $I_{HSD2(ON)}$ or $I_{HSD1(ON)}$	V_{DD} = 3.6V, IN = 3.6V, EN = 3.6V, V_{COMD1} or V_{COMD2} = 0.3V, 3.0V, V_{HSD2} or V_{HSD1} = 0.3V, 3.0V	+25	-20	2	20	nA
		Full	-70	-	70	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 3.3V, R_L = 45Ω, C_L = 10pF, (See Figure 1)	+25	-	25	-	ns
Turn-OFF Time, t_{OFF}	V_{DD} = 3.3V, R_L = 45Ω, C_L = 10pF, (See Figure 1)	+25	-	15	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 3.3V, R_L = 45Ω, C_L = 10pF, (See Figure 2)	+25	-	7	-	ns
Skew, t_{SKEW} (HSx Switch)	V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V, R_L = 45Ω, C_L = 10pF, $t_R = t_F$ = 720ps at 480Mbps, (Duty Cycle = 50%) (See Figure 7)	+25	-	50	-	ps
Total Jitter, t_J (HSx Switch)	V_{DD} =3.3V, IN = 3.3V, EN = 3.3V, R_L = 45Ω, C_L = 10pF, $t_R = t_F$ = 720ps at 480Mbps	+25	-	210	-	ps
Propagation Delay, t_{PD} (HSx Switch)	V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V, R_L = 45Ω, C_L = 10pF, (See Figure 7)	+25	-	250	-	ps
Skew, t_{SKEW} (FSx Switch)	V_{DD} = 3.3V, IN = 0V, EN = 3.3V, R_L = 39Ω, C_L = 50pF, $t_R = t_F$ = 12ns at 12Mbps, (Duty Cycle = 50%) (See Figure 7)	+25	-	0.15	-	ns
Rise/Fall Time Mismatch, t_M (FSx Switch)	V_{DD} = 3.3V, IN = 0V, EN = 3.3V, R_L = 39Ω, C_L = 50pF, $t_R = t_F$ = 12ns at 12Mbps, (Duty Cycle = 50%)	+25	-	10	-	%
Total Jitter, t_J (FSx Switch)	V_{DD} = 3.3V, IN = 0V, EN = 3.3V, R_L = 39Ω, C_L = 50pF, $t_R = t_F$ = 12ns at 12Mbps	+25	-	1.6	-	ns
Propagation Delay, t_{PD} (FSx Switch)	V_{DD} = 3.3V, IN = 0V, EN = 3.3V, R_L = 39Ω, C_L = 50pF, (See Figure 7)	+25	-	0.9	-	ns
Crosstalk	V_{DD} = 3.3V, R_L = 45Ω, f = 1MHz (See Figure 6)	+25	-	-70	-	dB
Off Isolation	V_{DD} = 3.3V, R_L = 45Ω, f = 100kHz	+25	-	-98	-	dB
FSx Switch -3dB Bandwidth	Signal = -10dBm, 1.0VDC offset, R_L = 45Ω, C_L = 5pF	+25	-	550	-	MHz
HSx Switch -3dB Bandwidth	Signal = -10dBm, 0.2VDC offset, R_L = 45Ω, C_L = 5pF	+25	-	880	-	MHz
HSx OFF Capacitance, C_{HSxOFF}	f = 1MHz, V_{DD} = 3.3V, IN = 0V, EN = 3.3V, V_{HSD1} or V_{HSD2} = V_{COMx} = 0V, (See Figure 5)	+25	-	6	-	pF
FSx OFF Capacitance, C_{FSxOFF}	f = 1MHz, V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V, V_{FSD1} or V_{FSD2} = V_{COMx} = 0V, (See Figure 5)	+25	-	9	-	pF
COM ON Capacitance, $C_{COMX(ON)}$	f = 1MHz, V_{DD} = 3.3V, IN = 3.3V, EN = 3.3V, V_{HSD1} or V_{HSD2} = V_{COMx} = 0V, (See Figure 5)	+25	-	12	-	pF
COM ON Capacitance, $C_{COMX(ON)}$	f = 1MHz, V_{DD} = 3.3V, IN = 0V, EN = 3.3V, V_{FSD1} or V_{FSD2} = V_{COMx} = 0V, (See Figure 5)	+25	-	15	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	2.7	-	5.5	V
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, IN = 0V or 3.6V, EN = 0V or 3.6V	+25	-	20	60	nA
		Full	-	-	80	nA

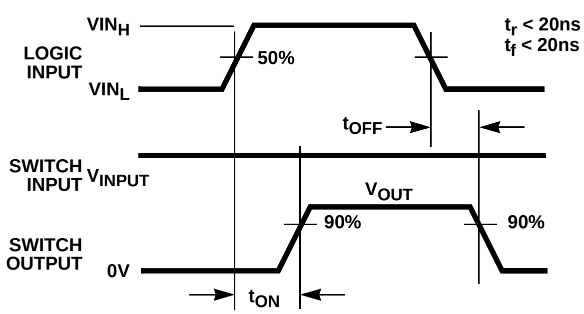
Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{ENH} = 1.4V, V_{ENL} = 0.5V, (Note 4), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 6)	TYP	MAX (Notes 5, 6)	UNITS
DIGITAL INPUT CHARACTERISTICS						
Input Voltage Low, V_{INL}, V_{ENL}	V_{DD} = 2.7V to 3.6V	Full	-	-	0.5	V
Input Voltage High, V_{INH}, V_{ENH}	V_{DD} = 2.7V to 3.6V	Full	1.4	-	-	V
Input Current, I_{INL}, I_{ENL}	V_{DD} = 3.6V, IN = 0V, EN = 0V	Full	-	10	-	nA
Input Current, I_{INH}	V_{DD} = 3.6V, IN = 3.6	Full	-	10	-	nA
Input Current, I_{ENH}	V_{DD} = 3.6V, EN = 3.6	Full	-	1	-	µA

NOTES:

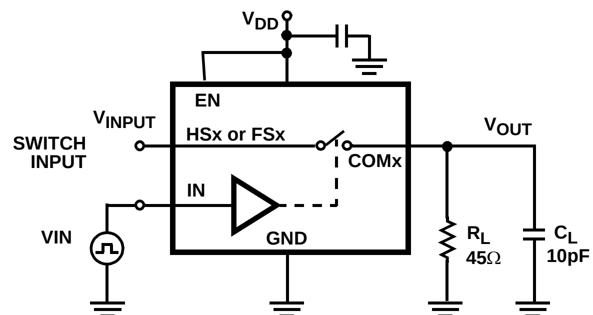
4. V_{LOGIC} = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.
7. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
8. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value, between HSD2 and HSD1 or between FSD2 and FSD1.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)}\frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

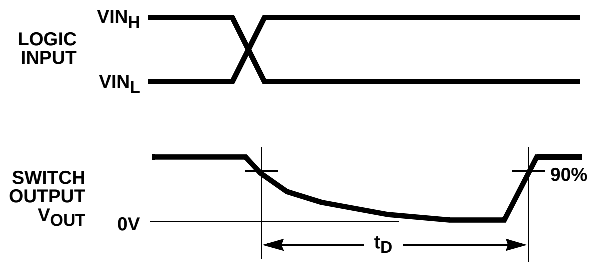
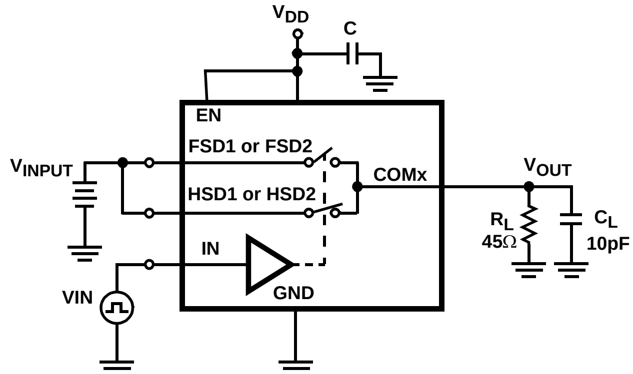


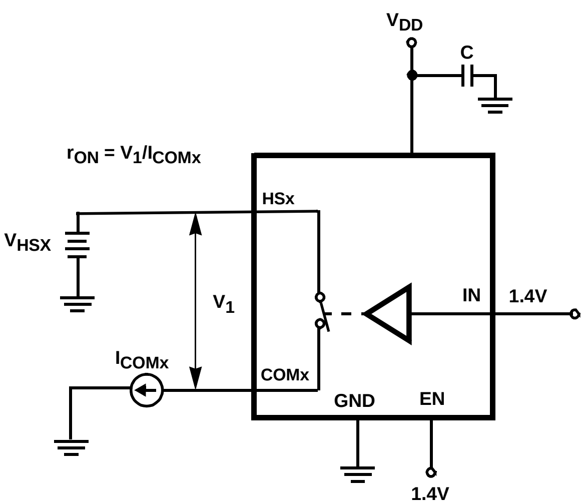
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

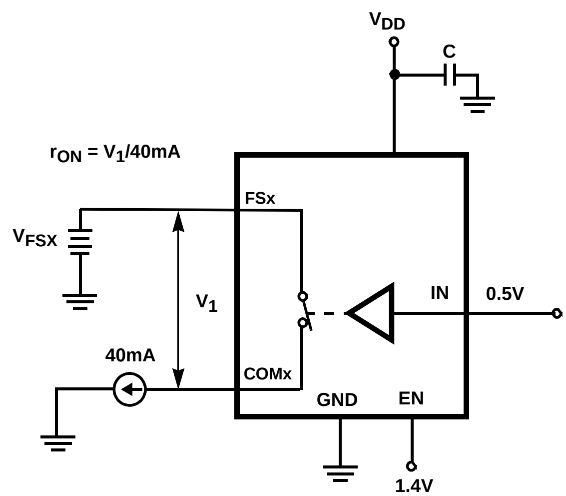
FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

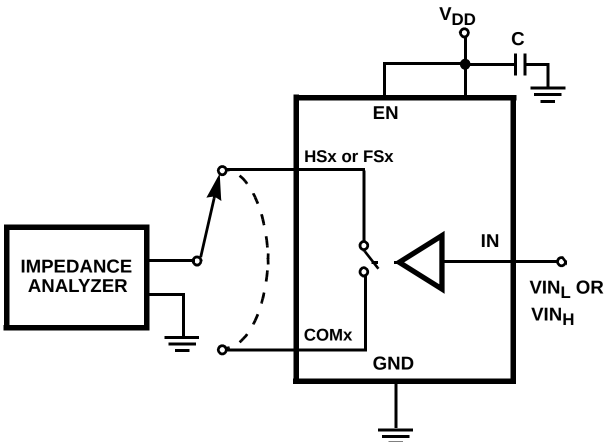
FIGURE 3. HSx SWITCH r_{ON} TEST CIRCUIT



Repeat test for all switches.

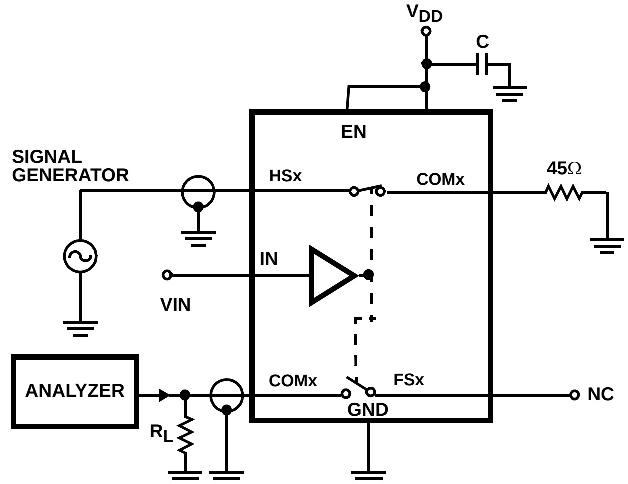
FIGURE 4. FSx SWITCH r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 5. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. CROSSTALK TEST CIRCUIT

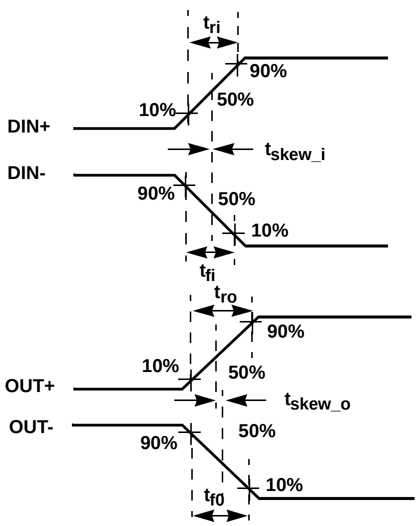
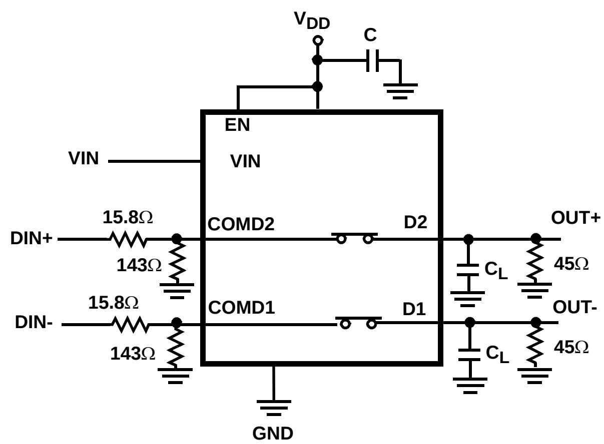


FIGURE 7A. MEASUREMENT POINTS



|tro-tri| Delay Due to Switch for Rising Input and Rising Output Signals.

|tfo-tfi| Delay Due to Switch for Falling Input and Falling Output Signals.

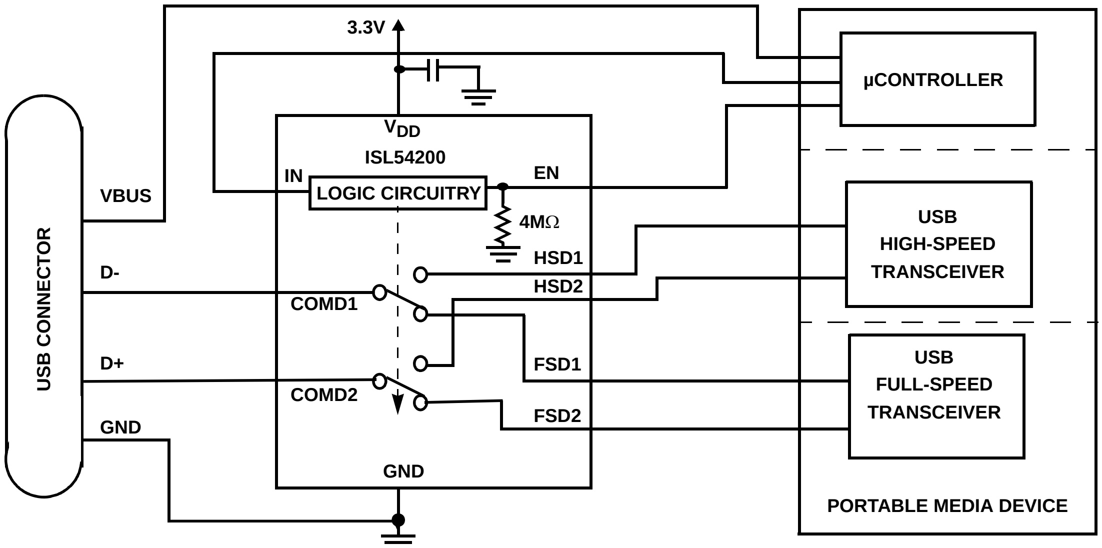
|tskew_0| Change in Skew through the Switch for Output Signals.

|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 7B. TEST CIRCUIT

FIGURE 7. SKEW TEST

Application Block Diagram



Detailed Description

The ISL54200 device is a dual single pole/double throw (SPDT) analog switch that operates from a single DC power supply in the range of 2.7V to 5.5V. It was designed to function as a dual 2-to-1 multiplexer to select between a USB high-speed transceiver and a USB full-speed transceiver in portable battery powered products. It is offered in a TDFN package and a small µTQFN package for use in MP3 players, cameras, PDAs, cellphones, and other personal media players. The device has an enable pin to open all switches.

The part consists of two 7Ω full speed (FSx) switches and two 4.5Ω high speed (HSx) switches. The FSx switches can swing from 0V to V_{DD}. They were designed to pass USB full speed (12Mbps) differential data signals with minimal distortion. The HSx switches have high bandwidth and low capacitance to pass USB high-speed (480Mbps) differential data signals with minimal edge and phase distortion.

The ISL54200 was designed for MP3 players, cameras, cellphones, and other personal media player applications that have both high-speed and full-speed transceivers and need to multiplex between these USB sources to a single USB host (computer). A typical application block diagram of this functionality is shown on page 8.

A detailed description of the two types of switches are provided in the following sections.

FSx Switches (FSD1, FSD2)

The two FSx switches (FSD1, FSD2) are bidirectional switches that can pass rail-to-rail signals. When powered with a 3.3V supply, these switches have a nominal r_{ON} resistance of 7Ω over the signal range of 0V to 3.3V. They were specifically designed to pass USB full-speed (12Mbps) differential signals and meet the USB 2.0 full-speed signal quality specifications. See Figure 8.

The FSx switches can also pass USB high speed signals (480Mbps) but do not quite meet the USB 2.0 high speed signal quality eye diagram compliance requirement.

The maximum signal range for the FSx switches is from -1.5V to V_{DD}. The signal voltage should not be allowed to exceed the V_{DD} voltage rail or go below ground by more than -1.5V.

When operated with a 2.7V to 3.6V supply, the FSx switches are active (turned ON) whenever the IN logic control voltage is ≤0.5V and the EN logic voltage ≥1.4V.

HSx Switches (HSD1, HSD2)

The two HSx switches (HSD2, HSD1) are bi-directional switches that can pass rail-to-rail signals. When powered with a 3.3V supply, these switches have a nominal r_{ON} of 4.5Ω over the signal range of 0V to 400mV with a r_{ON} flatness of 0.4Ω. The r_{ON} matching between the HSD1 and HSD2 switches over this signal range is only 0.01Ω, ensuring minimal impact by the switches to USB high speed signal transitions. As the signal level increases, the r_{ON} switch resistance increases. At signal level of 3.3V, the switch resistance is nominally 20Ω.

The HSx switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high speed signal quality specifications. See Figures 9 and 10.

The HSx switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See Figure 11.

The maximum signal range for the HSx switches is from -1.5V to V_{DD}. The signal voltage should not be allow to exceed the V_{DD} voltage rail or go below ground by more than -1.5V.

The HSx switches are active (turned ON) whenever the IN voltage is ≥1.4V and the EN logic voltage ≥1.4V when operated with a 2.7V to 3.6V supply.

ISL54200 Operation

The discussion that follows will discuss using the ISL54200 in the typical application shown in the“Application Block Diagram” on page 8.

POWER

The power supply connected at the VDD (pin 1) provides the DC bias voltage required by the ISL54200 part for proper operation. The ISL54200 can be operated with a VDD voltage in the range of 2.7V to 5.5V. When used in a USB application, the VDD voltage should be kept in the range of 3.0V to 5.5V to ensure you get the proper signal levels for good signal quality.

A 0.01µF or 0.1µF decoupling capacitor should be connected from the VDD pin to ground to filter out any power supply noise from entering the part. The capacitor should be located as close to the VDD pin as possible.

LOGIC CONTROL

The state of the ISL54200 device is determined by the voltage at the IN pin (pin 2) and the EN pin (pin 10). IN is only active when the EN pin is logic “1” (High). Refer to the “Truth Table” on page 2.

The EN pin is internally pulled low through a 4MΩ resistor to ground. For logic “0” (Low) it can be driven low or allowed to Float. The IN pin must be driven low or high and cannot be left floating.

Logic control voltage levels:

EN = Logic “0” (Low) when V_{EN} ≤0.5V or Floating.
EN = Logic “1” (High) when V_{EN} ≥1.4V
IN = Logic “0” (Low) when V_{IN} ≤0.5V.
IN = Logic “1” (High) when V_{IN} ≥1.4V

Full-speed Mode

If the IN pin = Logic “0” and the EN pin = Logic “1”, the part will be in the full-speed mode. In this mode, the FSD1 and FSD2 switches are ON and the HSD1 and HSD2 switches are OFF (high impedance). In a typical application, V_{DD} will be in the range of 2.8V to 3.6V and will be connected to the battery or LDO of the portable media device. When a computer or USB hub is plugged into the common USB connector and the part is in the full-speed mode, a link will be established between the full-speed driver section of the media player and the computer. The device will be able to transmit and receive data from the computer at a data rate of 12Mbps.

High-speed Mode

If the IN pin = Logic “1” and the EN pin = Logic “1”, the part will go into high-speed mode. In high-speed mode, the HSD1 and HSD2 switches are ON and the FSD1 and FSD2 switches are OFF (high impedance). When a USB cable from a computer or USB hub is connected at the common USB connector and the part is in the high-speed mode, a link will be established between the high-speed driver section of the media player and the computer. The device will be able to transmit and receive data from the computer at a data rate of 480Mbps.

All Switches OFF Mode

If the IN pin = Logic “0” or Logic “1” and the EN pin = Logic “0”, all of the switches will turn OFF (high impedance).

The all OFF state can be used to switch between the two USB sections of the media player. When disconnecting from one USB device to the other USB device, you can momentarily put the ISL54200 switch in the “all off” state in order to get the computer to disconnect from the one device so it can properly connect to the other USB device when that channel is turned ON.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

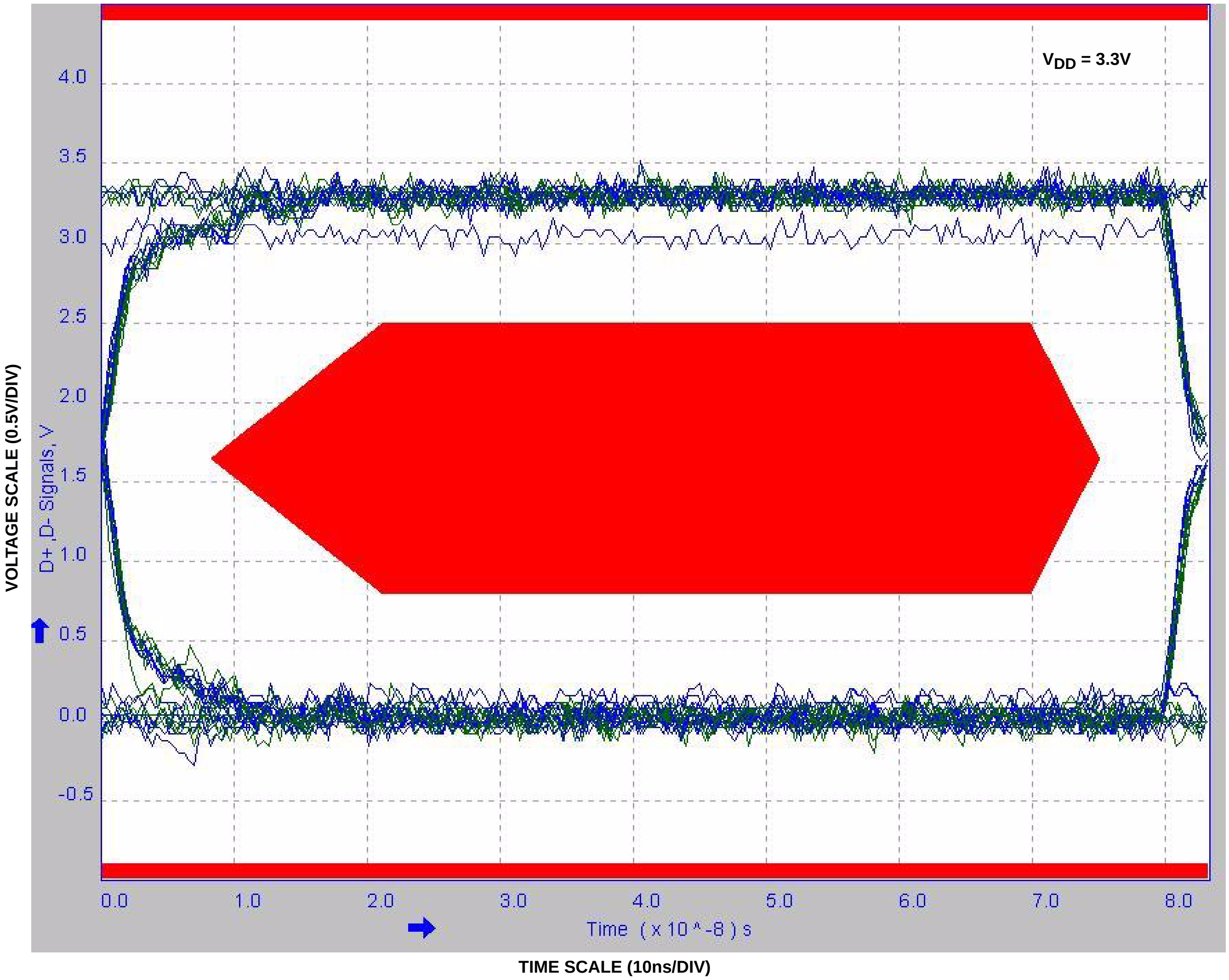


FIGURE 8. EYE PATTERN: 12MBPS USB SIGNAL WITH FSx SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

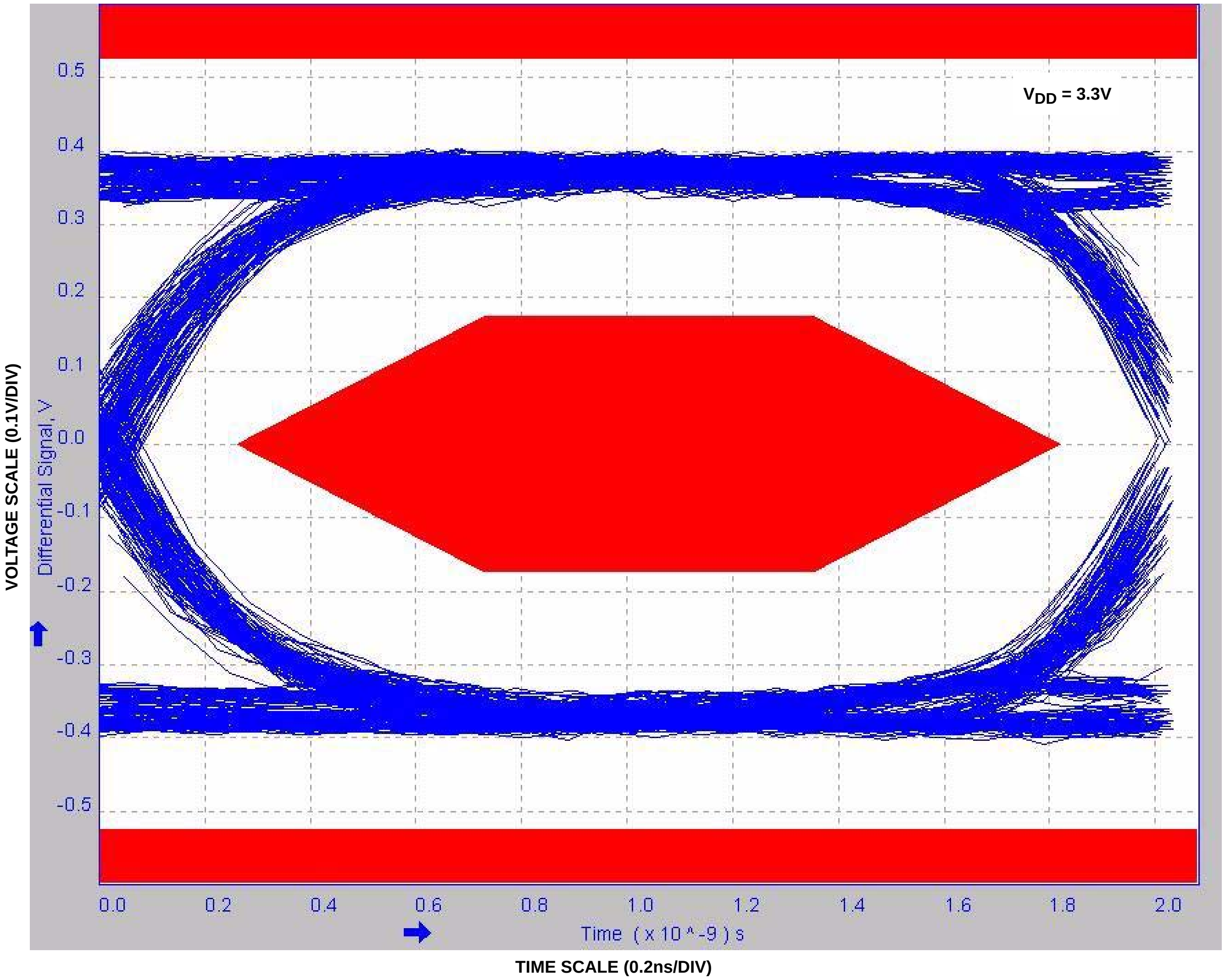


FIGURE 9. EYE PATTERN WITH FAR END MASK: 480MBPS USB SIGNAL WITH HSx SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

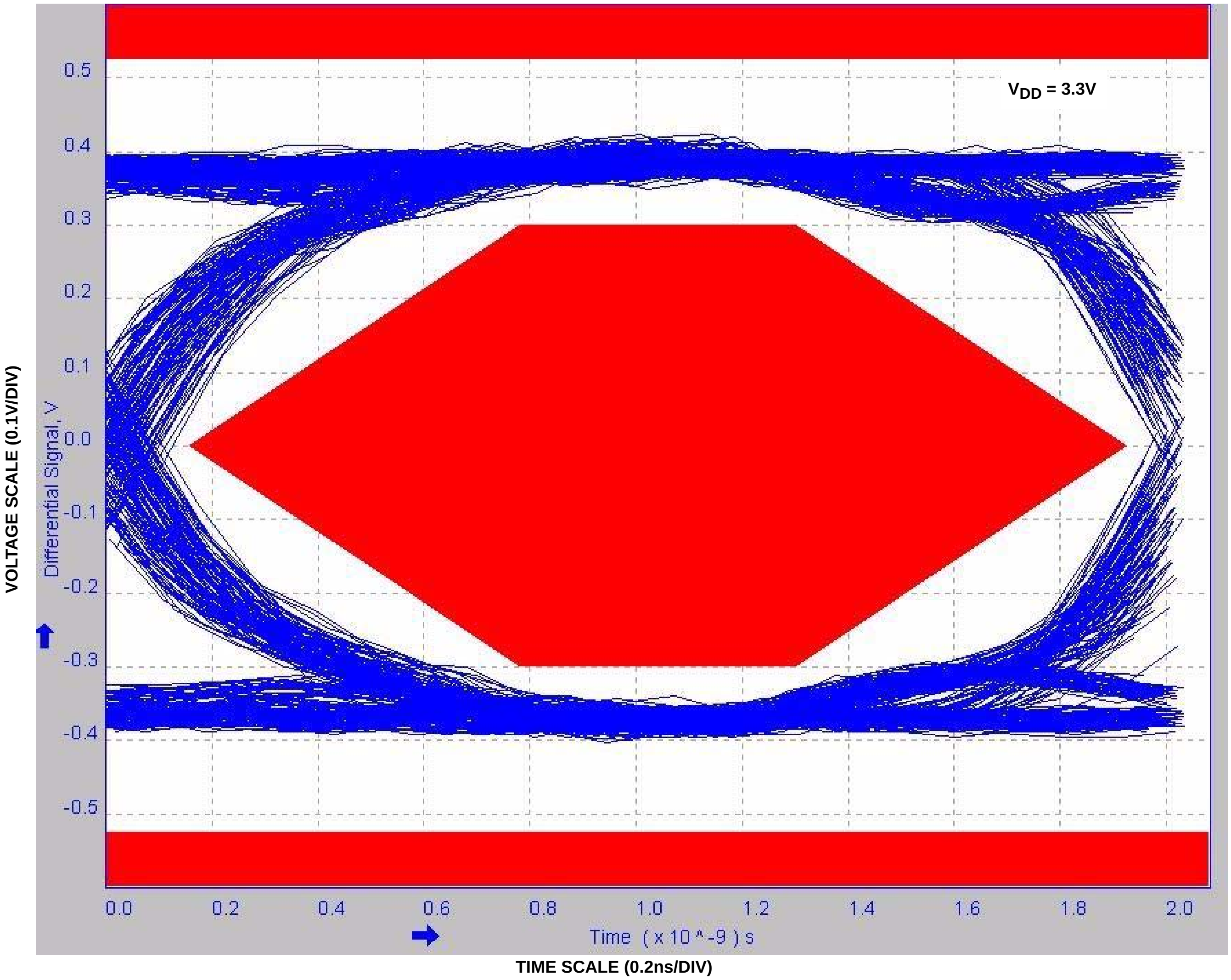


FIGURE 10. EYE PATTERN WITH NEAR END MASK: 480MBPS USB SIGNAL WITH HSx SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

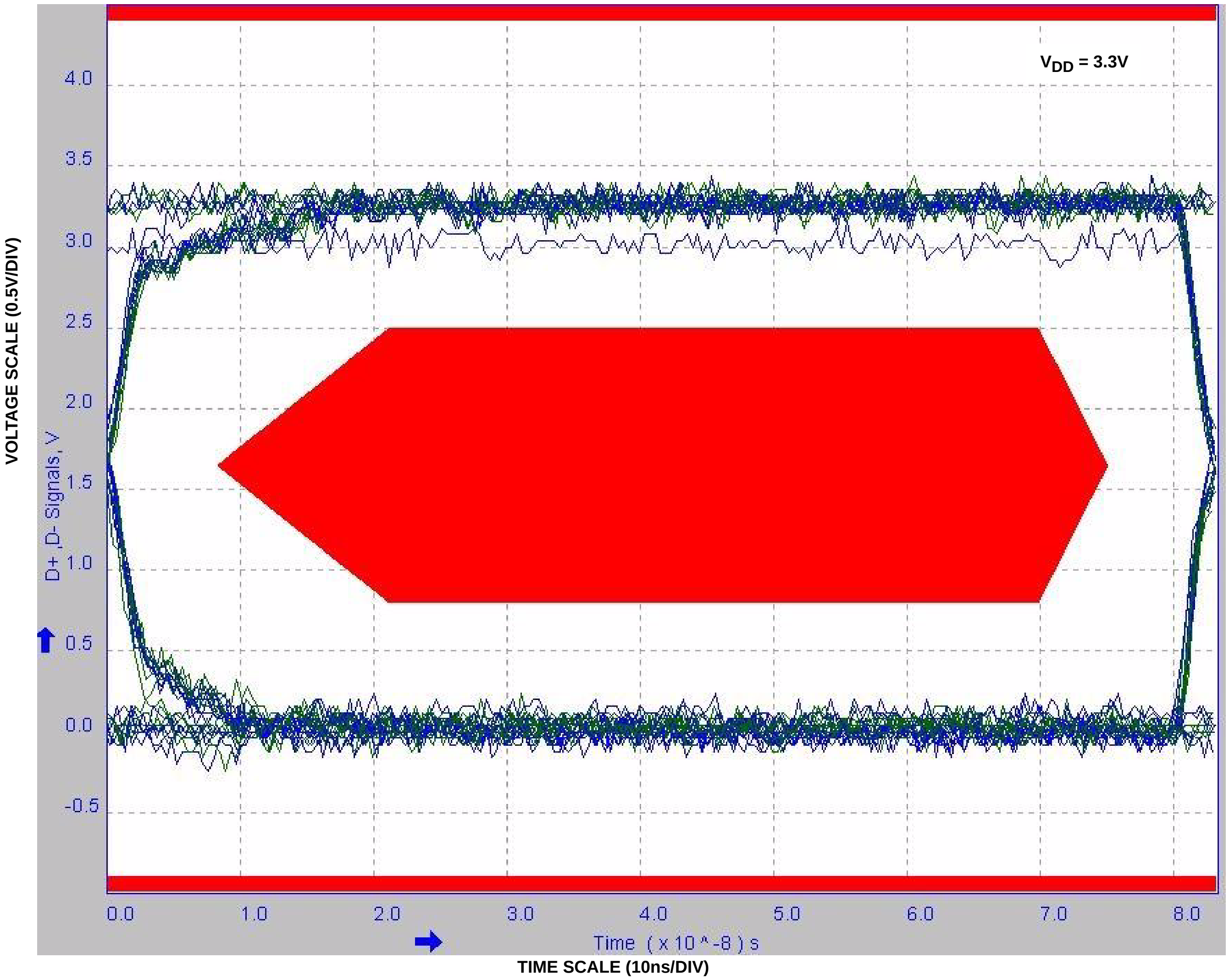


FIGURE 11. EYE PATTERN: 12MBPS USB SIGNAL WITH HSx SWITCHES IN THE SIGNAL PATH

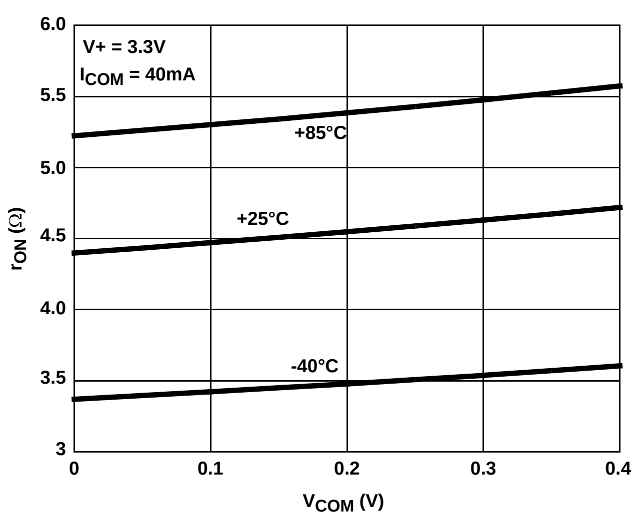


FIGURE 12. HSx SWITCH ON-RESISTANCE vs SWITCH VOLTAGE

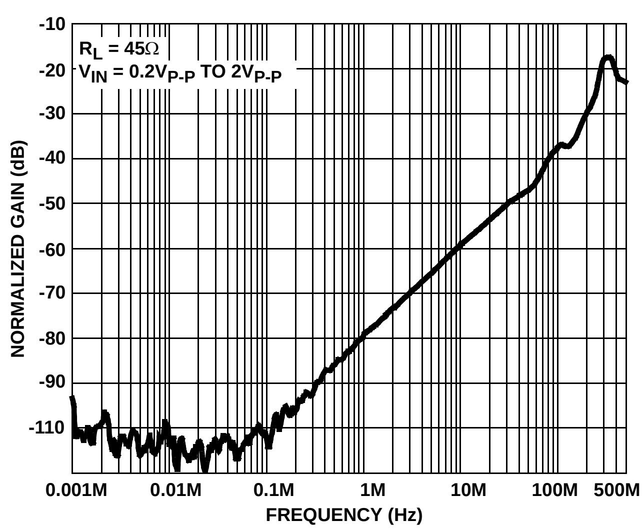


FIGURE 13. OFF-ISOLATION

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

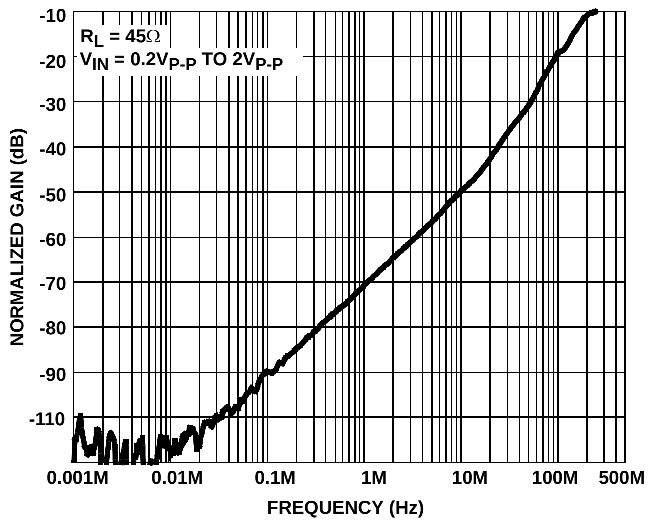


FIGURE 14. CROSSTALK

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND (TDFN Paddle Connection: Tie to GND or Float)

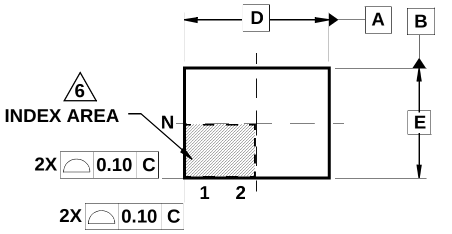
TRANSISTOR COUNT:

98

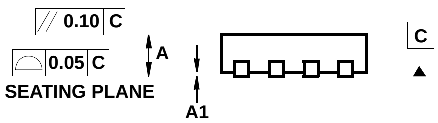
PROCESS:

Submicron CMOS

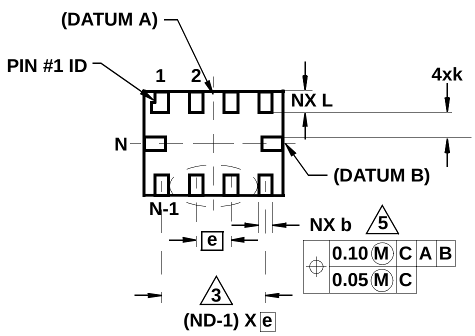
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



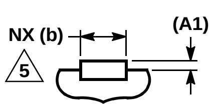
TOP VIEW



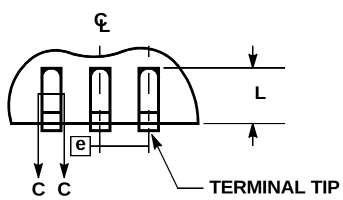
SIDE VIEW



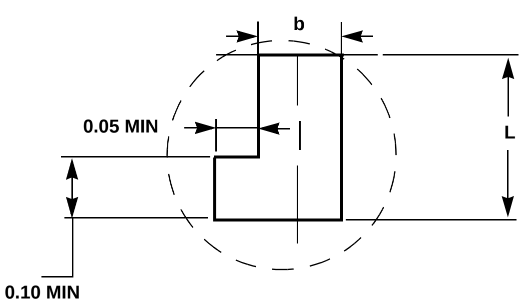
BOTTOM VIEW



SECTION "C-C"



FOR ODD TERMINAL/SIDE



DETAIL “A” PIN 1 ID

L10.2.1x1.6A

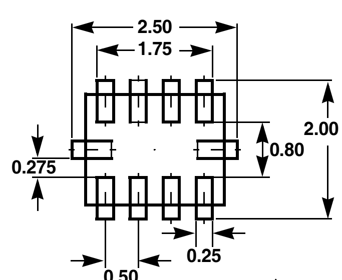
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	5
D	2.05	2.10	2.15	-
E	1.55	1.60	1.65	-
e	0.50 BSC			-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N	10			2
Nd	4			3
Ne	1			3
θ	0	-	12	4

Rev. 3 6/06

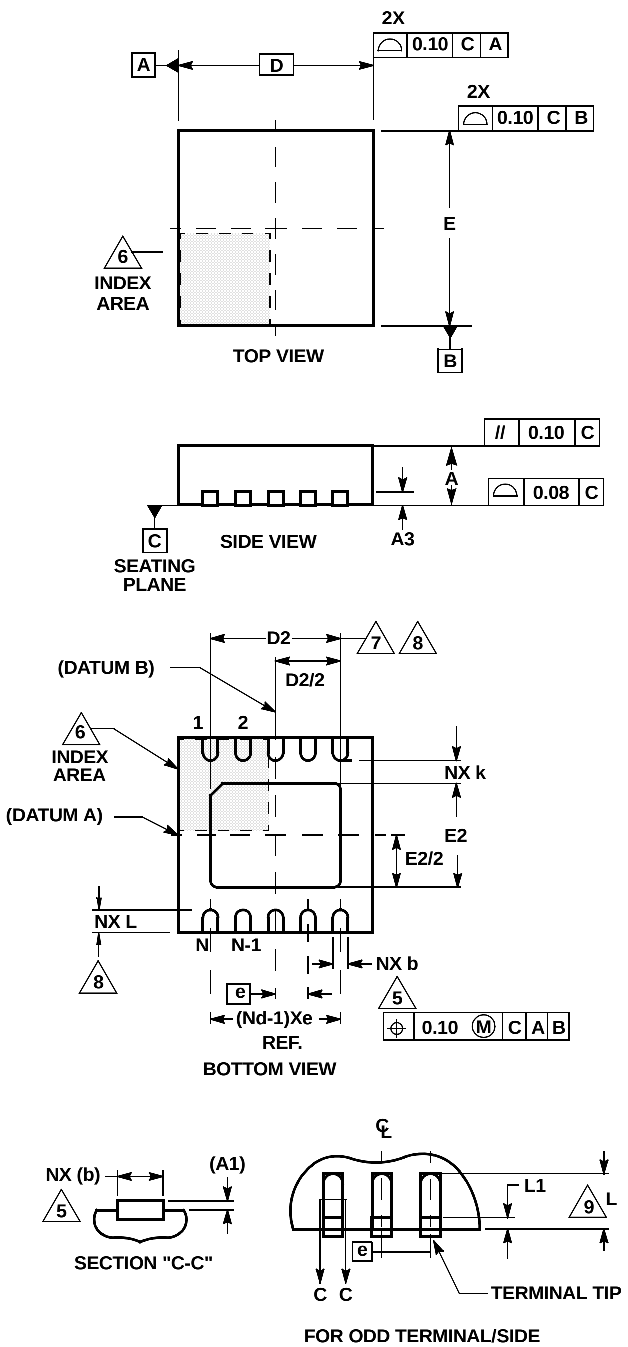
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



LAND PATTERN 10

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e	0.50 BSC			-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N	10			2
Nd	5			3

Rev. 3 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.