

HSD119

Silicon Epitaxial Planar Diode for High Speed Switching

REJ03G1309-0100

Rev.1.00

Oct 27, 2005

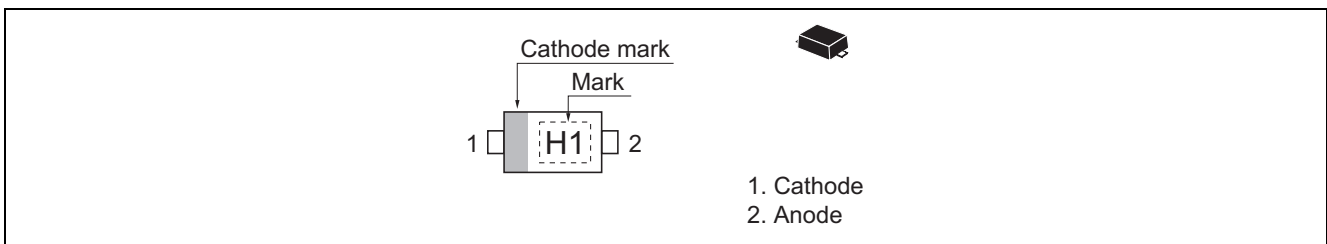
Features

- Low capacitance. ($C = 2.0$ pF max)
- Short reverse recovery time. ($t_{rr} = 3.0$ ns max)
- Super small Flat Lead Package (SFP) is suitable for surface mount design.

Ordering Information

Type No.	Laser Mark	Package Name	Package Code (Previous Code)
HSD119	H1	SFP	PUSF0002ZB-A (SFP)

Pin Arrangement



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Peak reverse voltage	V_{RM}	85	V
Reverse voltage	V_R	80	V
Average rectified current	I_O	100	mA
Peak forward current	I_{FM}	300	mA
Non-Repetitive peak forward surge current	I_{FSM}^*	4	A
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	-55 to +125	°C

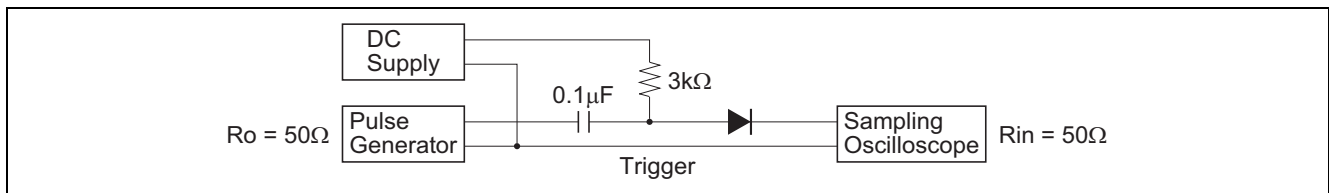
Note: Within 1μs forward surge current.

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Forward voltage	V_{F1}	—	—	0.8	V	$I_F = 10 \text{ mA}$
	V_{F2}	—	—	1.2		$I_F = 100 \text{ mA}$
Reverse current	I_R	—	—	0.1	μA	$V_R = 80 \text{ V}$
Capacitance	C	—	—	2.0	pF	$V_R = 0 \text{ V}, f = 1 \text{ MHz}$
Reverse recovery time*1	t_{rr}	—	—	3.0	ns	$I_F = 10 \text{ mA}, V_R = 6 \text{ V}, R_L = 50 \Omega$

Note: 1. Reverse recovery time test circuit



Main Characteristics

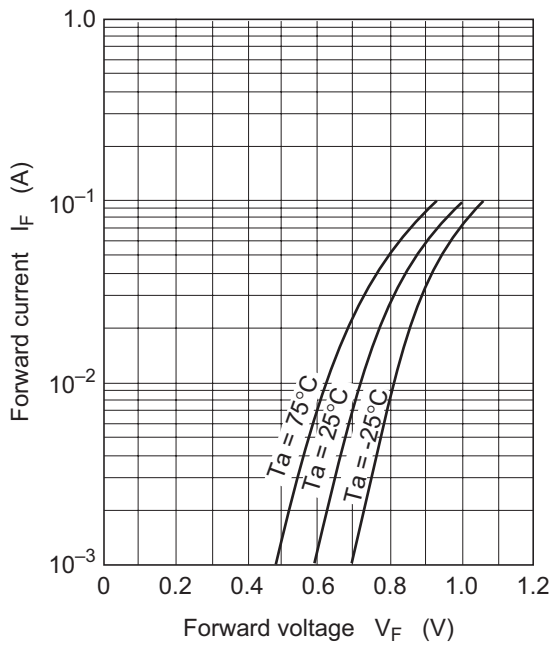


Fig.1 Forward current vs. Forward voltage

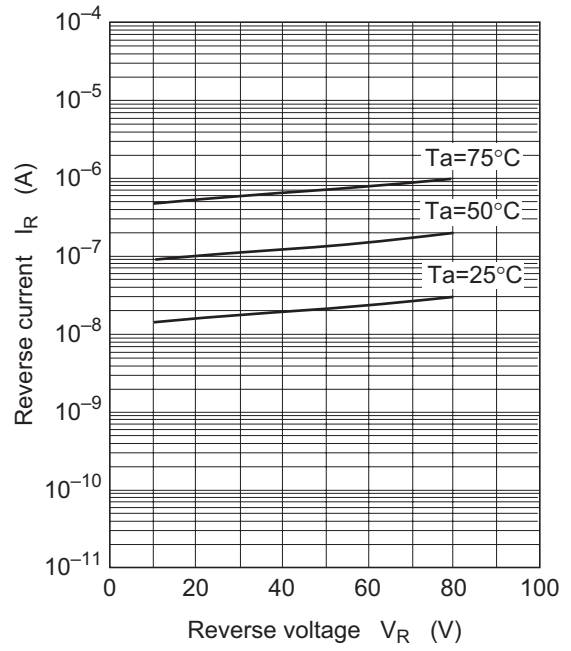


Fig.2 Reverse current vs. Reverse voltage

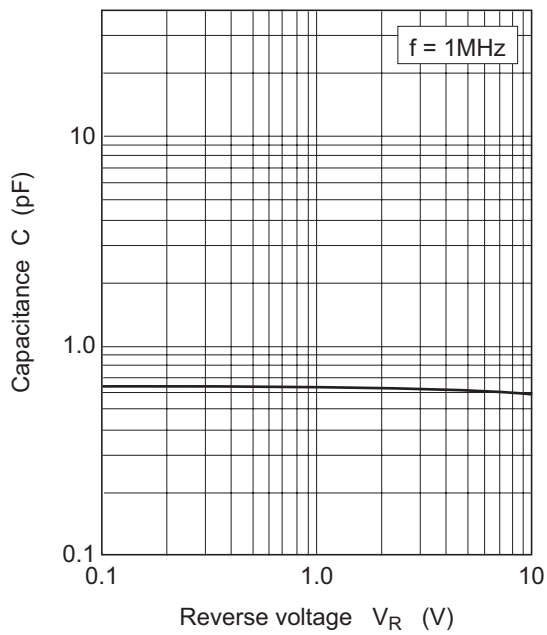
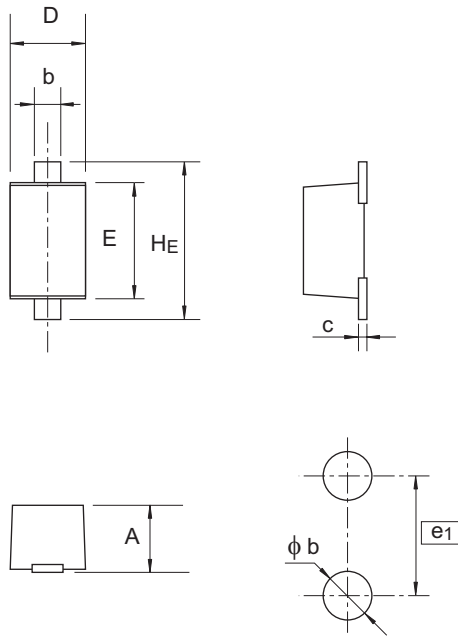


Fig.3 Capacitance vs. Reverse voltage

Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
SFP	—	PUSF0002ZB-A	SFP / SFPV	0.0010g



Pattern of terminal position areas

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	0.50	—	0.55
b	0.25	0.30	0.35
c	0.08	0.13	0.18
D	0.55	0.60	0.65
E	0.90	1.00	1.10
H_E	1.30	1.40	1.50
ϕb	—	0.50	—
e_1	—	1.40	—

Keep safety first in your circuit designs!

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