# Low Threshold N-Channel Enhancement-Mode Vertical DMOS FET

## Features

- Low threshold - 2.0V max
- High input impedance
- Low input capacitance - 125pF max
- Fast switching speeds
- Low ON-resistance
- Free from secondary breakdown
- Low input and output leakage

## Applications

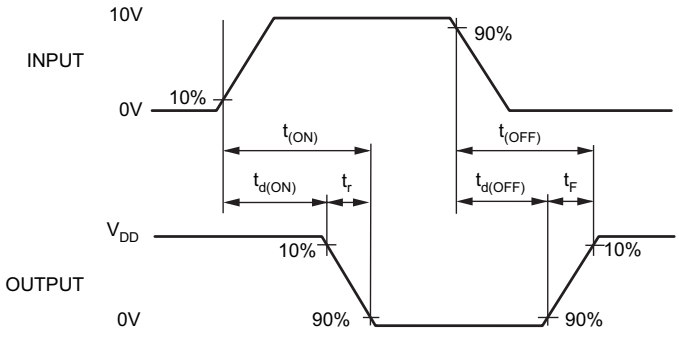
- Logic level interfaces – ideal for TTL and CMOS
- Solid state relays
- Battery operated systems
- Photo voltaic devices
- Analog switches
- General purpose line drivers
- Telecom switches

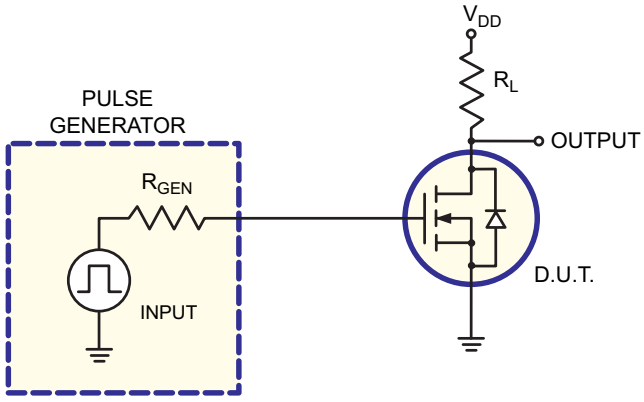
## General Description

The Supertex TN2529 is a low threshold enhancement-mode transistor that utilizes an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

## Switching Waveforms and Test Circuit



## Ordering Information

| Device | Package Options | $BV_{DSS}/BV_{DGS}$ (V) | $R_{DS(ON)}$ (max) (Ω) | $V_{GS(th)}$ (max) (V) | $I_{D(ON)}$ (min) (A) |
|---|---|---|---|---|---|
| | 14-Lead QFN *5x5mm body, 1.0mm height (max), 1.27mm pitch* | | | | |
| TN2529 | TN2529K6-G | 290 | 6.0 | 2.0 | 1.0 |

*-G indicates package is RoHS compliant ('Green')*

## Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| Drain to source voltage | $BV_{DSS}$ |
| Drain to gate voltage | $BV_{DGS}$ |
| Gate to source voltage | ±20V |
| Operating and storage temperature | -55°C to +150°C |
| Maximum junction temperature | 150°C |

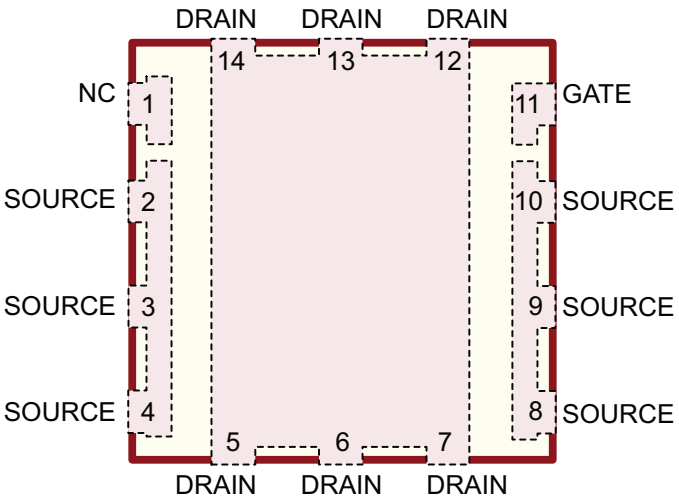
*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

## Product Marking


L = Lot Number
YY = Year Sealed
WW = Week Sealed
A = Assembler ID
C = Country of Origin
—— = "Green" Packaging

**14-Lead QFN**

## Pin Configuration




**14-Lead QFN**
***(top view)***

## Thermal Characteristics

| Package | $I_D$ (continuous) (mA) | $I_D$ (pulsed) (A) | Power Dissipation @$T_A$ = 25°C (W) | $\theta_{jc}$ (°C/W) | $\theta_{ja}$ (°C/W) | $I_{DR}$ (mA) | $I_{DRM}$ (A) |
|---|---|---|---|---|---|---|---|
| 14-Lead QFN | 410† | 2.0 | 2.0‡ | 30 | 62.5 | 410† | 2.0 |

***Notes:***
† *$I_D$ (continuous) is limited by max rated $T_j$ of 150°C.*
‡ *Mounted on FR4 board, 25mm x 25mm x 1.57mm.*

## Electrical Characteristics ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-source breakdown voltage | 290 | - | - | V | $V_{GS}$ = 0V, $I_D$ = 2.0mA |
| $V_{GS(th)}$ | Gate threshold voltage | 0.6 | - | 2.0 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = 1.0mA |
| $\Delta V_{GS(th)}$ | $V_{GS(th)}$ change with temperature | - | - | -5.0 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = 1.0mA |
| $I_{GSS}$ | Gate body leakage current | - | - | 100 | nA | $V_{GS}$ = ±20V, $V_{DS}$ = 0V |
| $I_{DSS}$ | Zero gate voltage drain current | - | - | 10 | µA | $V_{GS}$ = 0V, $V_{DS}$ = Max rating |
| | | - | - | 1.0 | mA | $V_{DS}$ = 0.8 Max Rating, $V_{GS}$ = 0V, $T_A$ = 125°C |
| $I_{D(ON)}$ | ON-state drain current | 0.5 | 1.9 | - | A | $V_{GS}$ = 4.5V, $V_{DS}$ = 25V |
| | | 1.0 | 2.8 | - | | $V_{GS}$ = 10V, $V_{DS}$ = 25V |
| $R_{DS(ON)}$ | Static drain-to-source ON-state resistance | - | 4.0 | 6.0 | Ω | $V_{GS}$ = 4.5V, $I_D$ = 250mA |
| | | - | 4.0 | 6.0 | | $V_{GS}$ = 10V, $I_D$ = 500mA |
| $\Delta R_{DS(ON)}$ | Change in $R_{DS(ON)}$ with temperature | - | - | 1.4 | %/°C | $V_{GS}$ = 10V, $I_D$ = 500mA |
| $G_{FS}$ | Forward transconductance | 300 | 600 | - | mmho | $V_{DS}$ = 25V, $I_D$ = 500mA |
| $C_{ISS}$ | Input capacitance | - | 65 | 125 | pF | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1.0MHz |
| $C_{OSS}$ | Common source output capacitance | - | 35 | 70 | | |
| $C_{RSS}$ | Reverse transfer capacitance | - | 10 | 25 | | |
| $t_{d(ON)}$ | Turn-ON delay time | - | - | 10 | ns | $V_{DD}$ = 25V, $I_D$ = 1.0A, $R_{GEN}$ = 25Ω |
| $t_r$ | Rise time | - | - | 10 | | |
| $t_{d(OFF)}$ | Turn-OFF delay time | - | - | 20 | | |
| $t_f$ | Fall time | - | - | 20 | | |
| $V_{SD}$ | Diode forward voltage drop | - | - | 1.8 | V | $V_{GS}$ = 0V, $I_{SD}$ = 1.0A |
| $t_{rr}$ | Reverse recovery time | - | 300 | - | ns | $V_{GS}$ = 0V, $I_{SD}$ = 1.0A |

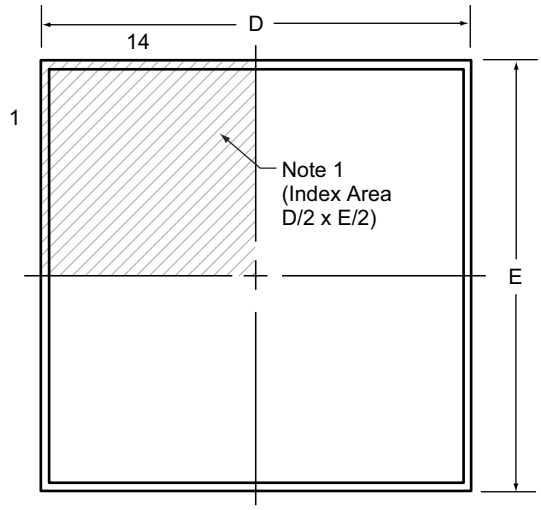
***Notes:***

*1.All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*

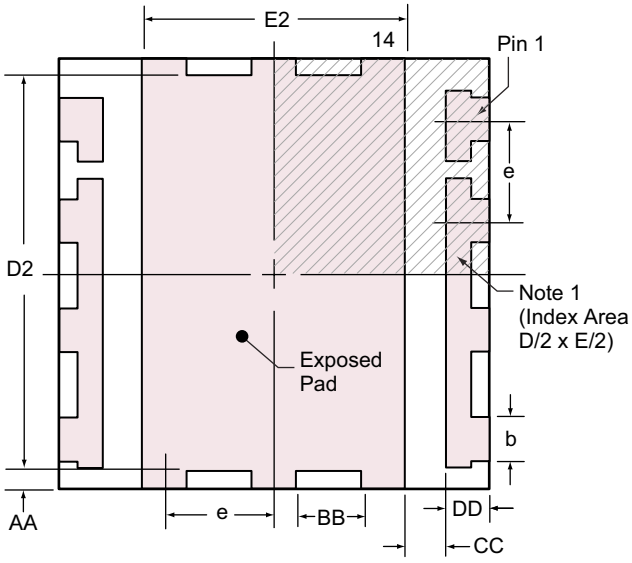
*2.All A.C. parameters sample tested.*

# 14-Lead QFN Package Outline (K6)

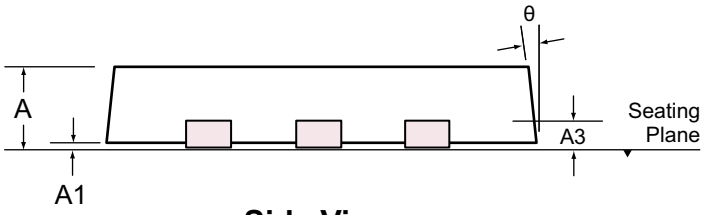
***5x5mm body, 1.0mm height (max), 1.27mm pitch***




**Top View**




**Bottom View**




**Side View**

***Notes:***

*1. Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or a marked feature.*

| Symbol | | A | A1 | A3 | b | D | D2 | E | E2 | e | AA | BB | CC | DD | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.46 | 4.85 | 4.45 | 4.85 | 2.52 | 1.27 BSC | 0.152 | 0.473 | 0.66 | 0.456 | 0° |
| | NOM | 0.90 | 0.02 | | 0.51 | 5.00 | 4.50 | 5.00 | 2.57 | | 0.252 | 0.523 | 0.71 | 0.506 | - |
| | MAX | 1.00 | 0.05 | | 0.58 | 5.15 | 4.55 | 5.15 | 2.62 | | 0.352 | 0.583 | 0.77 | 0.566 | 14° |

***Drawings not to scale.***

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*



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