Dimmable, Low Noise, Dual EL Lamp Driver

Features

- Adjustable output regulation for dimming
- Lamp fade-in/fade-out capability
- Low audible noise
- 180V_{PP} output voltage for higher brightness
- 1.5V enable input logic high
- Single cell lithium ion compatible
- One miniature inductor to power both lamps
- Separately adjustable lamp and converter frequencies
- Split supply capability
- 16-Lead QFN package

Applications

- Dual display cellular phones
- Keypad and LCD backlighting
- PDAs
- Handheld wireless communication products
- Global Positioning Systems (GPS)

General Description

The Supertex HV862 is a low noise, dimmable, high voltage, dual EL Lamp driver designed for driving two electroluminescent (EL) Lamps with a combined area of 5.0 square inches. The input supply voltage range is from 2.5V to 4.5V. Enable input logic high can go as low as 1.5V, which allows logic interface operating from typical 1.8V supplies. The device is designed to minimize audible noise emitted by the EL Lamps.

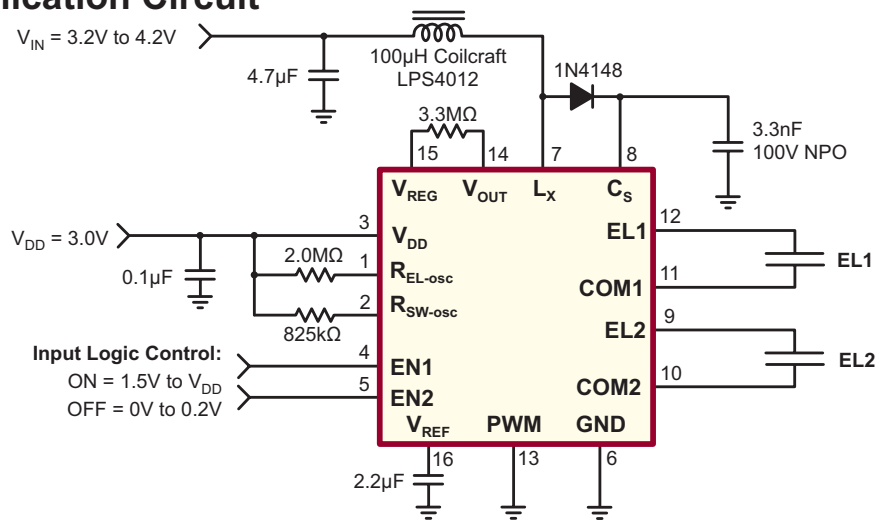
The device uses a single inductor and a minimum number of passive components. Using the internal reference voltage, the regulated output voltage is at a nominal value of 90V. The EL Lamps will therefore see ±90V. The two EL Lamps can be turned ON and OFF using two CMOS logic inputs, EN1 and EN2. The driver is disabled when both EN1 and EN2 are at logic low.

The HV862 has two internal oscillators, a switching MOSFET, and two high voltage EL Lamp driver H-bridges. Each driver has its own half bridge common output, COM1 and COM2, which significantly minimizes the DC offset seen by the EL Lamp. The frequency for the switching MOSFET is set by an external resistor connected between the $R_{SW\text{-}osc}$ pin and the supply pin V_{DD}. The EL Lamp driver frequency is set by an external resistor connected between the $R_{EL\text{-}osc}$ pin and the V_{DD} pin. An external inductor is connected between the L_X and V_{DD} pins or V_{IN} for split supply applications. Depending upon the EL Lamp sizes, a 1.0nF to 10.0nF capacitor is connected between the C_S and ground.

As the switching MOSFET charges the external inductor and discharges it into the capacitor at C_S, the voltage at C_S will start to increase. Once the voltage at C_S reaches a nominal value of 90V, the switching MOSFET is turned OFF to conserve power.

EL Lamp dimming can be accomplished by applying a PWM logic signal to the PWM pin. The EL Lamp brightness will be proportional to the PWM duty cycle. The HV862 can also slowly turn the EL Lamp ON/OFF giving a fade ON/OFF appearance.

Typical Application Circuit



Ordering Information

Device	Package Option
	16-Lead QFN *(3x3mm body, 0.80mm height (max), 0.50mm pitch)*
HV862	HV862K7-G

-G indicates package is RoHS compliant ('Green')

Absolute Maximum Ratings

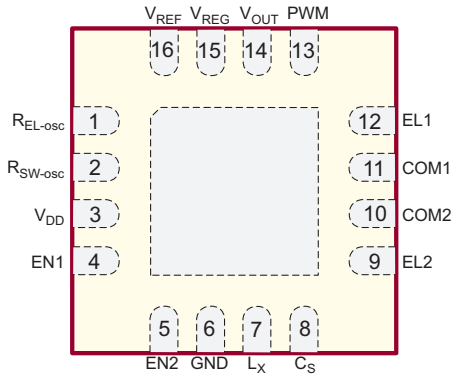
Parameter	Value
V_{DD}, Supply Voltage	-0.5V to 5.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Power Dissipation	1.6W
V_{CS}, Output Voltage	-0.5V to +120V

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Thermal Resistance

Package	θ_{ja}
16-Lead QFN	60 °C/W

Pin Configuration



16-Lead QFN
(top view)

Note:
Pads are at the bottom of the package. Center heat slug is at ground potential.

Product Marking

Y = Last Digit of Year Molded
W = Code for Week Molded
L = Lot Number
———— = "Green" Packaging

16-Lead QFN Package

Electrical Characteristics

(Over recommended operating conditions unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{DS(ON)}$	On-resistance of switching transistor	-	-	7.0	Ω	I = 100mA
V_{CS}	Maximum output regulation voltage	80	90	100	V	V_{DD} = 2.5V to 4.5V
V_{CS}	Output regulation voltage	-	78	-	V	V_{DD} = 2.5V to 4.5V, V_{REG} = 1.092V
		-	62	-		V_{DD} = 2.5V to 4.5V, V_{REG} = 0.862V
		-	45	-		V_{DD} = 2.5V to 4.5V, V_{REG} = 0.632V
V_{REG}	External input voltage range	0	-	1.40	V	V_{DD} = 2.5V to 4.5V
V_{REFH}	V_{REF} output high voltage	1.12	1.26	1.40	V	V_{DD} = 2.5V to 4.5V
$I_{REF(SOURCE)}$	Average sourcing current from V_{REF} pin	-	6.0	-	µA	V_{DD} = 2.5V to 4.5V
$I_{REF(SINK)}$	Average sinking current from V_{REF} pin	-	6.0	-	µA	V_{DD} = 2.5V to 4.5V
I_{DDQ}	Quiescent V_{DD} supply current	-	-	300	nA	V_{DD} = 2.5V, EN1 = EN2 = PWM = LOW
		-	-	400		V_{DD} = 3.0V, EN1 = EN2 = PWM = LOW
		-	-	500		V_{DD} = 4.5V, EN1 = EN2 = PWM = LOW

Electrical Characteristics (cont.)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{DD}	Input current going into the V_{DD} pin	-	-	250	µA	V_{DD} = 2.5V to 4.5V, R_{EL} = 2.0MΩ, R_{SW} = 825kΩ
I_{IN}	Input current including inductor current	-	25	50	mA	V_{IN} = 3.2V (see Test Circuit)
f_{EL}	EL Lamp frequency	160	190	220	Hz	R_{EL} = 2.0MΩ
f_{SW}	Switching transistor frequency	84	100	116	kHz	R_{SW} = 825kΩ
PWM	Input PWM frequency	10	-	100	kHz	---
D	Switching transistor duty cycle	-	88	-	%	---
V_{IH}	Enable PWM input logic high voltage	1.5	-	V_{DD}	V	V_{DD} = 2.5V to 4.5V
V_{IL}	Enable PWM input logic low voltage	0	-	0.2	V	V_{DD} = 2.5V to 4.5V
I_{IH}	Enable PWM input logic high current	-	-	1.0	µA	V_{IH} = V_{DD} = 2.5V to 4.5V
I_{IL}	Enable PWM input logic low current	-	-	-1.0	µA	V_{IL} = 0V, V_{DD} = 2.5V to 4.5V
C_{IN}	Enable PWM input capacitance	-	-	15	pF	---

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	2.5	-	4.5	V	---
f_{SW}	Switching frequency	40	-	200	kHz	---
f_{EL}	EL output frequency	100	-	500	Hz	---
C_{LOAD}	Total EL Lamp capacitance load	0	-	20	nF	---
T_A	Operating Temperature	-40	-	+85	°C	---

Function Table

EN1	EN2	EL1	EL2	COM1	COM2	IC
0	0	Hi Z	Hi Z	Hi Z	Hi Z	OFF
0	1	Hi Z	ON	Hi Z	ON	ON
1	0	ON	Hi Z	ON	Hi Z	ON
1	1	ON	ON	ON	ON	ON

Typical Performance

V_{DD} (V)	V_{IN} (V)	Lamp	I_{IN} (mA)	V_{CS} (V_{PEAK})	F_{EL} (Hz)	Lamp Brightness (cd/m2)	
						EL1	EL2
3.0	4.0	EL1 ON	16.9	93	188	14.8	-
		EL2 ON	11.4			-	18.0
		EL1 and EL2 ON	25.0			14.6	17.7

Pin Configuration and External Component Description

Pin #	Name	Description
1	REL-Osc	External resistor from REL-Osc to VDD sets the EL frequency. The EL frequency is inversely proportional to the external R_{EL} resistor value. Reducing the resistor value by a factor of two will result in increasing the EL frequency by two. f_{EL} = (2.0MΩ • 190Hz) / R_{EL}
2	RSW-Osc	External resistor from RSW-Osc to VDD sets the switch converter frequency. The switch converter frequency is inversely proportional to the external R_{SW} resistor value. Reducing the resistor value by a factor of two will result in increasing the switch converter frequency by two. f_{SW} = (825kΩ • 100kHz) / R_{SW}
3	VDD	Low voltage input supply pin.
4	EN1	Enable input signal for EL Lamp 1. CMOS logic input pin. Refer to the function table.
5	EN2	Enable input signal for EL Lamp 2. CMOS logic input pin. Refer to the function table.
6	GND	Device ground.
7	LX	Drain of internal switching MOSFET. Connection for an external inductor. The inductor LX is used to boost the low input voltage by inductive flyback. When the internal switch is on, the inductor is being charged. When the internal switch is off, the charge stored in the inductor will be transferred to the high voltage capacitor C_S. The energy stored in the capacitor is connected to the internal H-bridge, and therefore to the EL Lamp. In general, smaller value inductors, which can handle more current, are more suitable to drive larger size Lamps. As the inductor value decreases, the switching frequency of the inductor (controlled by R_{SW}) should be increased to avoid saturation.
8	CS	Connect a 100V capacitor between this pin and ground. This capacitor stores the energy transferred from the inductor.
9	EL2	EL Lamp 2 connection.
10	COM2	Common connection for EL2 Lamp.
11	COM1	Common connection for EL1 Lamp.
12	EL1	EL Lamp 1 connection.
13	PWM	PWM pulse input for EL Lamp dimming. The duty cycle of the PWM signal is proportional to the output voltage. If PWM dimming is not desired, then the PWM pin should be tied to ground.
14	VOUT	Switched internal reference voltage.
15	VREG	Input voltage to set V_{CS} regulation voltage. This pin allows an external voltage source to control the V_{CS} amplitude. EL Lamp dimming can be accomplished by varying the input voltage to V_{REG}. The V_{CS} voltage is approximately 71 times the voltage seen on V_{REG}. External resistor connected between VREG and VOUT pins controls the V_{CS} charging rate. The charging rate is inversely proportional to the resistor value.
16	VREF	Internal reference voltage to set the regulation voltage. Connect an external capacitor (C_{REF}) from V_{REF} to ground to slowly brighten the Lamp during power-up and dim down the Lamp during power-down. The size of the capacitor determines the time taken to brighten up or dim down. If fade-in and fade-out are not required, this pin should be left floating. Fade in/Fade out time = C_{REF} • 210e^3.

Figure 1: Block Diagram

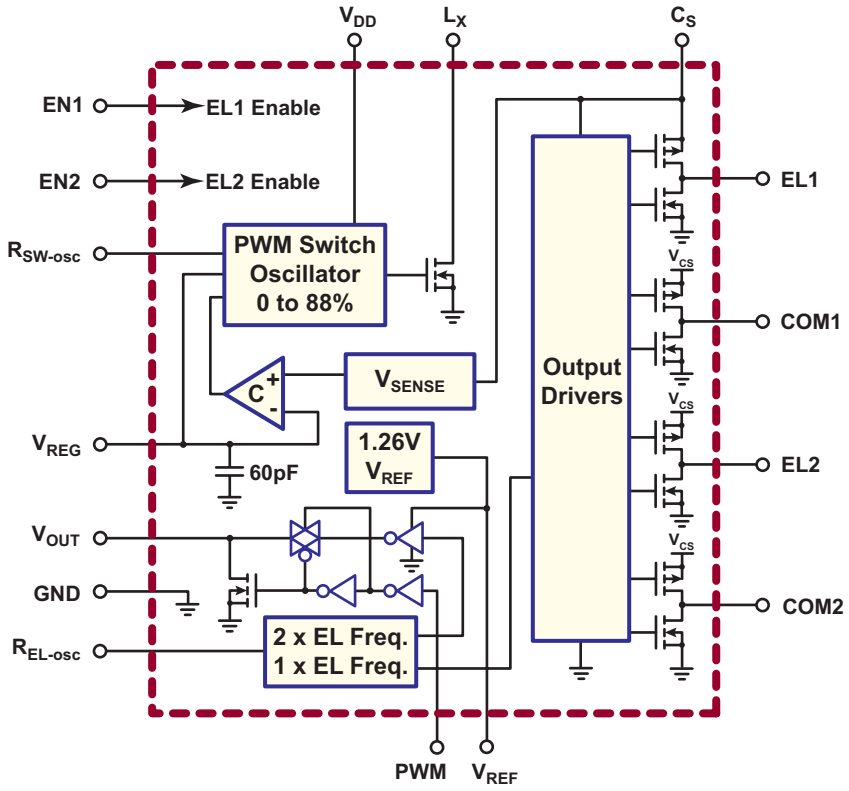


Figure 2: Test Circuit

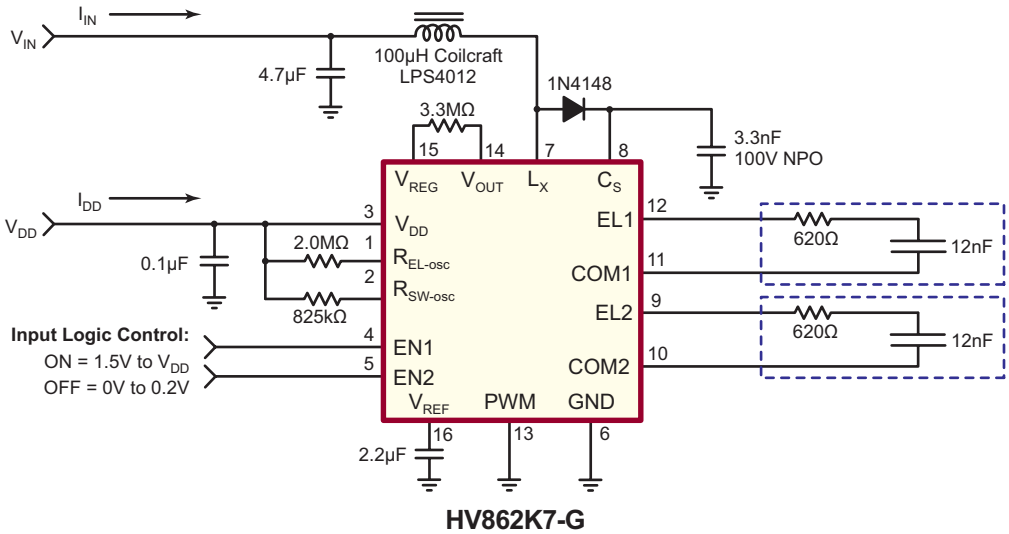
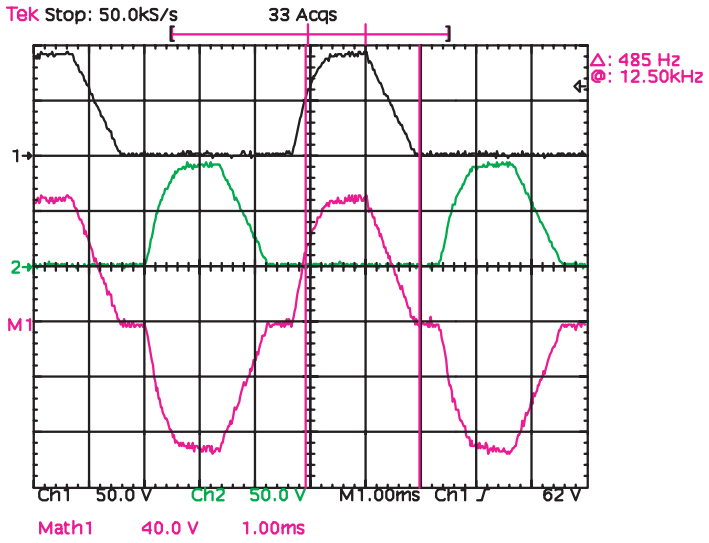


Figure 3: Typical Waveform EL1, COM1 and Differential Waveform EL1 – COM1



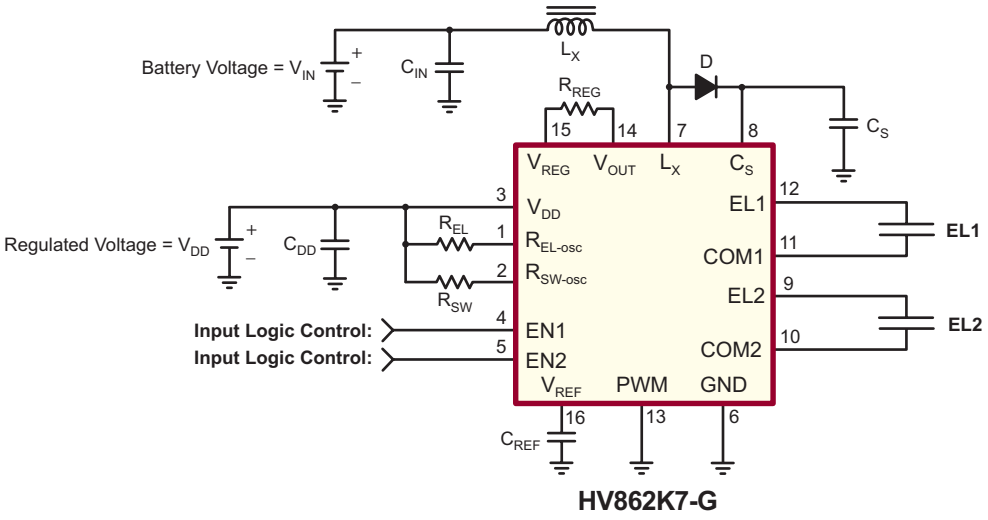
Split Supply Configuration

The HV862 can also be used for handheld devices operating from a battery where a regulated voltage is available. This is shown in Figure 4. The regulated voltage can be used to run the internal logic of the HV862. The amount of current necessary to run the internal logic is 250µA max. Therefore, the regulated voltage could easily provide the current without being loaded down.

Enable/Disable Configuration

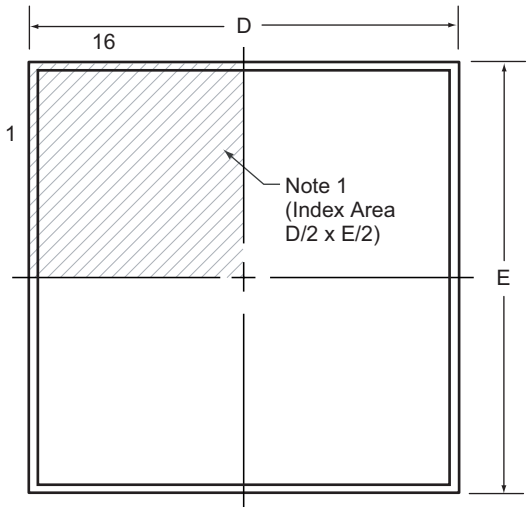
EL1 and EL2 outputs can be enabled and disabled via a logic control signal on the EN1 and EN2 pins respectively. When EN1 is high/low, the Lamp1 (EL1) will be ON/OFF. When EN2 is high/low, the Lamp2 (EL2) will be ON/OFF. The control signal can be from a microprocessor.

Figure 4: Split Supply and Enable/Disable Configuration

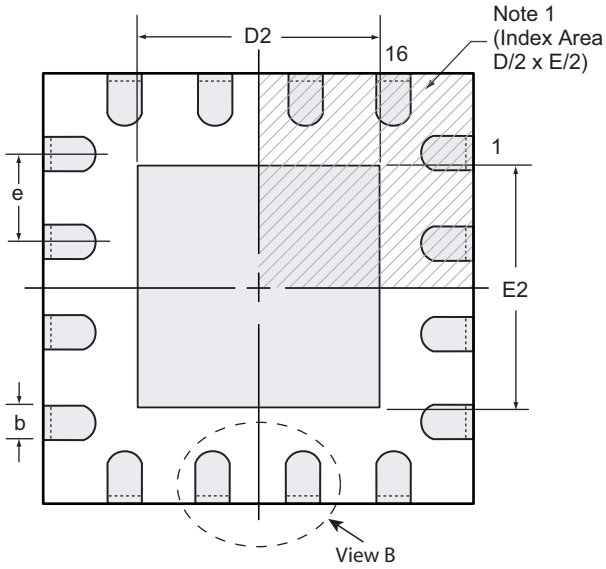


16-Lead QFN Package Outline (K7)

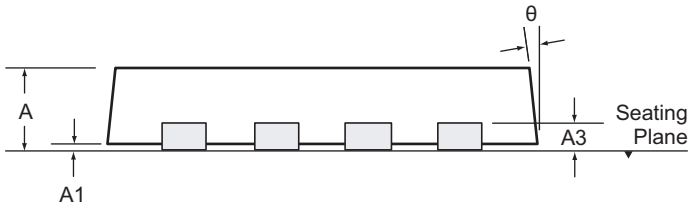
(3x3mm body, 0.80mm height (max), 0.50mm pitch)



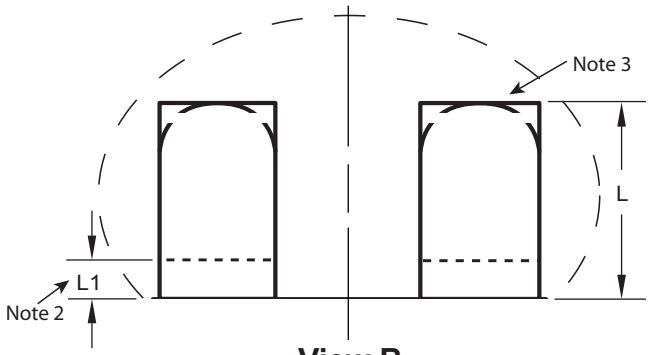
Top View



Bottom View



Side View



View B

Notes:

1. *Details of Pin 1 identifier are optional, but must be located within the indicated area. The Pin 1 identifier may be either a mold, or an embedded metal or marked feature.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	2.85	1.50	2.85	1.50	0.50 BSC	0.20*	0.00	0°
	NOM	0.75	0.02		0.25	3.00	1.65	3.00	1.65		0.30*	-	-
	MAX	0.80	0.05		0.30	3.15	1.80	3.15	1.80		0.45	0.15	14°

JEDEC Registration MO-220, Variation WEED-4, Issue K, June 2006.
Dimensions marked with (*) are non-JEDEC dimensions.
Drawings are not to scale.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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