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Low Power 315/433 MHz OOK/ASK Superheterodyne Receiver with SAW-based Oscillator **PT4316**

DESCRIPTION

The PT4316 is a very low power consumption single chip OOK/ASK superheterodyne receiver for the 315MHz and 434MHz frequency bands and which offers a high level of integration and requires few external components. The PT4316 consists of a low-noise amplifier (LNA), mixer, SAW-based local oscillator, on-chip Sallen-Key low-pass filter, intermediate frequency (IF) limiting amplifier stage with received-signal-strength indicator (RSSI), and analog baseband data recovery circuitry (data filter, peak detector, and data slicer). The PT4316 also implements a discrete one-step automatic gain control (AGC) that reduces the LNA gain by 20dB when the RF input signal is greater than -60dBm. The PT4316 is available in a 16-pin SOP or SSOP package. Both versions are specified over the extended temperature range (-40℃ to +85℃).

FEATURES

- Low current consumption (4.2mA at VDD = 3.0V)
- 2.4V to 3.6V supply voltage operation range
- Optimized for 315MHz or 434MHz ISM Band
- Saw-based oscillator with low frequency drift
- High dynamic range with on-chip AGC
- Power down mode with very low supply current (<1μA)
- Low external parts count
- Available in 16 pins, SOP or SSOP package

APPLICATIONS

- Keyless entry systems
- Remote control systems
- Garage door openers
- Alarm systems
- Security systems
- Wireless sensors

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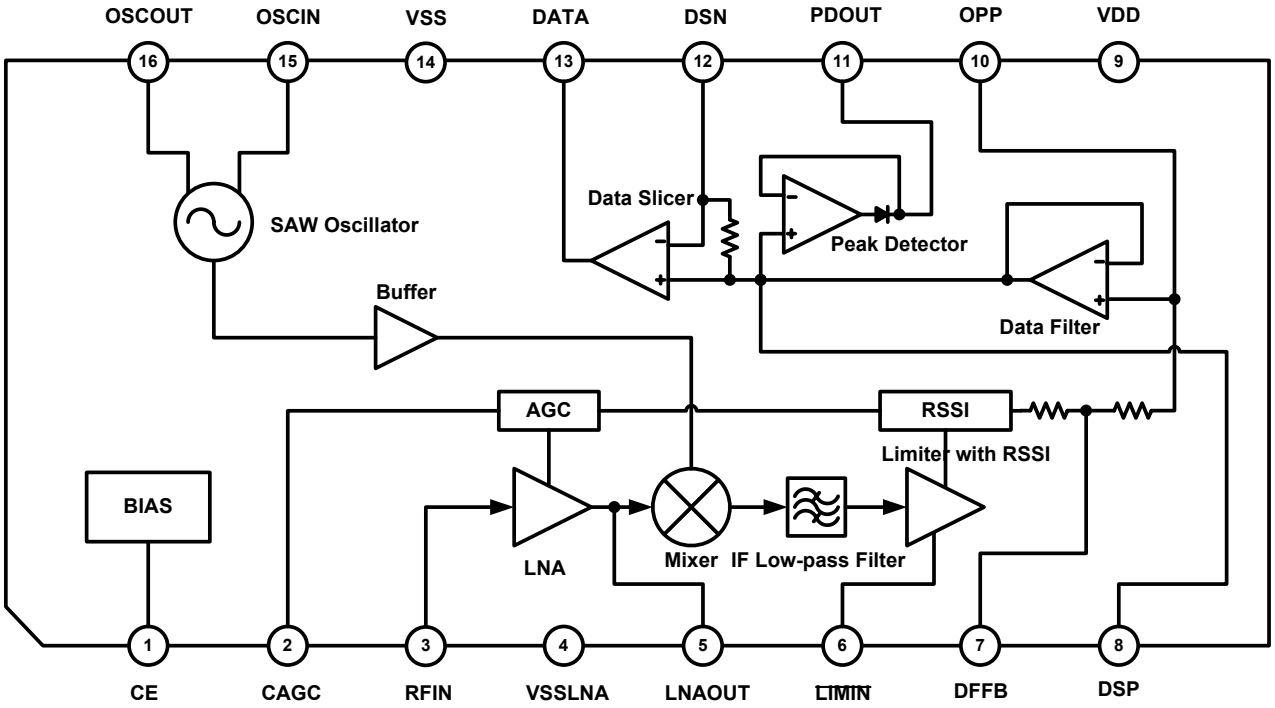
BLOCK DIAGRAM



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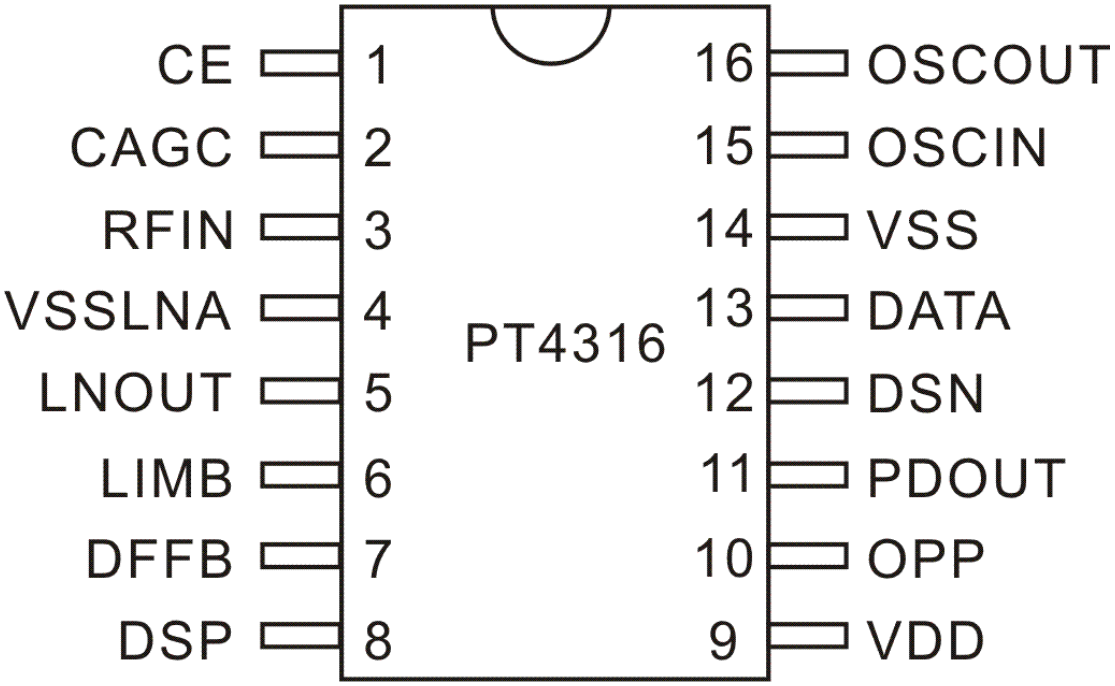
PIN CONFIGURATION



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PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
CE	I	Chip enable	1
CAGC	O	AGC capacitor	2
RFIN	I	RF input	3
VSSLNA	G	Ground for LNA	4
LNAOUT	O	LNAOUT	5
LIMIN	I	Limiting amplifier de-coupling input	6
DFFB	I	Data filter feedback point	7
DSP	I	Positive input of data slicer (data filter output)	8
VDD	P	Power supply	9
OPP	I	Non-inverting op-amp input	10
PDOUT	O	Peak detector output	11
DSN	I	Negative input of data slicer	12
DATA	O	Data output	13
VSS	G	Ground	14
OSCIN	I	Oscillator input	15
OSCOUT	O	Oscillator output	16

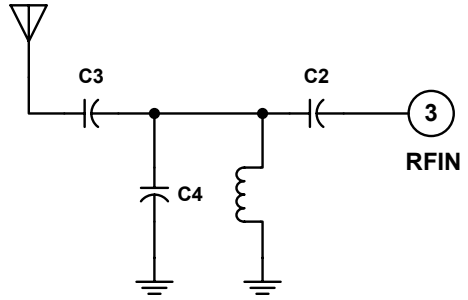
FUNCTION DESCRIPTION

The PT4316 CMOS superheterodyne receiver provides the functionality of a complete receive chain from an antenna input to digital data output. Depending upon signal power and component selection, data rates as high as 50 Kb/s may be achieved.

LOW NOISE AMPLIFIER (LNA)

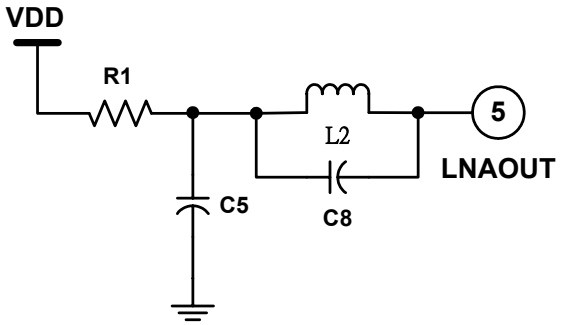
The LNA is an on-chip cascode amplifier with a power gain of 16dB and a noise figure of 3dB. The gain is determined by external matching networks situated ahead of the LNA and between the LNA output and the mixer input.

An example of the input matching network and the input impedance of PT4316 for 315/434MHz bands are shown in the following figure. The component values given in the table following the application circuit are nominal values only. For a particular PCB layout, the user may be required to make component adjustments in order to achieve highest sensitivity.



Frequency (MHz)	LNA Input Impedance (Pin 3) Normalized to 50Ω
315	4.18 – j251.63
433.92	3.60 – j180.20

The LNA output of PT4316 internally connects to the mixer stage so that its output impedance cannot be measured directly. The LNA output requires a DC supply through a choke inductor. For obtaining better LNA gain, a capacitor is recommended to be added in parallel with this inductor to implement a resonant tank at the desired frequency as shown in the following figure. Note that the LNA might self-oscillate and degrade the receiver sensitivity, particularly if a large inductor value is chosen. An alternate matching method is to replace the parallel capacitor with a 330 to 1KΩ resistor, which would reduce the resonant tank Q (quality factor) and avoid the self-oscillation.

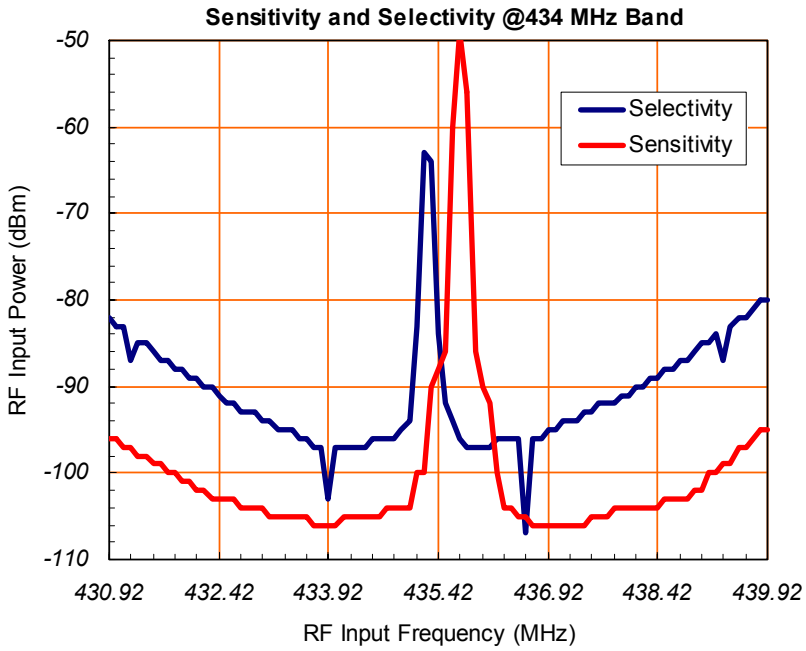


The LNA incorporates gain control circuitry. When the RSSI voltage exceeds a threshold reference value corresponding to an RF input level of approximately -60dBm, the AGC switches on the LNA gain reduction resistor. The loading resistor reduces the LNA gain by 20dB, thereby reducing the RSSI output by approximately 280mV. The threshold reference voltage which is compared with the RSSI voltage to determine the gain state of the LNA is also reduced. The LNA resumes high-gain mode when the RSSI voltage drops below this lower threshold voltage corresponding to approximately -66dBm RF input. The AGC has a hysteresis of around 6dB and the time constant of the AGC response is determined by the value of the capacitor connected to pin 2 (CAGC). The capacitor value should be chosen with consideration of the data rate.

MIXER

The doubly-balanced mixer down-converts the input frequency (RF) in the range of 250MHz to 500MHz to the intermediate frequency (IF) at 1.2MHz with a voltage gain of approximately 20dB by utilizing either high- or low-side injection of the local oscillator signal. In the case that the RF input to the mixer is single-ended, the unused mixer input must be tied to ground via a capacitor. The mixer is followed by a low pass filter with a corner frequency of 5MHz in order to suppress RF signals at the IF output.

Both the desired signal band and image signal band are converted to the IF band. If the environment, especially the image channel, is noisy, it is recommended that an external SAW filter be added to remove the unwanted signals. The channel selectivity indicates the ability of the noise rejection. The measurement of channel selectivity of PT4316 without the external SAW filter is shown in the figure as the following.



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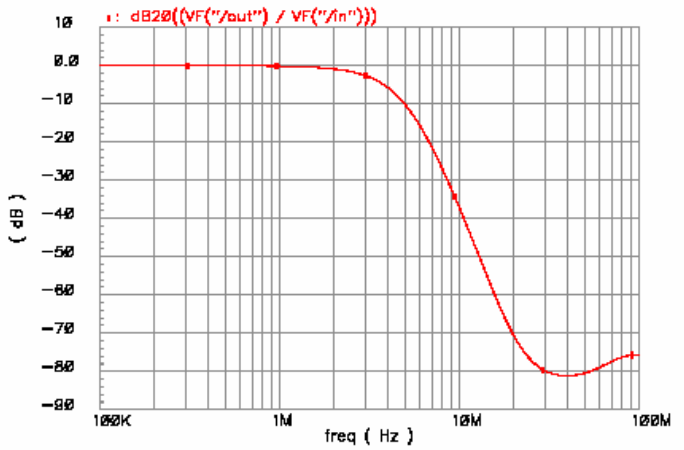
IF LOW-PASS FILTER

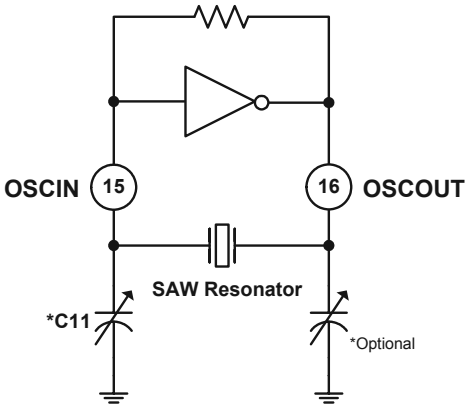
The built-in IF filter is composed of three Sallen-Key low-pass filter stages and it has a -3dB bandwidth of 3.1MHz. One stage Sallen-Key filter and frequency response of three cascaded filters as following figure.

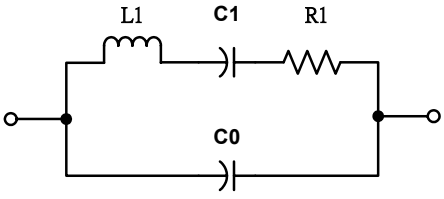


SAW OSCILLATOR

The SAW oscillator is configured as a Colpitts oscillator but consists of 3 cascaded amplifiers instead of a single amplifier. Although the circuit configuration is quite similar to the conventional Colpitts oscillator, this configuration is capable of generating a much higher value of negative resistance. The one-port SAW resonator is connected between pin 15 (OSCIN) and pin 16 (OSCOUT).

The capacitor connected from pin 15 (OSCIN) to ground is used for adjusting the oscillation frequency. In general, this capacitor is unnecessary if the frequency drift can be ignored. The figures at below, an equivalent circuit of a SAW resonator and its component valuesare, are shown for reference.





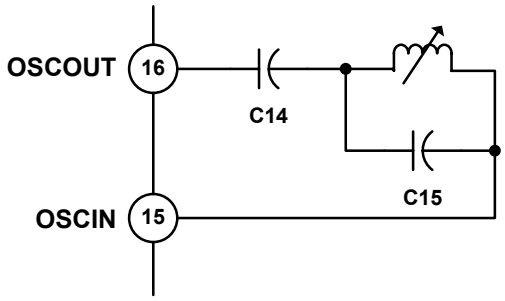
SAW resonator equivalent circuit

Part Number	Center Frequency(MHz)	R1 (Ω)	L1 (μH)	C1 (pF)	C0 (pF)
MFSRA316.2	316.2	19	119.06	0.00213	2.4
MFSRA435.2	435.2	20	86.47	0.00155	2.0

For down-converting the RF signal to the IF frequency, a suitable SAW oscillation frequency must be chosen. For the PT4316, the -3dB bandwidth of the IF chain is located from 250KHz to 3.1MHz and its optimum value is around 1.2MHz. The following equation may be utilized to calculate an appropriate SAW oscillator frequency.

SAW Oscillator (Freq.) = TX (Freq.) +/– (250KHz ~ 3.1MHz)

In addition to a SAW resonator, the resonant circuit may also be achieved by an “L-C tank”. The recommended circuit for an “L-C tank” is as the following figure.



Frequency (MHz)	C14 (pF)	C15 (pF)	Trimmer L3 (H)
315	100	10	2.5 T
433.92	100	5.6	1.5 T

LIMITER/RSSI

The limiter is an AC coupled multi-stage amplifier with a cumulative gain of approximately 70dB that has a band-pass characteristic centered around 2MHz. The -3dB bandwidth of the limiter is around 5MHz (from 250KHz to 5.2MHz). The limiter circuit also produces an RSSI voltage that is directly proportional to the input signal level with a slope of approximately 14mV/dB. This signal is used to demodulate ASK-modulated receive signals in the subsequent baseband circuitry.

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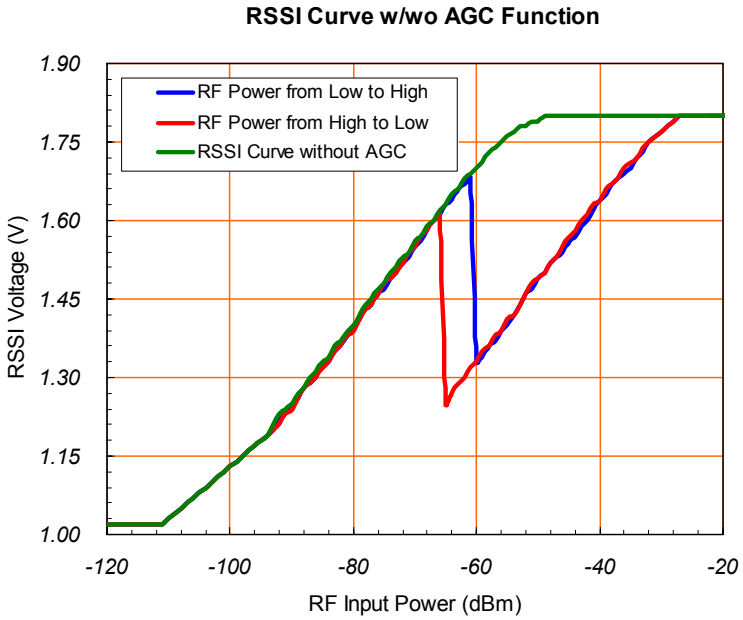
AUTO GAIN CONTROL (AGC)

The AGC circuitry monitors the RSSI voltage level. As described above, when the RSSI voltage reaches a first value corresponding to an RF input level of approximately -60dBm, the AGC reduces the LNA gain by 20dB, thereby reducing the RSSI output by approximately 280mV. When the RSSI voltage drops below a level corresponding to an RF input of approximately -66dBm, the AGC sets the LNA back to high-gain mode.

The change of RSSI voltage versus RF input power is shown as the following figure. When the RSSI level increases and then exceeds 1.68 V (RF input power rising), the AGC switches the LNA from high-gain mode to low-gain mode. As RSSI level decreases back to 1.25V (RF input power falling), the AGC switches the LNA from low-gain mode back to high-gain mode.



RSSI vs. RF input power

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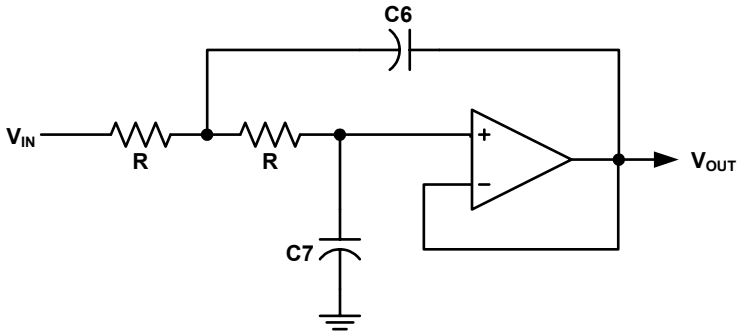
DATA FILTER

The data filter is also implemented as a 2nd-order low-pass Sallen-Key filter as shown in the following figure. The pole locations are set by the combination of two on-chip resistors and two external capacitors. Adjusting the value of the external capacitors changes the corner frequency to optimize for different data rates. The corner frequency should be set to approximately 1.5 times the highest expected data rate from the transmitter. Ideal Sallen-Key filter is as the following figure.



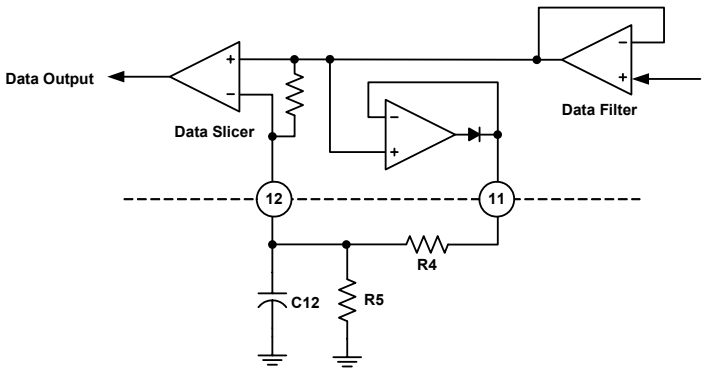
Utilizing the on-board voltage follower and the two 100KΩ on-chip resistors, a 2nd-order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 7 (DFFB) and 8 (DSP) and to pin 10 (OPP) as depicted in the Application Circuit (see p.18). The following table shows the recommended values of the capacitors for the different data rate.

Data Rate	C6 (pF)	C7 (pF)
< 2Kb/s	1000	270
2Kb/s — 10Kb/s	470	150
10Kb/s — 20Kb/s	150	56
20Kb/s — 40Kb/s	56	15
> 40Kb/s (see Note)	15	4.7

Note: the maximum data rate of PT4316 is 50Kb/s

PEAK DETECTOR

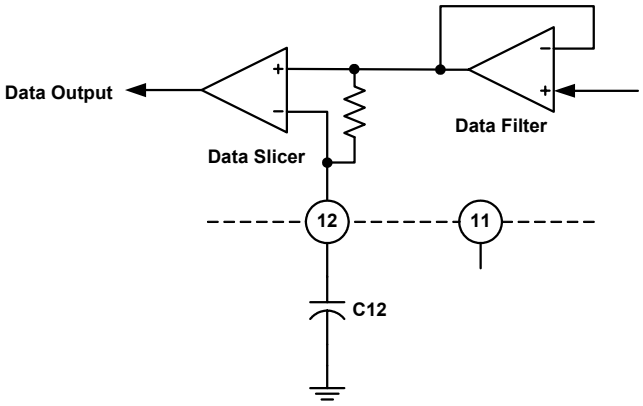
The peak detector generates a DC voltage which is proportional to the peak value of the received data signal. An external R-C network is necessary. The peak detector input is connected to the RSSI output of the limiter and the output is connected to pin 8 (DSP). This output can be used as an indicator for the received signal strength for use in wake-up circuits and as a reference for the data slicer in ASK mode. The time constant is calculated with the driving current of the data filter op-amp, 100μA. Circuit for using peak detector for faster start-up as the following figure.



DATA SLICER

The data slicer consists chiefly of a fast comparator, which allows for a maximum receive data rate of up to 50Kb/s. The maximum achievable data rate also depends upon the IF filter bandwidth. Both data slicer inputs are accessible off-chip to allow for easy adjustment of the slicing threshold. The output delivers a digital data signal (CMOS level) for subsequent circuits. The self-adjusting threshold on pin 12(DSN) is generated by an R-C network or peak detector depending upon the baseband coding scheme.

The suggested data slicer configuration uses an internal 100KΩ resistor connected between DSN and DSP with a capacitor from DSN to ground as shown in the following figure. The cut-off frequency of the R-C integrator must be set lower than the lowest frequency appearing in the data signal to minimize distortion in the output signal. Circuit for generating data slicer threshold as following figure.



DEMODULATION

By the different circuit combination, the PT4316 can achieve two demodulation modes, which are called “Peak Mode” and “Average Mode.”

PEAK MODE

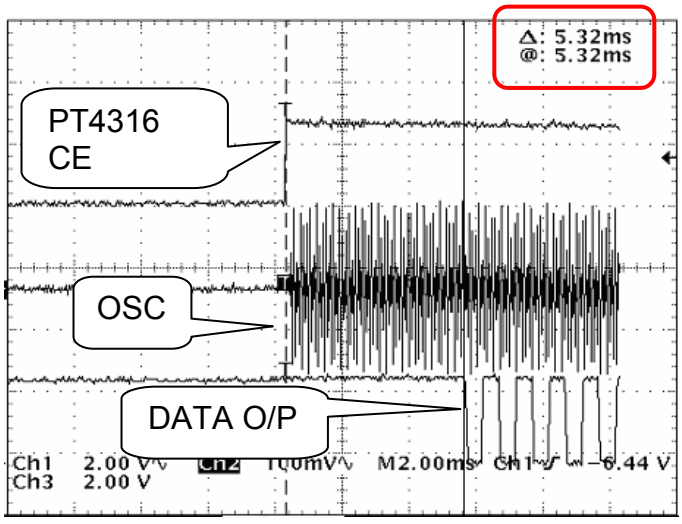
By adjusting the ratio of R4/R9, the threshold voltage can be set at the peak detector output for comparison (see the figure of Circuit for using peak detector for faster start-up at p.11). The demodulated data would go into a quasi-mute state as the RF input signal becomes very small, which means when there is no RF signal received or the RF signal is too small, the DATA output will remain mostly at a logic “HIGH” level. If the environment is very noisy, the R4 value may be enlarged to achieve better immunity against noise but at the cost of less sensitivity.

AVERAGE MODE

When the “Average Mode” has been set (see the figure of Circuit for generating data slicer threshold at p.11), the DATA output will exhibit a toggling behaviour similar to random noise. In this mode, better sensitivity may be achieved, but noise immunity is worse than in “Peak Mode.”

POWER-DOWN CONTROL

The chip enable (CE) pin controls the power on/off behaviour of the PT4316. Connecting CE to “HIGH” sets the PT4316 to the normal operation mode; connecting CE to “LOW” sets the PT4316 to standby mode. The chip consumption current will be lower than 1μA in standby mode. Once enabled, the PT4316 requires <10ms to recover received data. Timing plot of PT4316 chip enable as following figure.



ANTENNA DESIGN

For a $\lambda/4$ dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L = \frac{7132}{f}.$$

For example, if the frequency is 315MHz, then the length of a $\lambda/4$ antenna is 22.6cm. If the calculated antenna length is too long for the application, then it may be reduced to $\lambda/8$, $\lambda/16$, etc. without degrading the input return loss. However, the RF input matching circuit may need to be re-optimized. Note that in general, the shorter the antenna, the worse the receiver sensitivity and the shorter the detection distance. Usually, when designing a $\lambda/4$ dipole antenna, it is better to use a single conductive wire (diameter about 0.8 mm to 1.6 mm) rather than a multiple core wire.

If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB (ε_r = 4.7) and a strip-width of 30mil, the length of the antenna, L (in cm), is calculated by

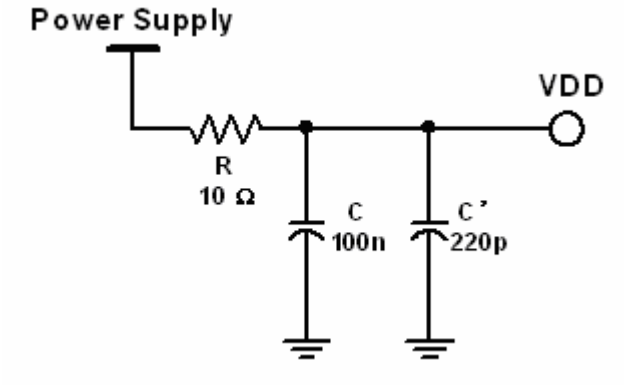
$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$ where “c” is the speed of light (3 x 1010 cm/s)

When the PT4316 is operated in a noisy environment, it is recommended that an external SAW filter be added between the input matching network and antenna.

PCB LAYOUT CONSIDERATION

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers. Note that if the PCB design incorporates a printed loop antenna, there should be no ground plane beneath the antenna.

Within the PT4316, the power supply rails of the LNA and others blocks should be separated for improving the isolation and minimizing the noise coupling effects. Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to the VSS and VSSLNA pins. To reduce supply bus noise coupling, sensitive blocks such as the LNA or mixer should be biased thru separated power supply traces, incorporating series-R, shunt-C filtering as the following figure.



If the power source is capable of supplying a stable voltage, C' may be ignored. In some applications, the DC source may be supplied from a simple AC-DC transformer. In such cases, the DC voltage level could be unstable and may adversely affect ASK/OOK receiver sensitivity. A solution may be to increase C to an appropriately large value while continuing to make the power source as stable as possible.

Finally, in an RF system, it is extremely important to keep the LNA or RF signal traces away from large voltage swing signals and digital data signal traces to avoid unnecessary interference.

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V)

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	V_{SS}- 0.3 to V_{SS} + 6.0	V
Soldering temperature	T_{SLD}	225	℃
Soldering time	t_{STG}	10	s
Operating temperature range	Topr	-40 to 85	℃
Storage temperature range	Tstg	-55 to 150	℃

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage range	V_{DD}	2.4	3.0	3.6	V
Operating temperature	T_A	-40	27	85	℃

ELECTRICAL CHARACTERISTICS

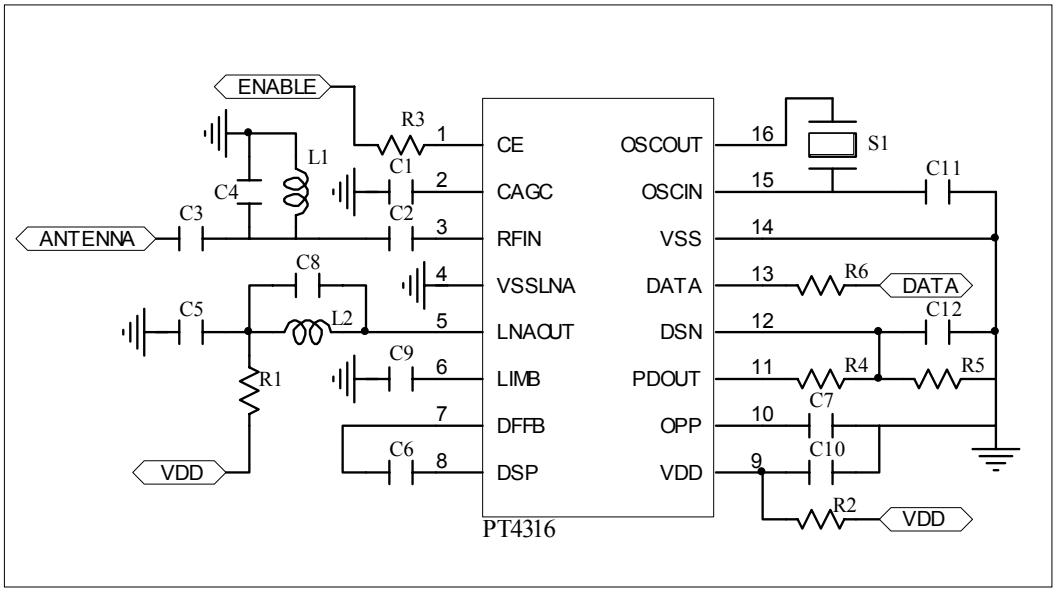
(V_{DD} = 3.0V, V_{SS} = 0V, CE = "HIGH", Temp= +27℃, f_{RF} = 433.92MHz)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
General Characteristics						
Frequency range	f_{RF}		250		500	MHz
Maximum receiver input level	$P_{RF, MAX}$		-20	-10		dBm
Sensitivity (see Note 1)	S_{IN}	ASK (see Note 2), peak power level		-103	-100	dBm
		OOK, peak power level		-97	-94	
Data rate (see Note 3)	D_{Rate}			1	50	Kb/s
Power Supply						
Supply voltage	V_{DD}		2.4	3.0	3.6	V
Consumption DC current	I_{DD}	CE = "HIGH"		4.2	4.6	mA
Standby DC current	$I_{stand-by}$	CE = "LOW"			1.0	μA
LNA						
Power gain	G_{LNA}	Matched to 50Ω		16	18	dB
Noise figure	NF_{LNA}	Matched to 50Ω		3	3.6	dB
Input third-order intermodulation intercept point	$IIP3_{LNA}$	Matched to 50Ω		-12		dBm
Auto Gain Control (AGC)						
AGC attack and decay ratio (see Note 4)	RA_{AGC}	T_{attack}/T_{decay}		0.1		-
AGC leakage current	$I_{Leak,AGC}$	at +85℃		±100		nA
AGC threshold voltage	V_{thresh}	LNA gain from low to high		1.25		V
		LNA gain from high to low		1.68		
AGC threshold referred to the RF input power (see Note 5)	$P_{in,thresh}$	LNA gain from low to high		-66		dBm
		LNA gain from high to low		-60		
Down-Conversion Mixer						
Conversion voltage gain	G_{MIX}		16	20		dB
Noise figure (SSB)	NF_{MIX}			19	20	dB
Input third-order intermodulation intercept point	$IIP3_{MIX}$			-16		dBm
IF Filter						
Bandwidth	BW_{IFF}			3.1		MHz
SAW Oscillator						
Start-Up time	$T_{OSC,start}$				200	μs
IF Limiting Amplifier						
IF frequency	f_{IF}			1.2		MHz
Gain	G_{LIM}			70	80	dB

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Bandwidth	BW_{LIM}			5		MHz
RSSI dynamic range	DR_{RSSI}			70		dB
RSSI curve slope	SL_{RSSI}			14	10.8	mV/dB
RSSI level	V_{RSSI}	P_{RF} < -120dBm		1.0		V
		P_{RF} > -30dBm		1.8		
Data Filter						
Bandwidth	BW_{DF}			1	50	KHz
Maximum load capacitance	$C_{Load,DS}$				20	pF

Notes:
1. BER = 1e-3, data rate = 2Kb/s.
2. Use AM 99% with square wave modulation (if limited by capabilities of signal generator).
3. Data rate selection affects choice of component values for data filter, peak detector and slicer.
4. AGC attack and decay currents are around 15μA and 1.5μA.
5. AGC threshold depends on the gain setting and matching of LNA.

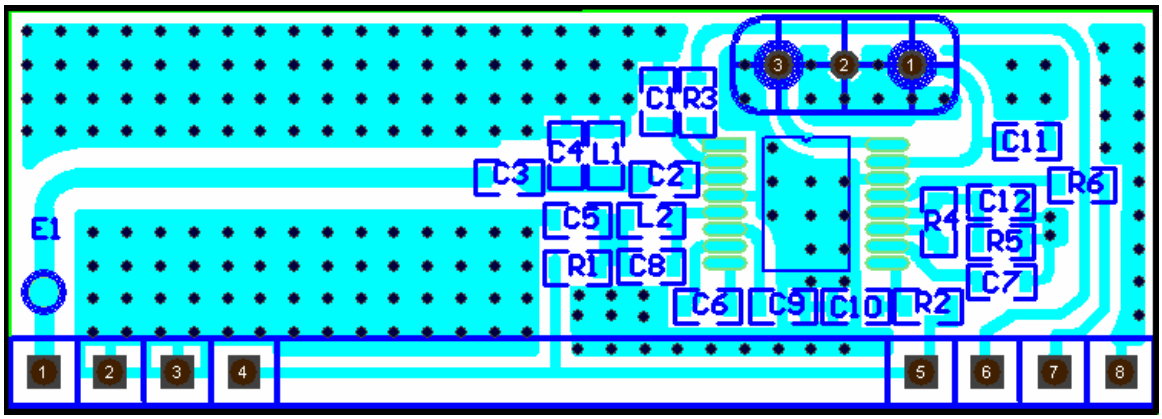
APPLICATION CIRCUIT



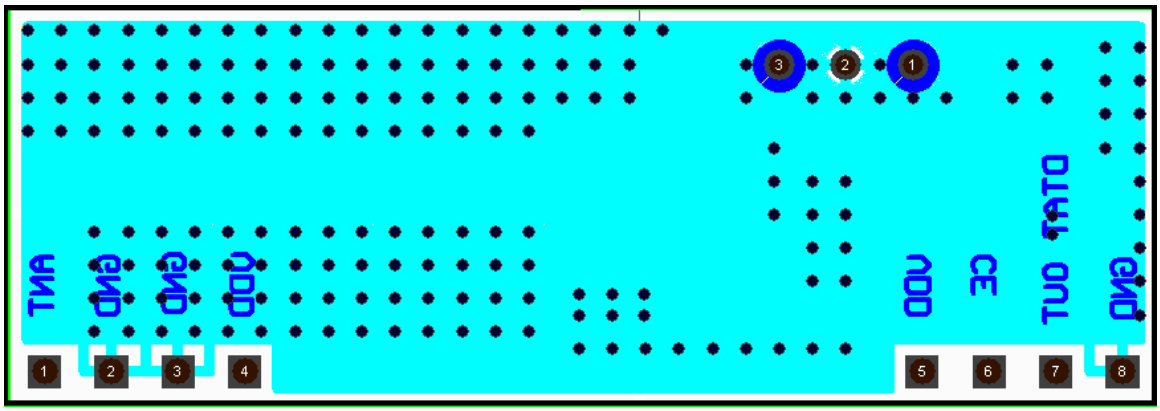
Component	Value for 315MHz		Value for 434MHz		Unit
	Peak Mode	Average mode	Peak Mode	Average mode	
S1 (see Note 1)	313.2 — 314.5 315.5 — 316.8		432.1 — 432.4 434.4 — 435.7		MHz
R1, R2	33	33	33	33	Ω
R3	10K	10K	10K	10K	Ω
R4	12K	—	12K	—	Ω
R5	1M	—	1M	—	Ω
R6	1K	1K	1K	1K	Ω
L1	56n	56n	33n	33n	H
L2	82n	82n	68n	68n	H
C1, C5, C10, C12	100n	100n	100n	100n	F
C2	10p	10p	10p	10p	F
C3	1.8p	1.8p	1.8p	1.8p	F
*C4	0.56p	0.56p	0.56p	0.56p	F
C6	470p	470p	470p	470p	F
C7	150p	150p	150p	150p	F
*C8	1.5p	1.5p	—	—	F
C9	100p	100p	100p	100p	
*C11	—	—	—	—	F

Notes:
1. S1 is the SAW resonator, and ±700KHz frequency difference is acceptable for 2dB sensitivity variation.
2. The data filter and slicer are optimized for 1K ~ 5Kbps data rate in this application circuit.
3. * (C4, C8 and C11) means the optional component.

TEST BOARD LAYOUT



<Top Side>



<Bottom Side>

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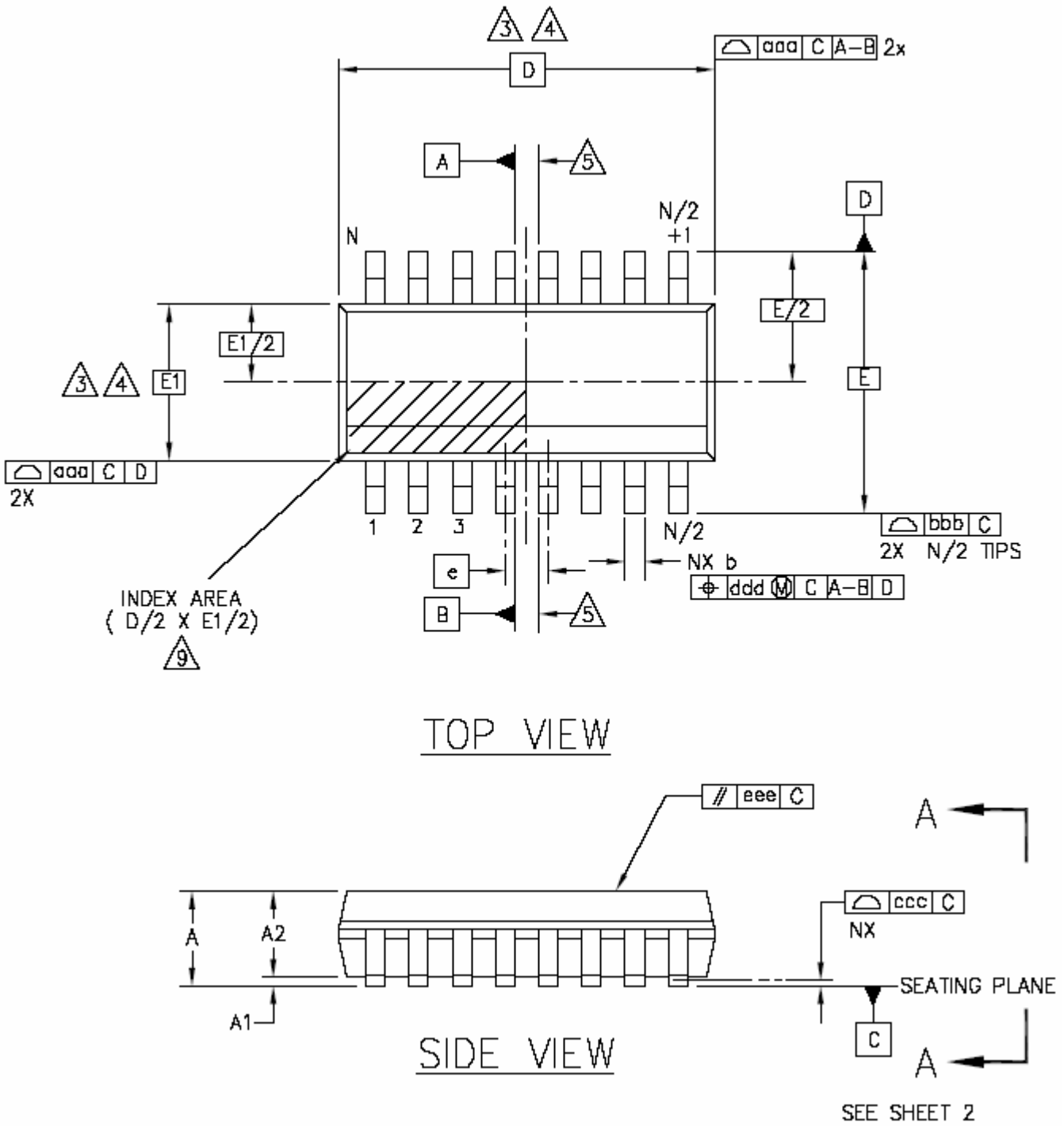
ORDER INFORMATION

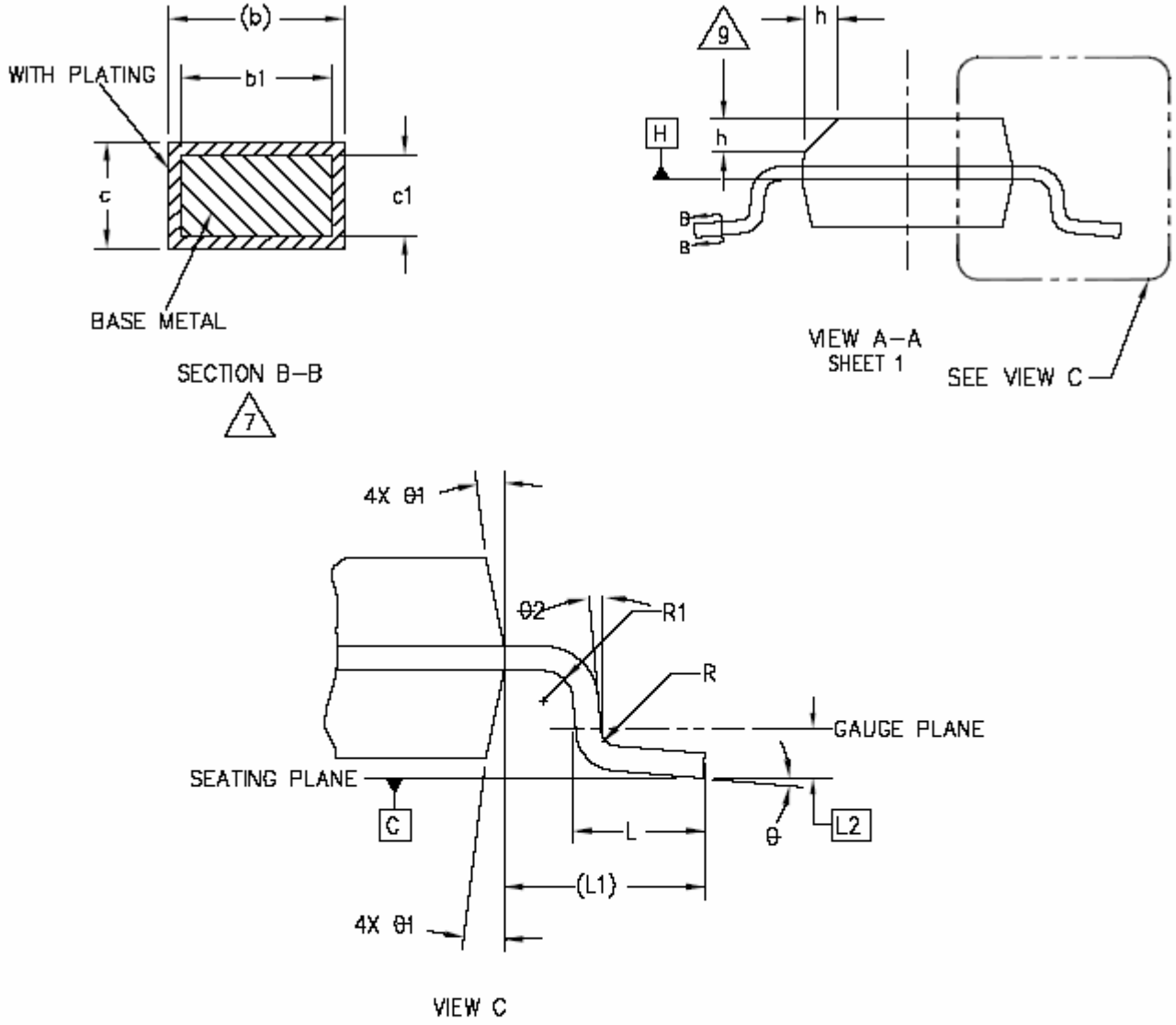
Valid Part Number	Package Type	Top Code
PT4316-S (L)	16 Pins, SOP, 150mil	PT4316-S
PT4316-X (L)	16 Pins, SSOP, 150mil	PT4316-X

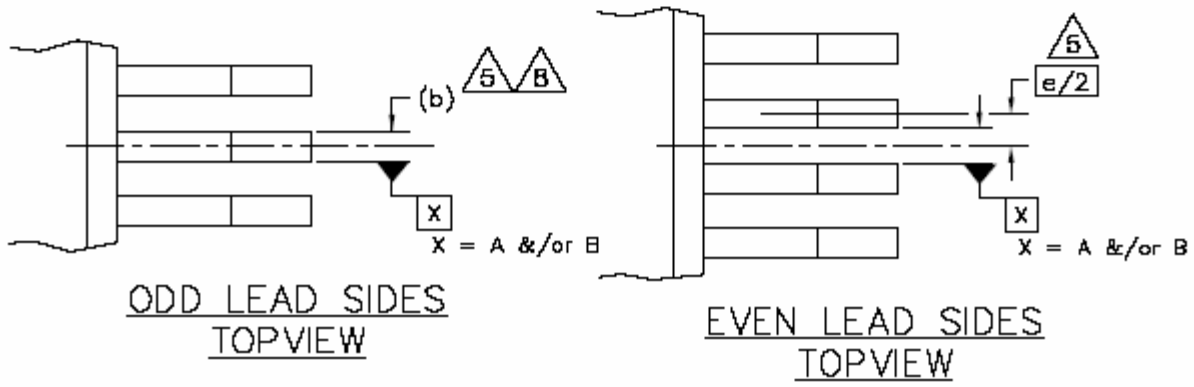
Notes:
1. (L) means Lead Free.
2. The Lead Free mark is placed in-front of the date code.

PACKAGE INFORMATION

16 PINS, SOP, 150MIL




(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
9
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C


(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	9.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=16)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AC.

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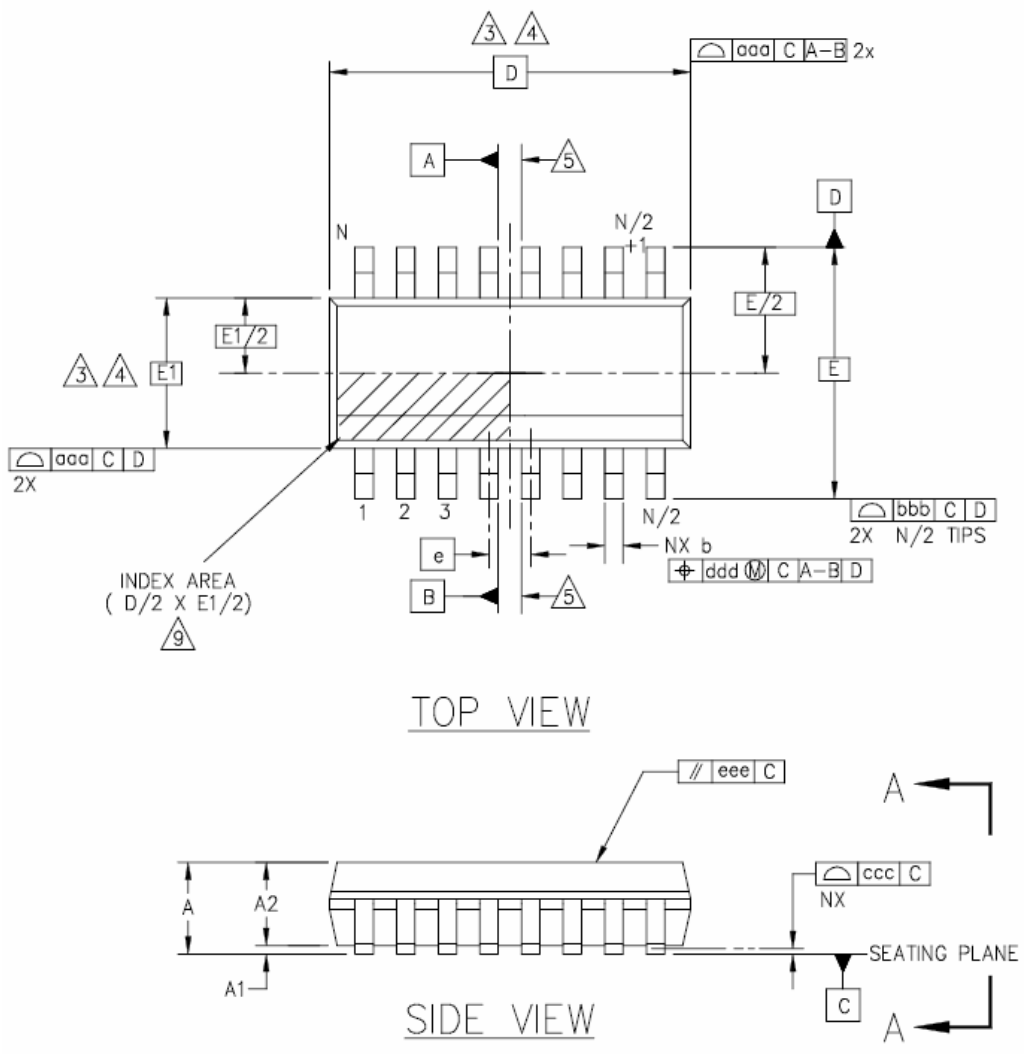
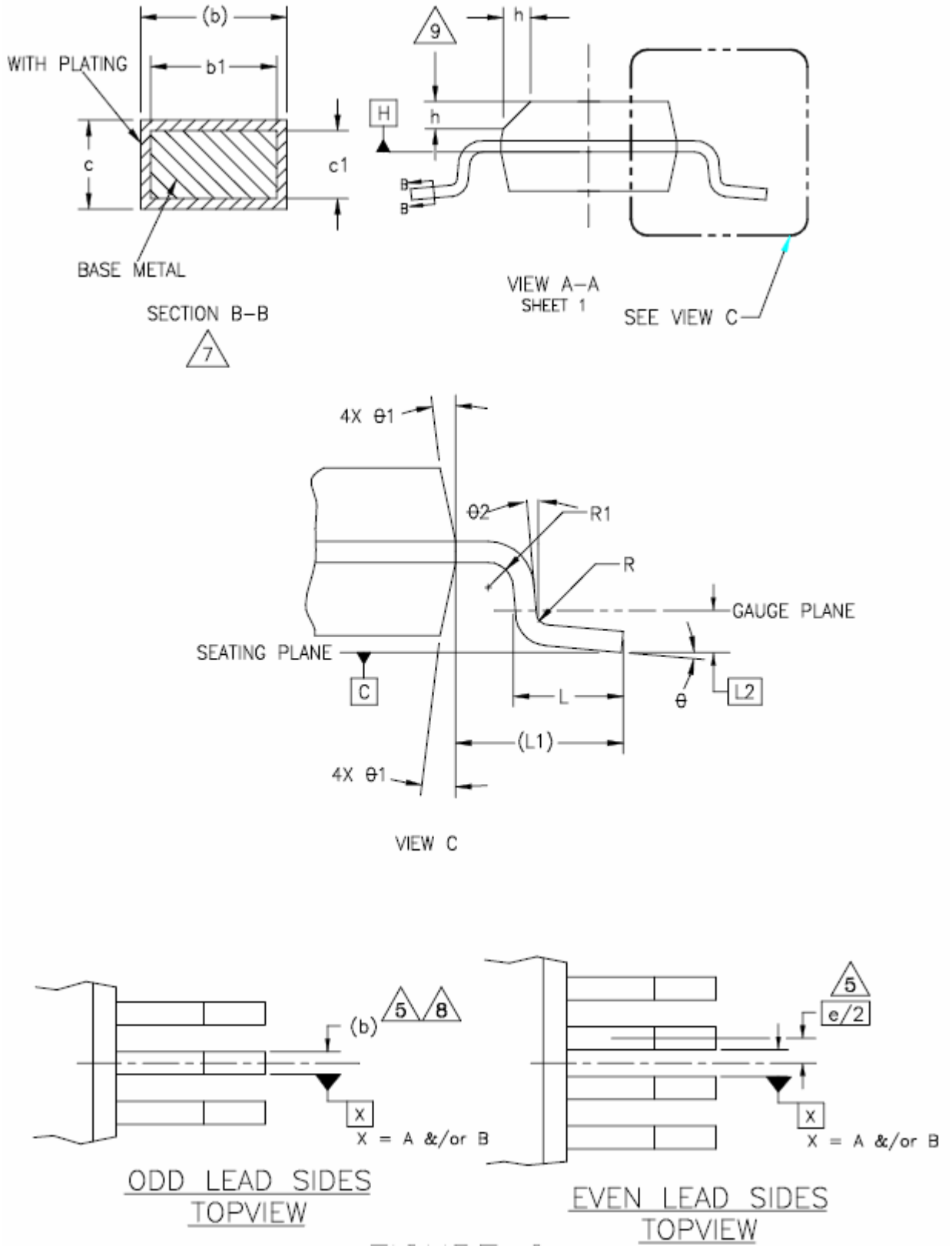
16 PINS, SSOP, 150MIL




(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B-B
7
9
h
H
h
B
B
VIEW A-A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
(b)
5
8
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Nom.	Max.
A	0.053	-	0.069
A1	0.004	-	0.010
A2	0.049	-	0.065
b	0.008	-	0.012
b1	0.008	0.010	0.011
c	0.006	-	0.010
c1	0.006	0.008	0.009
D	0.193 BSC		
E	0.236 BSC		
E1	0.154 BSC		
e	0.025 BSC		
L	0.016	-	0.050
L1	0.041 REF		
L2	0.010 BSC		
R	0.003	-	-
R1	0.003	-	-
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-
aaa	0.004		
bbb	0.008		
ccc	0.004		
ddd	0.007		
eee	0.004		

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimensions in inches (angles in degrees)
3. Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.006” per end. Dimension E1 does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed “0.006” per side. D1 and E1 dimensions are determined at dutum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic.
5. Datums A and B to be determined at datum H.
6. N is the maximum number of terminal position. (N=16)
7. The dimensions apply to the flat section of the lead between 0.004 to 0.010 inches from the lead tip.
8. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.004” total in excess of b dimension at maximum material condition. The dambar can not be located on the lower radius of the foot.
9. Refer to JEDEC MO-137 variation AB.

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