



PRELIMINARY

## DUAL TVS ZENER FOR ESD / TRANSIENT PROTECTION

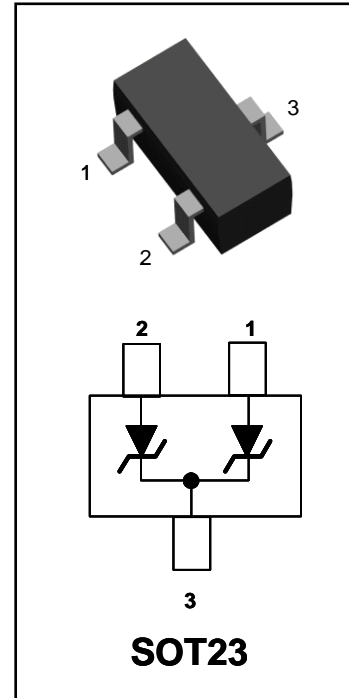
This Dual Zener ESD/Transient Protector with a Common Cathode Configuration has been designed to protect Sensitive Equipment against ESD and prevent Latch-Up events. The combination of a dual device protects up to two data lines in a single package giving the advantage of board space savings where this is a premium.

### SPECIFICATION FEATURES

- Working Peak Reverse Voltage of 15V and 22V
- Maximum Leakage Current of 100nA and 50nA @ VWRM
- IEC61000-4-2 Compliance 15kV Air, 8kV Contact Discharge
- Industry Standard SOT23 Package

### APPLICATIONS

- Data Transmission Line Ports
- Computer Monitor Interface Port Protection
- Portable Consumer Electronics
- Instrumentation Equipment



### MAXIMUM RATINGS

Rating	Symbol	Value	Units
Peak Pulse Power 8x20µsec Waveform	$P_{pp}$	150	W
Peak Pulse Power 10x1000µsec Waveform		25	W
ESD Voltage (HBM)	$V_{ESD}$	>25	kV
Operating Temperature Range	$T_J$	-55 to +125	°C
Storage Temperature Range	$T_{stg}$	-55 to +150	°C
Lead Soldering Temperature (max 10 secs)	$T_L$	260	°C

### ELECTRICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$

#### PJMBZ15VD

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				12	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 1\text{mA}$	14.25		15.75	V
Reverse Leakage Current	$I_R$	$V_R = 15\text{V}$			100	nA
Clamping Voltage (8x20µsec)	$V_{cl}$	$I_{pp} = 6\text{Amps}$			24	V
Clamping Voltage (10x1000µsec)	$V_{cl}$	$I_{pp} = 1\text{Amps}$			23	V
Maximum Peak Pulse Current	$I_{pp}$	8x20 µsec Waveform			7	A
Off State Junction Capacitance	$C_j$	0 Vdc Bias f = 1MHz Between I/O pins and pin 3			80	pF



ELECTRICAL CHARACTERISTICS  $T_j = 25^\circ\text{C}$

PJMBZ27VC

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	$V_{WRM}$				22	V
Reverse Breakdown Voltage	$V_{BR}$	$I_{BR} = 1 \text{ mA}$	25.65		28.35	V
Reverse Leakage Current	$I_R$	$V_R = 22\text{V}$			50	nA
Clamping Voltage (8x20μsec)	$V_{cl}$	$I_{pp} = 4 \text{ Amps}$			36	V
Clamping Voltage (10x1000μsec)	$V_{cl}$	$I_{pp} = 0.85$			30	V
Maximum Peak Pulse Current	$I_{pp}$	8x20 μsec Waveform			5	A
Off State Junction Capacitance	$C_j$	0 Vdc Bias $f = 1\text{MHz}$ Between I/O pins and pin 3			50	pF

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PACKAGE LAYOUT AND PAD DIMENSIONS

