TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L Series

TMP93PW46A

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

CAUTION
How to release the HALT mode

Usually, interrupts can release all halts status. However, the interrupts = ($\overline{NMI}$, INT0), which can release the HALT mode may not be able to do so if they are input during the period CPU is shifting to the HALT mode (for about 3 clocks of f_{FPH}) with IDLE1 or STOP mode (IDLE2/RUN are not applicable to this case). (In this case, an interrupt request is kept on hold internally.)

If another interrupt is generated after it has shifted to HALT mode completely, halt status can be released without difficultly. The priority of this interrupt is compare with that of the interrupt kept on hold internally, and the interrupt with higher priority is handled first followed by the other interrupt.

Low Voltage/Low Power

CMOS 16-Bit Microcontroller

TMP93PW46AF

1. Outline and Device Characteristics

The TMP93PW46A is OTP type MCU which includes 128-Kbyte One-time PROM. Using the adapter-socket, you can write and verify the data for the TMP93CW46A by general EPROM programmer.

The TMP93PW46A has the same pin-assignment as the TMP93CW46A (Mask ROM type).

Writing the program to built-in PROM, the TMP93PW46A operates as the same way as the TMP93CW46A.

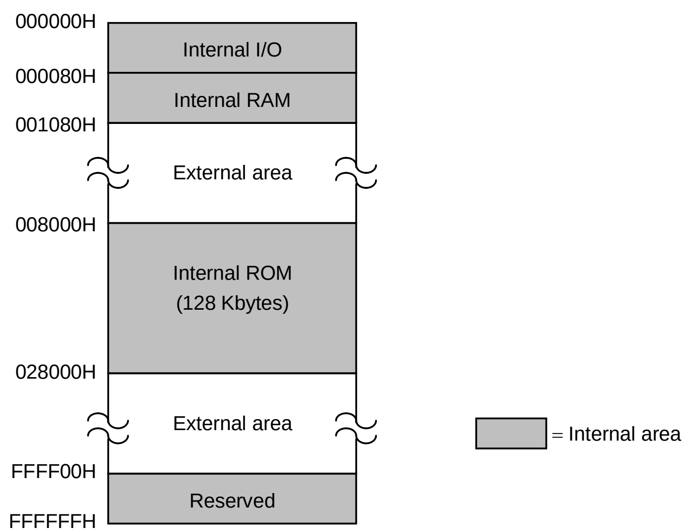


Figure 1.1 Memory map of TMP93CW46A/TMP93PW46A

MCU	ROM	RAM	Package	Adapter Socket
TMP93PW46AF	OTP 128 Kbytes	4 Kbytes	P-LQFP100-1414-0.50F	BM11129

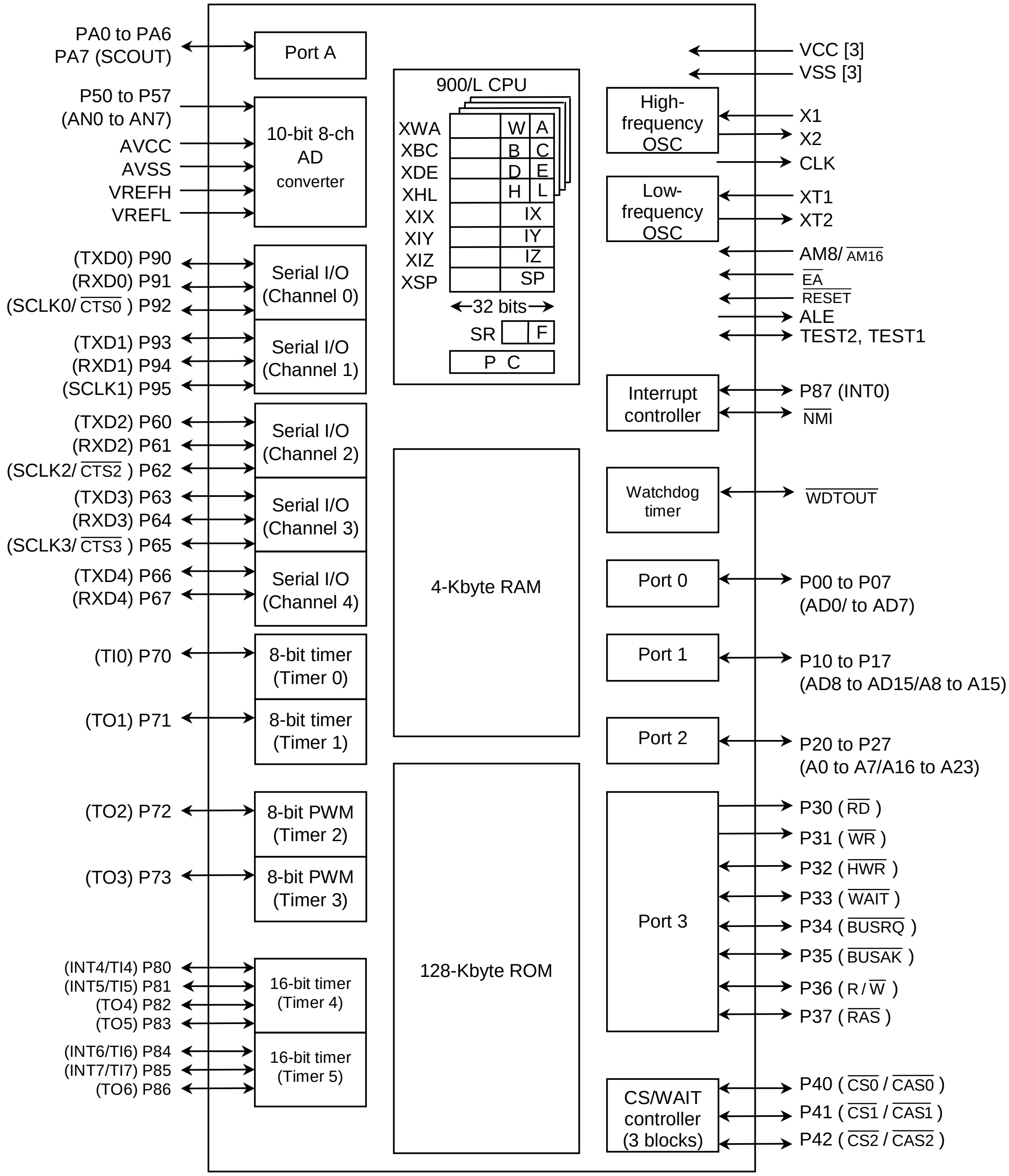


Figure 1.2 TMP93PW46A Block Diagram

2. Pin Assignment and Functions

The assignment of input/output pins for the TMP93PW46A their names and outline functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93PW46AF.

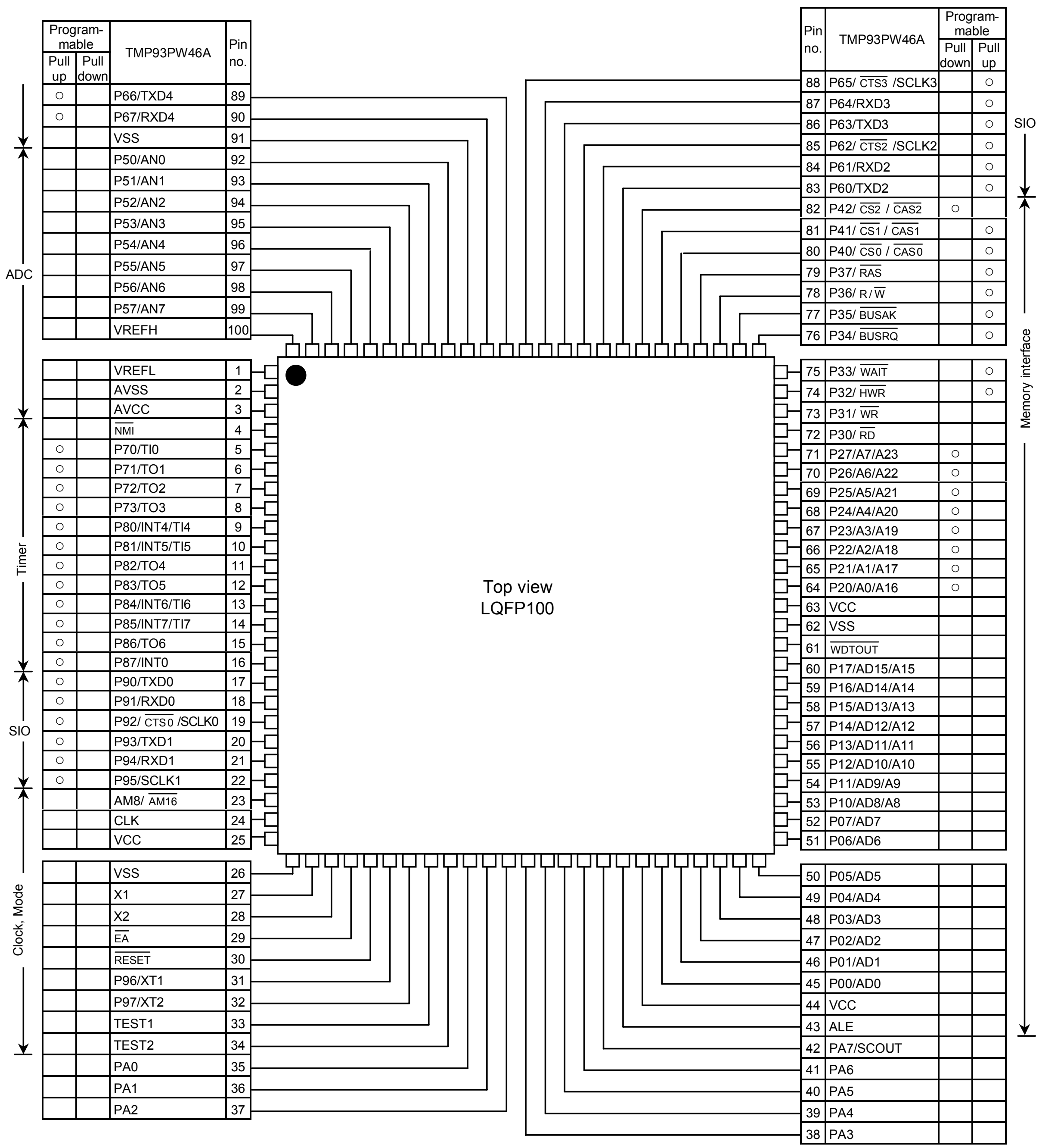


Figure 2.1.1 Pin Assignment (100-Pin LQFP)

2.2 Pin Names and Functions

(1) Pin function of TMP93PW46A in MCU mode.

Table 2.2.1 Name and Function in MCU Mode (1/4)

Pin Name	Number of Pins	I/O	Function
P00 to P07 AD0 to AD7	8	I/O 3 states	Port 0: I/O port that allows selection of I/O on a bit basis address/data (lower): Bits 0 to 7 for address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O 3 states Output	Port 1: I/O port that allows selection of I/O on a bit basis Address data (upper): Bits 8 to 15 of address/data bus Address: Bits 8 to 15 of address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: I/O port that allows selection of I/O on a bit basis (with pull-down resistor) Address: Bits 0 to 7 of address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output port Read: Strobe signal for reading external memory
P31 $\overline{WR}$	1	Output Output	Port 31: Output port Write: Strobe signal for writing data on pins AD0 to AD7
P32 $\overline{HWR}$	1	I/O Output	Port 32: I/O port (with pull-up resistor) High write: Strobe signal for writing data on pins AD8 to AD15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: I/O port (with pull-up resistor) Wait: Pin used to request CPU bus wait
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: I/O port (with pull-up resistor) Bus request: Signal used to request high impedance for AD0 to AD15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins. (For external DMAC)
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: I/O port (with pull-up resistor) Bus acknowledge: Signal indicating that AD0 to AD15, A0 to A23, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, $\overline{RAS}$, $\overline{CS0}$, $\overline{CS1}$, and $\overline{CS2}$ pins are at high impedance after receiving BUSRQ. (For external DMAC)
P36 R/$\overline{W}$	1	I/O Output	Port 36: I/O port (with pull-up resistor) Read/write: 1 represents read or dummy cycle. 0 represents write cycle.
P37 $\overline{RAS}$	1	I/O Output	Port 37: I/O port (with pull-up resistor) Row address strobe: Outputs "$\overline{RAS}$" strobe for DRAM.
P40 $\overline{CS0}$ $\overline{CAS0}$	1	I/O Output Output	Port 40: I/O port (with pull-up resistor) Chip select 0: Outputs 0 when address is within specified address area. Column address strobe 0: Outputs $\overline{CAS}$ strobe for DRAM when address is within specified address area.

Note: This device's built-in memory or built-in I/O cannot be accessed with the external DMA controller using the $\overline{BUSRQ}$ and $\overline{BUSAK}$ signals.

Table 2.2.2 Name and Function in MCU Mode (2/4)

Pin Name	Number of Pins	I/O	Function
P41 $\overline{CS1}$ $\overline{CAS1}$	1	I/O Output Output	Port 41: I/O port (with pull-up resistor) Chip select 1: Outputs 0 if address is within specified address area. Column address strobe 1: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P42 $\overline{CS2}$ $\overline{CAS2}$	1	I/O Output Output	Port 42: I/O port (with pull-down resistor) Chip select 2: Outputs 0 if address is within specified address area. Column address strobe 2: Outputs $\overline{CAS}$ strobe for DRAM if address is within specified address area.
P50 to P57 AN0 to AN7	8	Input Input	Port 5: Input port Analog input: Analog signal input for AD converter
VREFH	1	Input	Pin for high level reference voltage input to AD converter
VREFL	1	Input	Pin for low level reference voltage input to AD converter
P60 TXD2	1	I/O Output	Port 60: I/O port (with pull-up resistor) Serial send data 2
P61 RXD2	1	I/O Input	Port 61: I/O port (with pull-up resistor) Serial receive data 2
P62 $\overline{CTS2}$ SCLK2	1	I/O Input I/O	Port 62: I/O port (with pull-up resistor) Serial data send enable 2 (Clear to send) Serial clock I/O 2
P63 TXD3	1	I/O Output	Port 63: I/O port (with pull-up resistor) Serial send data 3
P64 RXD3	1	I/O Input	Port 64: I/O port (with pull-up resistor) Serial receive data 3
P65 $\overline{CTS3}$ SCLK3	1	I/O Input I/O	Port 65: I/O port (with pull-up resistor) Serial data send enable 3 (Clear to send) Serial clock I/O 3
P66 TXD4	1	I/O Output	Port 66: I/O port (with pull-up resistor) Serial send data 4
P67 RXD4	1	I/O Input	Port 67: I/O port (with pull-up resistor) Serial receive data 4
P70 TI0	1	I/O Input	Port 70: I/O port (with pull-up resistor) Timer input 0: Timer 0 input
P71 TO1	1	I/O Output	Port 71: I/O port (with pull-up resistor) Timer output 1: Timer 0 or 1 output
P72 TO2	1	I/O Output	Port 72: I/O port (with pull-up resistor) PWM output 2: 8-bit PWM timer 2 output
P73 TO3	1	I/O Output	Port 73: I/O port (with pull-up resistor) PWM output 3: 8-bit PWM timer 3 output

Table 2.2.3 Name and Function in MCU Mode (3/4)

Pin Name	Number of Pins	I/O	Function
P80 TI4 INT4	1	I/O Input Input	Port 80: I/O port (with pull-up resistor) Timer input 4: Timer 4 count/capture trigger signal input Interrupt request pin 4: Interrupt request pin with programmable rising/falling edge
P81 TI5 INT5	1	I/O Input Input	Port 81: I/O port (with pull-up resistor) Timer input 5: Timer 4 count/capture trigger signal input Interrupt request pin 5: Interrupt request pin with rising edge
P82 TO4	1	I/O Output	Port 82: I/O port (with pull-up resistor) Timer output 4: Timer 4 output pin
P83 TO5	1	I/O Output	Port 83: I/O port (with pull-up resistor) Timer output 5: Timer 4 output pin
P84 TI6 INT6	1	I/O Input Input	Port 84: I/O port (with pull-up resistor) Timer input 6: Timer 5 count/capture trigger signal input Interrupt request pin 6: Interrupt request pin with programmable rising/falling edge
P85 TI7 INT7	1	I/O Input Input	Port 85: I/O port (with pull-up resistor) Timer input 7: Timer 5 count/capture trigger signal input Interrupt request pin 7: Interrupt request pin with rising edge
P86 TO6	1	I/O Output	Port 86: I/O port (with pull-up resistor) Timer output 6: Timer 5 output pin
P87 INT0	1	I/O Input	Port 87: I/O port (with pull-up resistor) Interrupt request pin 0: Interrupt request pin with programmable level/rising edge
P90 TXD0	1	I/O Output	Port 90: I/O port (with pull-up resistor) Serial send data 0
P91 RXD0	1	I/O Input	Port 91: I/O port (with pull-up resistor) Serial receive data 0
P92 $\overline{CTS0}$ SCLK0	1	I/O Input I/O	Port 92: I/O port (with pull-up resistor) Serial data send enable 0 (Clear to send) Serial clock I/O 0
P93 TXD1	1	I/O Output	Port 93: I/O port (with pull-up resistor) Serial send data 1
P94 RXD1	1	I/O Input	Port 94: I/O port (with pull-up resistor) Serial receive data 1
P95 SCLK1	1	I/O I/O	Port 95: I/O port (with pull-up resistor) Serial clock I/O 1
PA0 to PA5	6	I/O	Port A0 to A5: I/O ports (Large current output)
PA6	1	I/O	Port A6: I/O port

Table 2.2.4 Name and Function in MCU Mode (4/4)

Pin Name	Number of Pins	I/O	Function
PA7 SCOUT	1	I/O Output	Port A7: I/O port System clock output: Outputs system clock or 2 oscillation clock for synchronizing to external circuit.
$\overline{\text{WDTOUT}}$	1	Output	Watchdog timer output pin
$\overline{\text{NMI}}$	1	Input	Non-maskable interrupt request pin: Interrupt request pin with falling edge. Can also be operated at rising edge by program.
CLK	1	Output	Clock output: Outputs "System clock ÷ 2" clock. Pulled up during reset. Can be disabled for reducing noise.
$\overline{\text{EA}}$	1	Input	Fixed to "1".
AM8/ $\overline{\text{AM16}}$	1	Input	Fixed to "1".
ALE	1	Output	Address latch enable (Can be disabled for reducing noise.)
$\overline{\text{RESET}}$	1	Input	Reset: Initializes LSI. (with pull-up resistor)
X1/X2	2	I/O	High-frequency oscillator connecting pin
XT1 P96	1	Input I/O	Low-frequency oscillator connecting pin Port 96: I/O port (Open-drain output)
XT2 P97	1	Output I/O	Low-frequency oscillator connecting pin Port 97: I/O port (Open-drain output)
TEST1/TEST2	2	Output/Input	TEST1 should be connected with TEST2 pin. Do not connect to any other pins.
VCC	3		Power supply pin
VSS	3		GND pin (0 V)
AVCC	1		Power supply pin for AD converter
AVSS	1		GND pin for AD converter (0 V)

Note: Built-in pull-up/pull-down resistors can be released from the pins other than the $\overline{\text{RESET}}$ pin by software.

2.3 PROM Mode

Table 2.3.1 Name and Function of PROM Mode

Pin Function	Number of Pins	Input/ Output	Function	Pin Name (MCU mode)
A7 to A0	8	Input	Memory address of program	P27 to P20
A15 to A8	8	Input		P17 to P10
A16	1	Input		P33
D7 to D0	8	I/O	Memory data of program	P07 to P00
$\overline{CE}$	1	Input	Chip enable	P32
$\overline{OE}$	1	Input	Output enable	P30
$\overline{PGM}$	1	Input	Program control	P31
VPP	1	Power supply	12.75 V/5 V (Power supply of program)	$\overline{EA}$
VCC	4	Power supply	6.25 V/5 V	VCC, AVCC
VSS	4	Power supply	0 V	VSS, AVSS

Pin Function	Number of Pins	Input/ Output	Pin State
P34	1	Input	Fix to low level (Security pin)
$\overline{RESET}$	1	Input	Fix to low level (PROM mode)
CLK	1	Input	
ALE	1	Output	Open
X1	1	Input	Self oscillation with resonator
X2	1	Output	
P42 to P40 P37 to P35 AM8/$\overline{AM16}$	7	Input	Fix to high level
TEST1, TEST2	2	Input/ Output	TEST1 should be connected with TEST2 pin. Do not connect to any other pins.
P57 to P50 P67 to P60 P73 to P70 P87 to P80 P97 to P90 PA7 to PA0 VREFH VREFL $\overline{NMI}$ $\overline{WDTOUT}$	48	I/O	Open

3. Operation

This section describes the functions and basic operational blocks of the TMP93PW46A.

The TMP93PW46A has PROM in place of the mask ROM which is included in the TMP93CW46A. The other configuration and functions are the same as the TMP93CW46A. Regarding the function of the TMP93PW46A, which is not described herein, see the TMP93CW46A.

The TMP93PW46A has two operational modes: MCU mode and PROM mode.

3.1 MCU Mode

(1) Mode setting and function

The MCU mode is set by releasing the CLK pin (Pin open). In the MCU mode, the operation is the same as TMP93CW46A.

(2) Memory map

The memory map of TMP93PW46A is the same as that of TMP93CW46A. The memory map in MCU mode is shown in Figure 3.2.1, and the memory map in PROM mode is shown in Figure 3.2.2.

3.2 Memory Map

Figure 3.2.1 and 3.2.2 are the memory map of the TMP93PW46A.

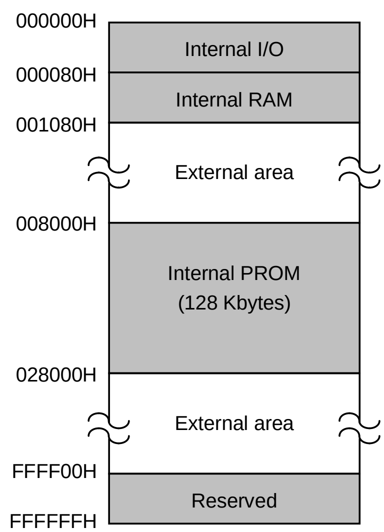


Figure 3.2.1 Memory Map in MCU Mode

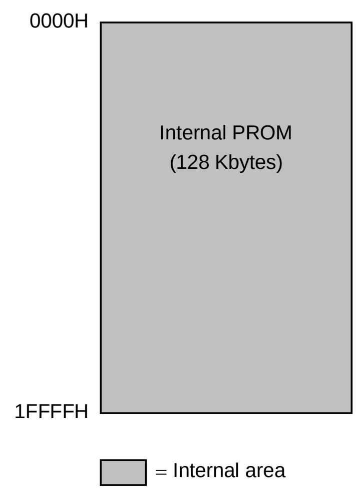


Figure 3.2.2 Memory Map in PROM Mode

3.3 PROM Mode

(1) Mode setting and programming

PROM mode is set by setting the $\overline{\text{RESET}}$ and CLK pins to the “L” level. The programming and verification for the internal PROM is achieved by using a general PROM programmer with the adaptor socket.

1. OTP adaptor

   BM11129: TMP93PW46AF adaptor

2. Setting OTP adaptor

   Set the switch (SW1) to N side.

3. Setting PROM programmer

   i) Set PROM type to TC571000D.

   Size: 1 Mbits (128 K × 8 bits)

   VPP: 12.75 V

   t_{PW}: 100 μs

   The electric signature mode (Hereinafter referred to as “signature”) is not supported. Therefore using signature with PROM programmer applies voltage of 12.75 V to pin 9 (A9) of the address, and the device is damaged. Do not use signature.

   ii) Transferring the data (Copy)

   In TMP93PW46A, PROM is placed on addresses 00000H to 1FFFFH in PROM mode, and addresses 08000H to 27FFFH in MCU mode. Therefore data should be transferred to addresses 00000H to 1FFFFH in PROM mode using the object converter (tuconv) or the block transfer mode. (See instruction manual of PROM programmer.)

   iii) Setting program address

   Start address: 00000H

   End address: 1FFFFH

4. Programming

   Program/verify according to the procedures of PROM programmer.

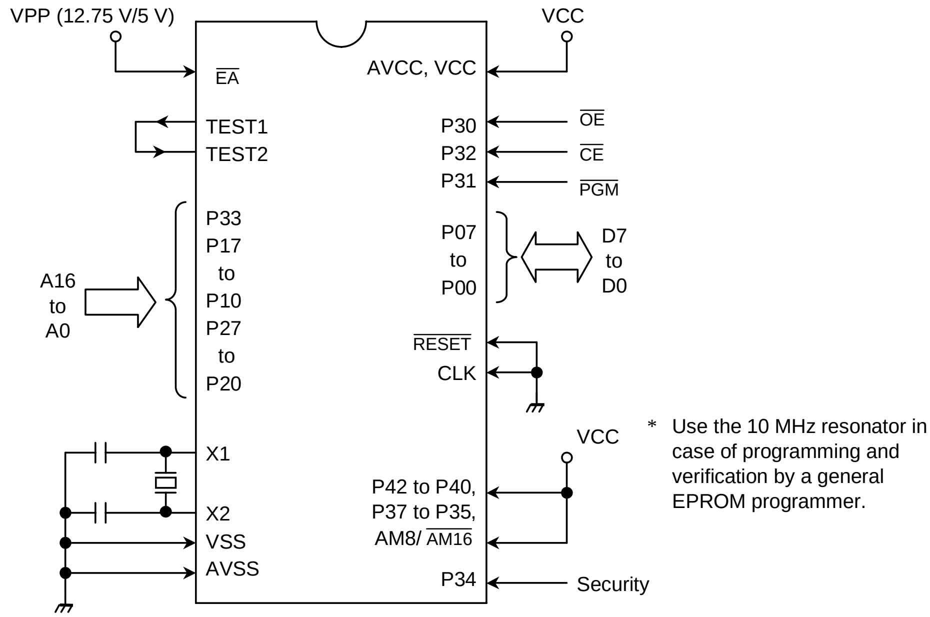


Figure 3.3.1 PROM Mode Pin Setting

(2) Programming flow chart

The programming mode is set by applying 12.75 V (Programming voltage) to the VPP pin when the following pins are set as follows,

(V_{CC}: 6.25 V, $\overline{\text{RESET}}$: "L" level, CLK: "L" level).

While address and data are fixed and $\overline{\text{CE}}$ pin is set to "L" level, 0.1 ms of "L" level pulse is applied to $\overline{\text{PGM}}$ pin to program the data.

Then the data in the address is verified.

If the programmed data is incorrect, another 0.1 ms pulse is applied to $\overline{\text{PGM}}$ pin.

This programming procedure is repeated until correct data is read from the address (25 times maximum).

Subsequently, all data are programmed in all addresses.

The verification for all data is done under the condition of $V_{PP} = V_{CC} = 5$ V after all data were written.

Figure 3.3.2 shows the programming flowchart.

High speed program writing.

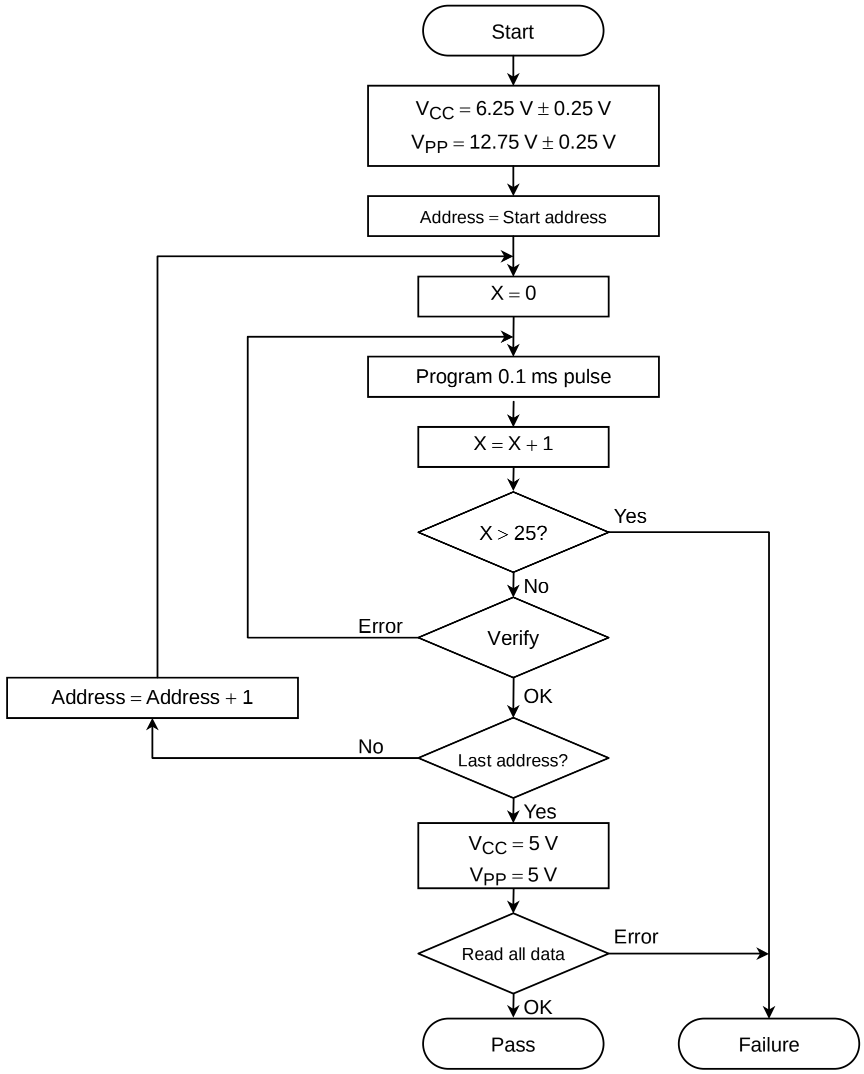


Figure 3.3.2 Flowchart

(3) Security bit

The TMP93PW46A has a security bit in PROM cell. If the security bit is programmed to “0”, the content of the PROM is disable to be read in PROM mode.

How to program the security bit

1) Set the PROM mode.
2) Set the security pin (Port 34) to “1”.
3) Set programming address to “00000H”.
4) Set programming data to “FEH”.

4. Electrical Characteristic

“X” used in an expression shows a frequency of clock f_{FPH} selected by SYSCR1<SYSCK>. If a clock gear or a low speed oscillator is selected, a value of “X” is different. The value as an example is calculated at fc, gear = 1/fc (SYSCR1<SYSCK, GEAR2:0> = “0000”).

4.1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{CC}	−0.5 to 6.5	V
Input voltage	V_{IN}	−0.5 to V_{CC} + 0.5	V
Output current (Per one pin), ports PA0 to PA5	IO_{L1}	20	mA
Output current (Per one pin), excluding ports PA0 to PA5	IO_{L2}	2	mA
Output current (Total of ports PA0 to PA5)	ΣI_{OL1}	80	mA
Output current (Total)	ΣI_{OL}	120	mA
Output current (Total)	ΣI_{OH}	−80	mA
Power dissipation (Ta = 85°C)	P_D	600	mW
Soldering temperature (10 s)	T_{SOLDER}	260	°C
Storage temperature	T_{STG}	−65 to 150	°C
Operating temperature	T_{OPR}	−40 to 85	°C

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

4.2 DC Characteristics (1/2) (V_{SS} = 0 V, Ta = −40 to 85°C)

	Parameter	Symbol	Condition		Min	Typ. (Note)	Max	Unit
Power supply voltage ($AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$)		V_{CC}	fc = 4 to 20 MHz	fs = 30 to 34 kHz	4.5		5.5	V
			fc = 4 to 12.5 MHz		2.7			
Input low voltage	AD0 to AD15	V_{IL}	V_{CC} ≥ 4.5 V		−0.3		0.8	V
			V_{CC} < 4.5 V				0.6	
	Port 2 to port A (except P87)	V_{IL1}	V_{CC} = 2.7 to 5.5 V				0.3 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$, INT0	V_{IL2}					0.25 V_{CC}	
	$\overline{EA}$, AM8/$\overline{AM16}$	V_{IL3}					0.3	
	X1	V_{IL4}					0.2 V_{CC}	
Input high voltage	AD0 to AD15	V_{IH}	V_{CC} ≥ 4.5 V		2.2		V_{CC} + 0.3	
			V_{CC} < 4.5 V		2.0			
	Port 2 to port A (except P87)	V_{IH1}	V_{CC} = 2.7 to 5.5 V		0.7 V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$, INT0	V_{IH2}			0.75 V_{CC}			
	$\overline{EA}$, AM8/$\overline{AM16}$	V_{IH3}			V_{CC} − 0.3			
	X1	V_{IH4}			0.8 V_{CC}			

Note: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

4.2 DC Characteristics (2/2) (V_{SS} = 0 V, Ta = –40 to 85°C)

Parameter	Symbol	Condition	Min	Typ. (Note 1)	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 1.6 mA (V_{CC} = 2.7 to 5.5 V)			0.45	V
Output low current (PA0 to PA5)	I_{OLA}	V_{OL} = 1.0 V (V_{CC} = 2.7 to 5.5 V)	10			mA
Output high voltage	V_{OH1}	I_{OH} = – 400 μA (V_{CC} = 3 V ± 10%)	2.4			V
	V_{OH2}	I_{OH} = – 400 μA (V_{CC} = 5 V ± 10%)	4.2			
Darlington drive current (8 output pins max)	I_{DAR} (Note 2)	V_{EXT} = 1.5 V R_{EXT} = 1.1 kΩ (Vcc = 5 V ± 10% only)	– 1.0		–3.5	mA
Input leakage current	I_{LI}	0.0 ≤ V_{IN} ≤ V_{CC}		0.02	±5	μA
Output leakage current	I_{LO}	0.2 ≤ V_{IN} ≤ V_{CC} – 0.2		0.05	±10	
Power down voltage (at STOP, RAM backup)	V_{STOP}	V_{IL2} = 0.2 V_{CC}, V_{IH2} = 0.8 V_{CC}	2.0		6.0	V
$\overline{\text{RESET}}$ pull-up resistor	R_{RST}	Vcc = 5 V ± 10%	50		150	kΩ
		Vcc = 3 V ± 10%	80		200	
Pin capacitance	C_{IO}	fc = 1 MHz			10	pF
Schmitt width $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, INT0	V_{TH}		0.4	1.0		V
Programmable Pull-down resistor	R_{KL}	V_{CC} = 5 V ± 10%	10		80	kΩ
		V_{CC} = 3 V ± 10%	30		150	
Programmable Pull-up resistor	R_{KH}	V_{CC} = 5 V ± 10%	50		150	
		V_{CC} = 3 V ± 10%	100		300	
NORMAL (Note 3)	I_{CC}	V_{CC} = 5 V ± 10% fc = 20 MHz		35	42	mA
RUN				30	37	
IDLE2				18	25	
IDLE1				3.5	5	
NORMAL (Note 3)		V_{CC} = 3 V ± 10% fc = 12.5 MHz (Typ.: V_{CC} = 3.0 V)		11	16	
RUN				9	13.5	
IDLE2				5.5	7.5	
IDLE1				1	1.5	
SLOW (Note 3)		V_{CC} = 3 V ± 10% fs = 32.768 kHz (Typ.: V_{CC} = 3.0 V)		35	50	μA
RUN				28	42	
IDLE2				20	33	
IDLE1				9	15	
STOP		Ta ≤ 50°C, V_{CC} = 2.7 to 5.5 V		0.2	10	
		Ta ≤ 70°C			20	
		Ta ≤ 85°C			50	

Note 1: Typical values are for Ta = 25°C and V_{CC} = 5 V unless otherwise noted.

Note 2: I_{DAR} is guranteed for total of up to 8 ports.

4.3 AC Characteristics

(1) V_{CC} = 5 V ± 10%

No.	Parameter	Symbol	Variable		16 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
1	Osc. period (= x)	t_{OSC}	50 ns	33.3 μs	62.5 ns		50		ns
2	CLK pulse width	t_{CLK}	2x – 40		85		60		ns
3	A0 to A23 valid → CLK hold	t_{AK}	0.5x – 20		11		5		ns
4	CLK valid → A0 to A23 hold	t_{KA}	1.5x – 70		24		5		ns
5	A0 to A15 valid → ALE fall	t_{AL}	0.5x – 15		16		10		ns
6	ALE fall → A0 to A15 hold	t_{LA}	0.5x – 20		11		5		ns
7	ALE high pulse width	t_{LL}	x – 40		23		10		ns
8	ALE fall → $\overline{RD}$ / $\overline{WR}$ fall	T_{LC}	0.5x – 25		6		0		ns
9	$\overline{RD}$ / $\overline{WR}$ rise → ALE rise	t_{CL}	0.5x – 20		11		5		ns
10	A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACL}	x – 25		38		25		ns
11	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACH}	1.5x – 50		44		25		ns
12	$\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold	T_{CA}	0.5x – 25		6		0		ns
13	A0 to A15 valid → D0 to D15 input	t_{ADL}		3.0x – 55		133		95	ns
14	A0 to A23 valid → D0 to D15 input	t_{ADH}		3.5x – 65		154		110	ns
15	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.0x – 60		65		40	ns
16	$\overline{RD}$ low pulse width	t_{RR}	2.0x – 40		85		60		ns
17	$\overline{RD}$ rise → D0 to D15 hold	t_{HR}	0		0		0		ns
18	$\overline{RD}$ rise → A0 to A15 output	t_{RAE}	x – 15		48		35		ns
19	$\overline{WR}$ low pulse width	t_{WW}	2.0x – 40		85		60		ns
20	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 55		70		45		ns
21	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	0.5x – 15		16		10		ns
22	A0 to A23 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode]	t_{AWH}		3.5x – 90		129		85	ns
23	A0 to A15 valid → $\overline{WAIT}$ input [(1 + N) WAIT mode]	t_{AWL}		3.0x – 80		108		70	ns
24	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold [(1 + N) WAIT mode]	t_{CW}	2.0x + 0		125		100		ns
25	A0 to A23 valid → Port input	t_{APH}		2.5x – 120		36		5	ns
26	A0 to A23 valid → Port hold	t_{APH2}	2.5x + 50		206		175		ns
27	$\overline{WR}$ rise → Port valid	t_{CP}		200		200		200	ns
28	A0 to A23 valid → $\overline{RAS}$ fall	t_{ASRH}	1.0x – 40		23		10		ns
29	A0 to A15 valid → $\overline{RAS}$ fall	t_{ASRL}	0.5x – 15		16		10		ns
30	$\overline{RAS}$ fall → D0 to D15 input	t_{RAC}		2.5x – 70		86		55	ns
31	$\overline{RAS}$ fall → A0 to A15 hold	t_{RAH}	0.5x – 15		16		10		ns
32	$\overline{RAS}$ low pulse width	t_{RAS}	2.0x – 40		85		60		ns
33	$\overline{RAS}$ high pulse width	t_{RP}	2.0x – 40		85		60		ns
34	$\overline{CAS}$ fall → $\overline{RAS}$ rise	t_{RSH}	1.0x – 40		23		10		ns
35	$\overline{RAS}$ rise → $\overline{CAS}$ rise	t_{RSC}	0.5x – 25		6		0		ns
36	$\overline{RAS}$ fall → $\overline{CAS}$ fall	t_{RCD}	1.0x – 40		23		10		ns
37	$\overline{CAS}$ fall → D0 to D15 input	t_{CAC}		1.5x – 65		29		10	ns
38	$\overline{CAS}$ low pulse width	t_{CAS}	1.5x – 30		64		40		ns

AC measuring conditions

- Output level: High 2.2 V/Low 0.8 V, CL = 50 pF
  (However CL = 100 pF for AD0 to AD15, A0 to A23, ALE, $\overline{RD}$, $\overline{WR}$, $\overline{HWR}$, R/$\overline{W}$, CLK, $\overline{RAS}$, $\overline{CAS0}$ to $\overline{CAS2}$)
- Input level: High 2.4 V/Low 0.45 V (AD0 to AD15)
  High 0.8 × V_{CC}/Low 0.2 × V_{CC} (except for AD0 to AD15)

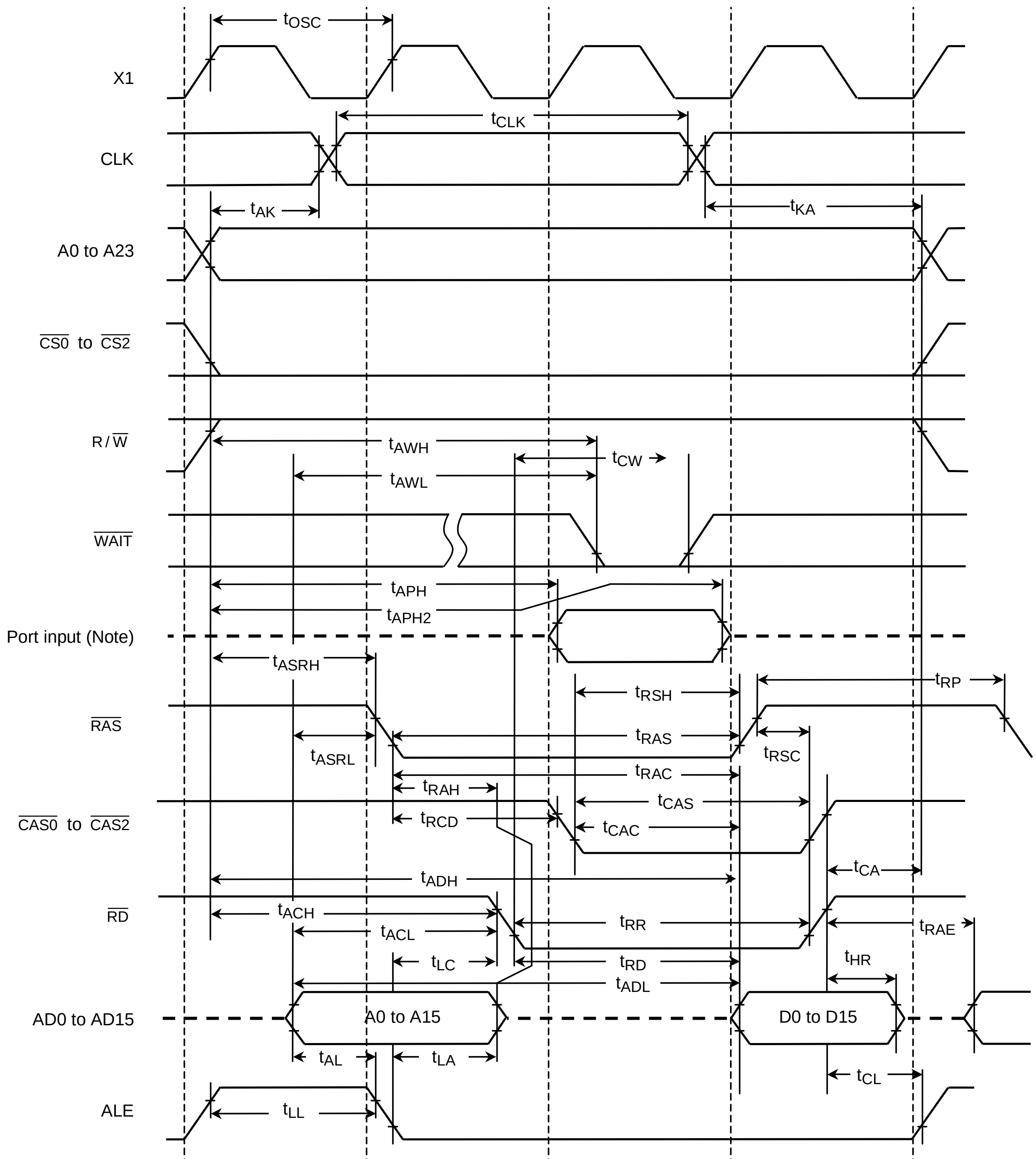
(2) $V_{CC} = 3\ V \pm 10\%$

No.	Parameter	Symbol	Variable		12.5 MHz		Unit
			Min	Max	Min	Max	
1	Osc. period (= x)	t_{OSC}	80 ns	33.3 μs	80 ns		
2	CLK pulse width	t_{CLK}	2x – 40		120		ns
3	A0 to A23 valid → CLK hold	t_{AK}	0.5x – 30		10		ns
4	CLK valid → A0 to A23 hold	t_{KA}	1.5x – 80		40		ns
5	A0 to A15 valid → ALE fall	t_{AL}	0.5x – 35		5		ns
6	ALE fall → A0 to A15 hold	t_{LA}	0.5x – 35		5		ns
7	ALE high pulse width	t_{LL}	x – 60		20		ns
8	ALE fall → $\overline{RD}$ / $\overline{WR}$ fall	t_{LC}	0.5x – 35		5		ns
9	$\overline{RD}$ / $\overline{WR}$ rise → ALE rise	t_{CL}	0.5x – 40		0		ns
10	A0 to A15 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACL}	x – 50		30		ns
11	A0 to A23 valid → $\overline{RD}$ / $\overline{WR}$ fall	t_{ACH}	1.5x – 50		70		ns
12	$\overline{RD}$ / $\overline{WR}$ rise → A0 to A23 hold	t_{CA}	0.5x – 40		0		ns
13	A0 to A15 valid → D0 to D15 input	t_{ADL}		3.0x – 110		130	ns
14	A0 to A23 valid → D0 to D15 input	t_{ADH}		3.5x – 125		155	ns
15	$\overline{RD}$ fall → D0 to D15 input	t_{RD}		2.0x – 115		45	ns
16	$\overline{RD}$ low pulse width	t_{RR}	2.0x – 40		120		ns
17	$\overline{RD}$ rise → D0 to D15 hold	t_{HR}	0		0		ns
18	$\overline{RD}$ rise → A0 to A15 output	t_{RAE}	x – 25		55		ns
19	$\overline{WR}$ low pulse width	t_{WW}	2.0x – 40		120		ns
20	D0 to D15 valid → $\overline{WR}$ rise	t_{DW}	2.0x – 120		40		ns
21	$\overline{WR}$ rise → D0 to D15 hold	t_{WD}	0.5x – 40		0		ns
22	A0 to A23 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode)	t_{AWH}		3.5x – 130		150	ns
23	A0 to A15 valid → $\overline{WAIT}$ input ((1 + N) WAIT mode)	t_{AWL}		3.0x – 100		140	ns
24	$\overline{RD}$ / $\overline{WR}$ fall → $\overline{WAIT}$ hold ((1 + N) WAIT mode)	t_{CW}	2.0x + 0		160		ns
25	A0 to A23 valid → Port input	t_{APH}		2.5x – 195		5	ns
26	A0 to A23 valid → Port hold	t_{APH2}	2.5x + 50		250		ns
27	$\overline{WR}$ rise → Port valid	t_{CP}		200		200	ns
28	A0 to A23 valid → $\overline{RAS}$ fall	t_{ASRH}	1.0x – 60		20		ns
29	A0 to A15 valid → $\overline{RAS}$ fall	t_{ASRL}	0.5x – 40		0		ns
30	$\overline{RAS}$ fall → D0 to D15 input	t_{RAC}		2.5x – 90		110	ns
31	$\overline{RAS}$ fall → A0 to A15 hold	t_{RAH}	0.5x – 25		15		ns
32	$\overline{RAS}$ low pulse width	t_{RAS}	2.0x – 40		120		ns
33	$\overline{RAS}$ high pulse width	t_{RP}	2.0x – 40		120		ns
34	$\overline{CAS}$ fall → $\overline{RAS}$ rise	t_{RSH}	1.0x – 55		25		ns
35	$\overline{RAS}$ rise → $\overline{CAS}$ rise	t_{RSC}	0.5x – 25		15		ns
36	$\overline{RAS}$ fall → $\overline{CAS}$ fall	t_{RCD}	1.0x – 40		40		ns
37	$\overline{CAS}$ fall→ D0 to D15 input	t_{CAC}		1.5x – 120		0	ns
38	$\overline{CAS}$ low pulse width	t_{CAS}	1.5x – 40		80		ns

AC measuring conditions

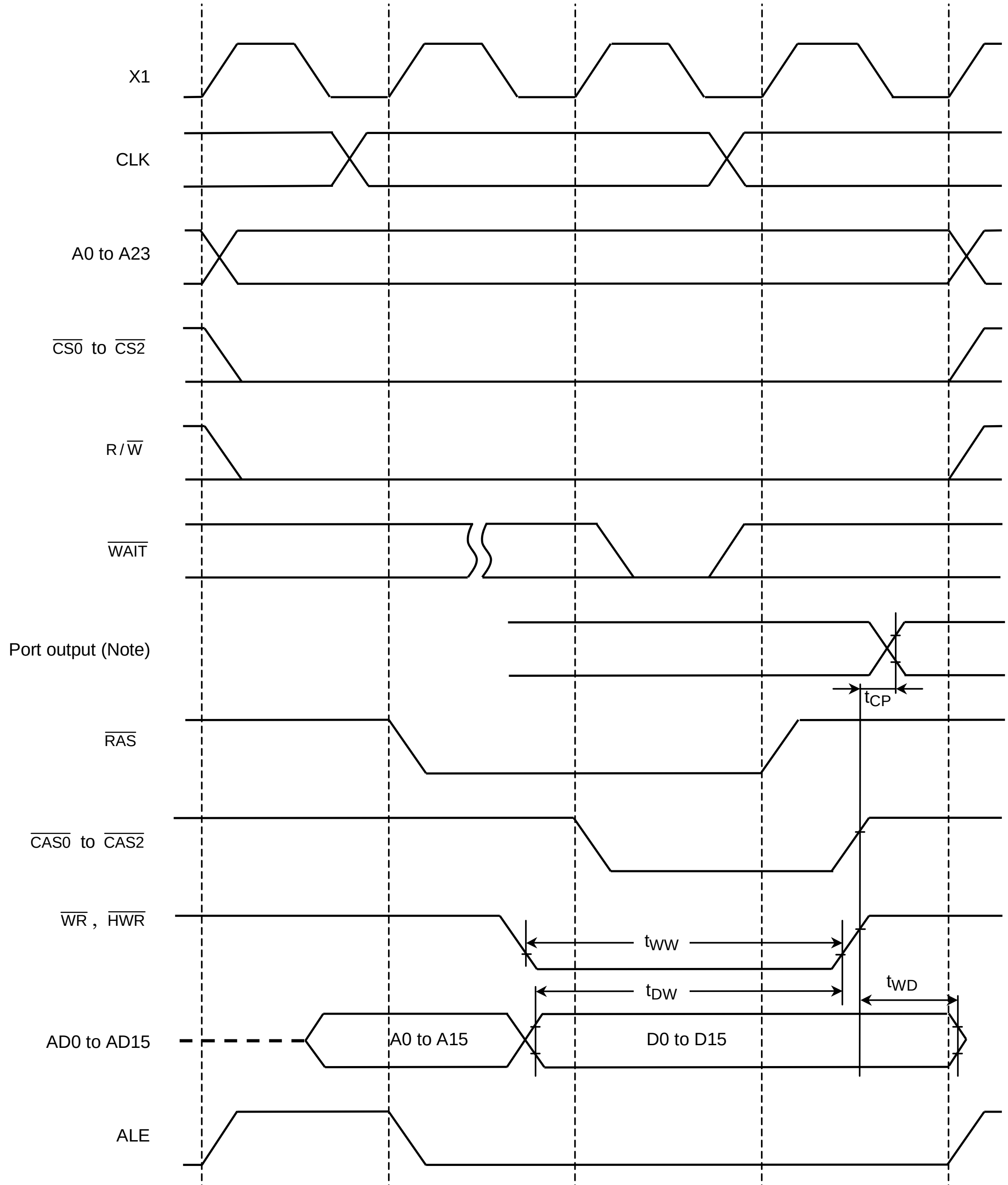
- Output level: High $0.7 \times V_{CC}$/Low $0.3 \times V_{CC}$, CL = 50 pF
- Input level: High $0.9 \times V_{CC}$/Low $0.1 \times V_{CC}$

(1) Read cycle



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as RD and CS are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(2) Write cycle



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics (V_{SS} = 0 V, Ta = –40 to 85°C, $AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$)

Parameter	Symbol	Power Supply	Min	Typ.	Max	Unit
Analog reference voltage (+)	V_{REFH}	V_{CC} = 5 V ± 10%	V_{CC} − 1.5	V_{CC}	V_{CC}	V
		V_{CC} = 3 V ± 10%	V_{CC} − 0.2	V_{CC}	V_{CC}	
Analog reference voltage (−)	V_{REFL}	V_{CC} = 5 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2	
		V_{CC} = 3 V ± 10%	V_{SS}	V_{SS}	V_{SS} + 0.2	
Analog input voltage range	V_{AIN}		V_{REFL}		V_{REFH}	
Analog current for analog reference voltage <VREFON> = 1	I_{REF} (V_{REFL} = 0 V)	V_{CC} = 5 V ± 10%		0.5	1.5	mA
		V_{CC} = 3 V ± 10%		0.3	0.9	
<VREFON> = 0		V_{CC} = 2.7 to 5.5 V		0.02	5.0	μA
Error	–	V_{CC} = 5 V ± 10%		±1.0	±3.0	LSB
		V_{CC} = 3 V ± 10%		±1.0	±3.0	

Note 1: 1LSB = $(V_{REFH} - V_{REFL})/2^{10}$ [V]

Note 2: Minimum operation frequency
The operation of the AD converter is guaranteed only when fc (High-frequency oscillator) is used. (It is not guaranteed when fs is used.) Additionally, it is guaranteed with $f_{FPH} \geq 4$ MHz.

Note 3: The value Icc includes the current which flows through AV_{CC} pin.

Note 4: Error excludes quantizing errors.

4.5 Serial Channel Timing (I/O interface mode)

(1) SCLK input mode

Parameter	Symbol	Variable		32.768 kHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	16X		488 μs		1.28 μs		0.8 μs	
Output data → Rising edge of SCLK	t_{OSS}	t_{SCY}/2 − 5X − 50		91.5 μs		190 ns		100 ns	
SCLK rising edge → Output data hold	t_{OHS}	5X − 100		152 μs		300 ns		150 ns	
SCLK rising edge → Input data hold	t_{HSR}	0		0		0		0	
SCLK rising edge → Effective data input	t_{SRD}		t_{SCY} − 5X − 100		336 μs		780 ns		450 ns

(2) SCLK output mode

Parameter	Symbol	Variable		32.768 kHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle (Programmable)	t_{SCY}	16X	8192X	488 μs	250 ms	1.28 μs	655.36 μs	0.8 μs	409.6 μs
Output data → SCLK rising edge	t_{OSS}	t_{SCY} − 2X − 150		427 μs		970 ns		550 ns	
SCLK rising edge → Output data hold	t_{OHS}	2X − 80		60 μs		80 ns		20 ns	
SCLK rising edge → Input data hold	t_{HSR}	0		0		0		0	
SCLK rising edge → Effective data input	t_{SRD}		t_{SCY} − 2X − 150		428 μs		970 ns		550 ns

(3) SCLK input mode (UART mode)

Parameter	Symbol	Variable		32.768 kHz (Note)		12.5 MHz		20 MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
SCLK cycle	t_{SCY}	4X + 20		122 μs		340 ns		220 ns	
SCLK Low level pulse width	t_{SCYL}	2X + 5		6 μs		165 ns		105 ns	
SCLK High level pulse width	t_{SCYH}	2X + 5		6 μs		165 ns		105 ns	

Note: When fs is used as system clock (f_{SYS}) or fs is used as input clock to prescaler.

4.6 Timer/Counter Input Clock (TI0, TI4, TI5, TI6, TI7)

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
Clock cycle	t_{VCK}	8X + 100		740		500		ns
Low level clock pulse width	t_{VCKL}	4X + 40		360		240		ns
High level clock pulse width	t_{VCKH}	4X + 40		360		240		ns

4.7 Interrupt and Capture

(1) $\overline{\text{NMI}}$, INT0 interrupt

Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{\text{NMI}}$, INT0 low level pulse width	t_{INTAL}	4X		320		200		ns
$\overline{\text{NMI}}$, INT0 high level pulse width	t_{INTAH}	4X		320		200		ns

(2) INT4 to INT7 interrupt, capture

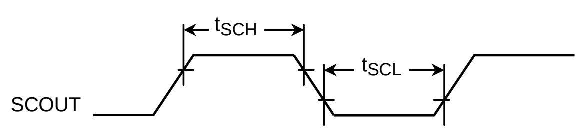
Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
INT4 to INT7 low level pulse width	t_{INTBL}	4X + 100		420		300		ns
INT4 to INT7 high level pulse width	t_{INTBH}	4X + 100		420		300		ns

4.8 SCOUT Pin AC Characteristics

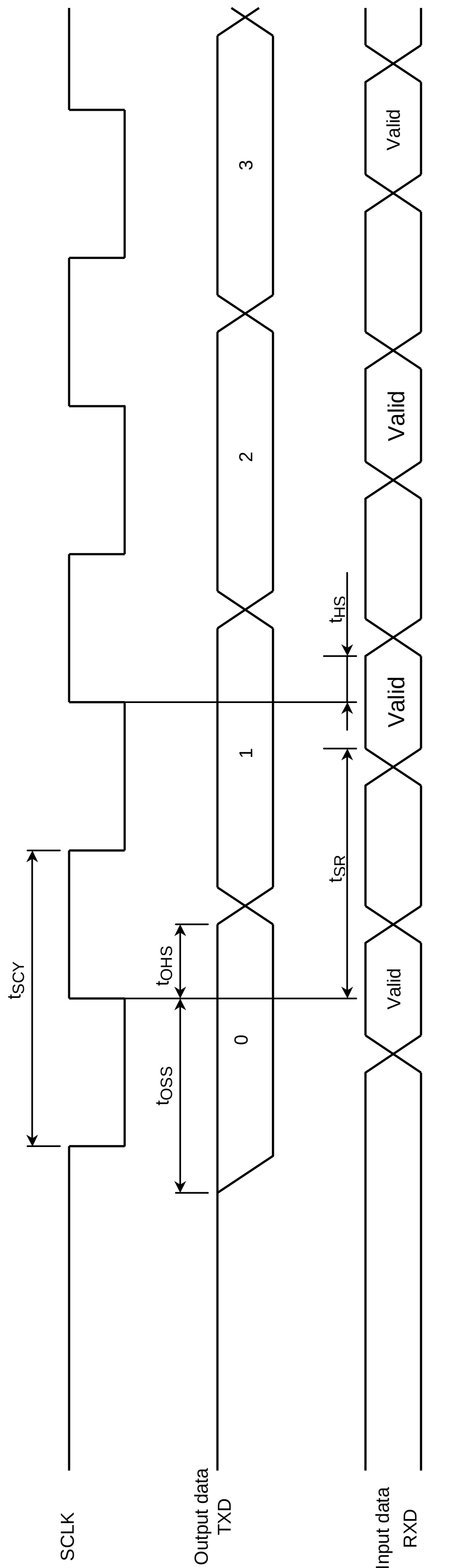
Parameter		Symbol	Variable		12.5 MHz		20 MHz		Unit
			Min	Max	Min	Max	Min	Max	
High to level pulse width	V_{CC} = 5 V ± 10%	t_{SCH}	0.5X – 10		30		15		ns
High to level pulse width	V_{CC} = 3 V ± 10%		0.5X – 20		20		–	–	
Low to level pulse width	V_{CC} = 5 V ± 10%	t_{SCL}	0.5X – 10		30		15		ns
Low to level pulse width	V_{CC} = 3 V ± 10%		0.5X – 20		20		–	–	

Measurement condition

- Output level: High 2.2 V/Low 0.8 V, CL = 10 pF

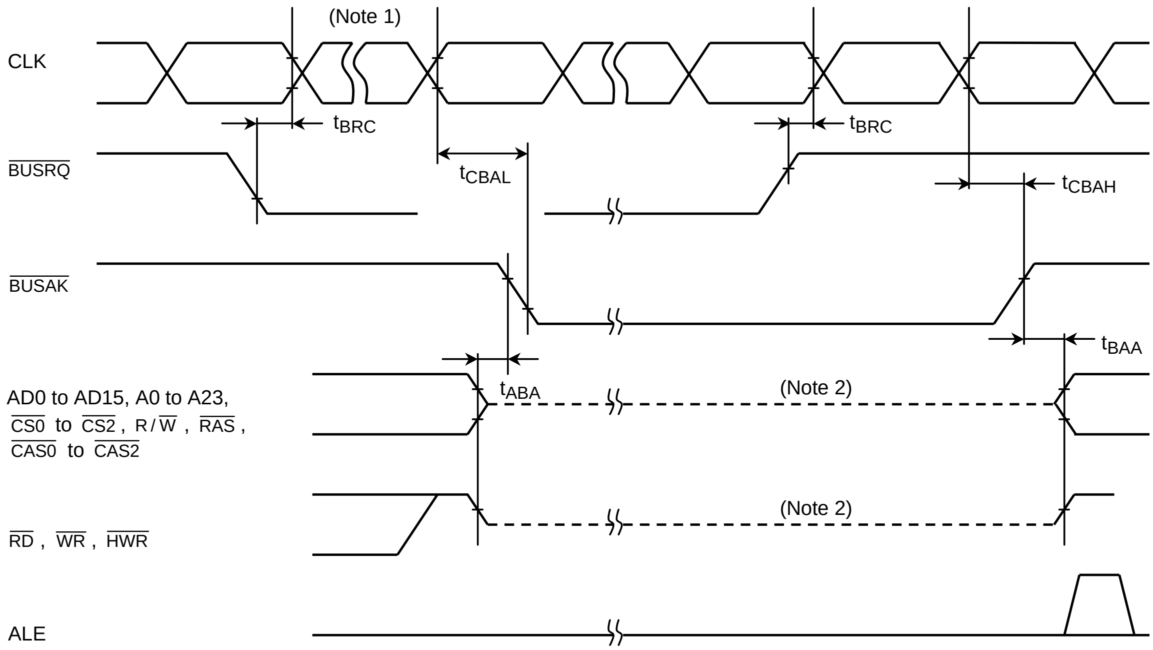


4.9 Timing Chart for I/O Interface Mode



Note: SCLK is reversed in SCLK input falling mode.

4.10 Timing Chart for Bus Request (BUSRQ)/Bus Acknowledge (BUSAK)



Parameter	Symbol	Variable		12.5 MHz		20 MHz		Unit
		Min	Max	Min	Max	Min	Max	
BUSRQ set to up time to CLK	t_{BRC}	120		120		120		ns
CLK → BUSAK falling edge	t_{CBAL}		1.5x + 120		240		195	ns
CLK → BUSAK rising edge	t_{CBAH}		0.5x + 40		80		65	ns
Output buffer is off to BUSAK ↘	t_{ABA}	0	80	0	80	0	80	ns
BUSAK ↗ to output buffer is on.	t_{BAA}	0	80	0	80	0	80	ns

Note 1: The bus will be released after the WAIT request is inactive, when the BUSRQ is set to "0" during "Wait" cycle.

Note 2: This line only shows the output buffer is off to state.
It doesn't indicate the signal level is fixed.
Just after the bus is released, the signal level which is set before the bus is released is kept dynamically by the external capacitance. Therefore, to fix the signal level by an external resistor during bus releasing, designing is executed carefully because the level to fix will be delayed.
The internal programmable pull-up/pull-down resistor is switched active/non-active by an internal signal.

4.11 Read Operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5°C V_{CC} = 5 V ± 10%

Parameter	Symbol	Condition	Min	Max	Unit
V_{PP} read voltage	V_{PP}	–	4.5	5.5	V
Input high voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH1}	–	2.2	V_{CC} + 0.3	
Input low voltage (A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL1}	–	–0.3	0.8	
Address to output delay	t_{ACC}	C_L = 50 pF	–	2.25 T_{CYC} + α	ns

T_{CYC} = 400 ns (10 MHz Clock)
α = 200 ns

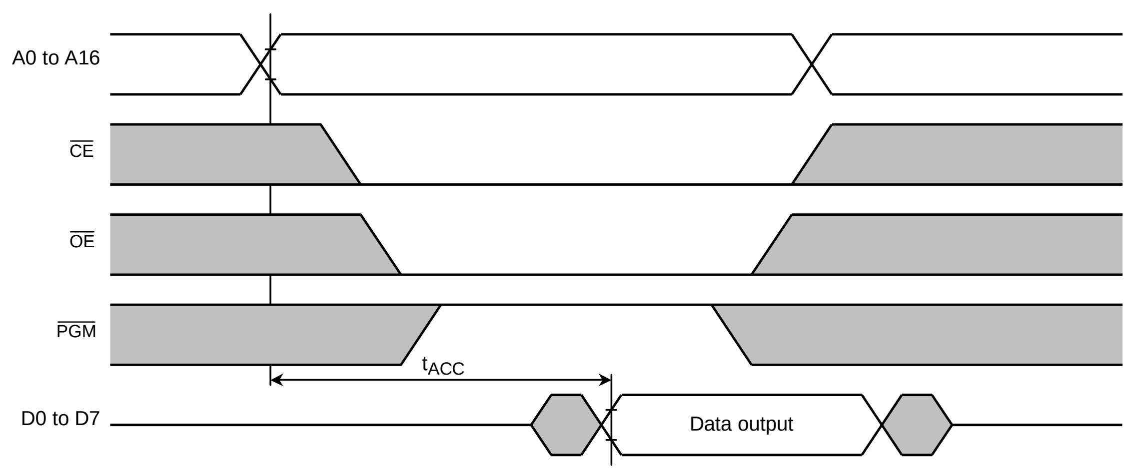
4.12 Program Operation in PROM Mode

DC/AC characteristics

Ta = 25 ± 5°C V_{CC} = 6.25 V ± 0.25 V

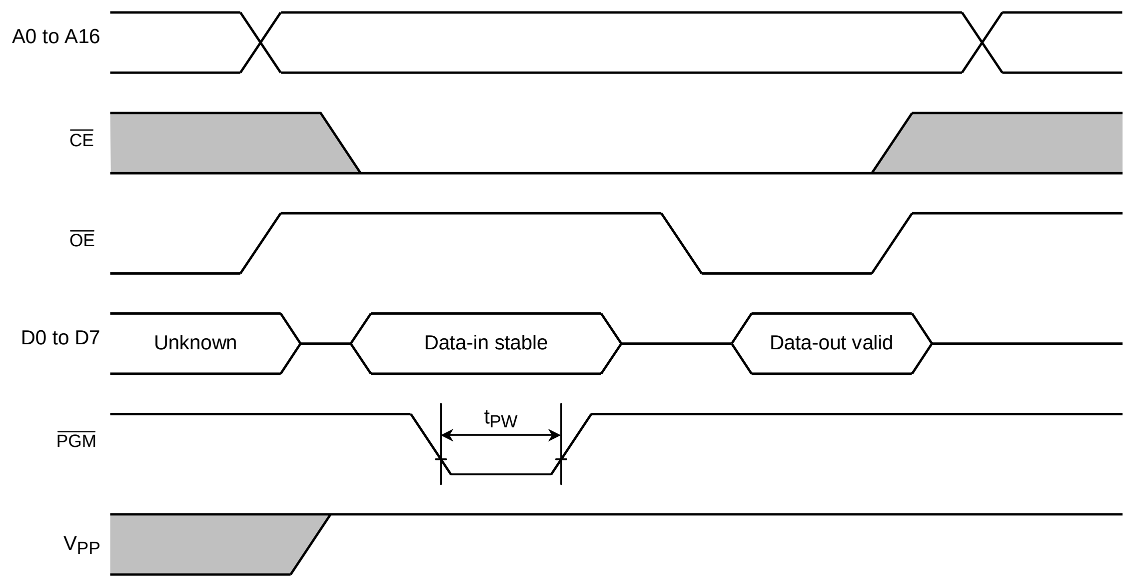
Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Programming supply voltage	V_{PP}	–	12.50	12.75	13.00	V
Input high voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IH}	–	2.6		V_{CC} + 0.3	
Input low voltage (D0 to D7, A0 to A16, $\overline{CE}$, $\overline{OE}$, $\overline{PGM}$)	V_{IL}	–	–0.3		0.8	
V_{CC} supply current	I_{CC}	fc = 10 MHz	–		50	mA
V_{PP} supply current	I_{PP}	V_{PP} = 13.00 V	–		50	
$\overline{PGM}$ program pulse width	t_{PW}	C_L = 50 pF	0.095	0.1	0.105	ms

4.13 Timing Chart of Read Operation in PROM Mode



4.14 Timing Chart of Program Operation in PROM Mode

High-speed programming formula



Note 1: The power supply of V_{PP} (12.75 V) must be turned on at the same time or the later time for a power supply of V_{CC} and must be clear power-on at the same time or early time for a power supply of V_{CC}.

Note 2: The pull-up/pull-down device on condition of V_{PP} = 12.75 V suffers a damage for the device.

Note 3: The maximum spec of V_{PP} pin is 14.0 V. Be careful a overshoot at the programming.

5. Package Dimensions

P-LQFP100-1414-0.50F

Unit: mm