TOSHIBA BiCD Process Integrated Circuit Silicon Monolithic

TB62217AFG

PWM drive Stepping Motor Driver / Brush DC Motor Driver Selectable, DC-DC Converter and Reset function IC

The TB62217FG is a dual stepping motor driver driven by PWM chopper micro step, with 3- channel step-down DC-DC converters and an external-IC reset function.

To drive a two-phase bipolar-type stepping motor, a 16-bit latch and a 16-bit shift register are built into the IC. The IC is suitable for driving stepping motors with low-torque ripple in a highly efficient manner. In addition, a signal axis can be switched to serve as a PWM driver for two DC motors.

By equipping the stepping motor driver with Selectable Mixed Decay Mode for switching the attenuation ratio during chopping, and also equipping it with a DC-DC converter, it is possible for the IC to supply external voltage.

With a built-in timer that starts running when the IC is supplied with power, the IC can be used in resetting (initializing) external devices.

Weight: 0.45 g (typ.)

Features

- The following motor combinations can be used.

	Stepper	DC Large DC (L)	DC Small DC (S)
(1)	Dual motors	—	—
(2)	Single motor	Single motor	—
(3)	Single motor	—	Dual motors
(4)	—	Single motor	Dual motors
(5)	—	Dual motors	—
(6)	—	—	Quadruple motors

Note Hereafter, DC Large will be referred to as DC (L) and DC Small will be referred to as DC (S).

Stepping Motor	**1.0A(MAX)**	**(Single Motor)**
DC Motor Mode	**DC Large**	**DC Small**
Pulse spike Peak	**8.0A(500ns)**	**8.0A (500ns)**
Recommended maximum current	**3.0A(100ms)**	**2.5A (100ms)**
Stationary current	**0.8A**	**0.8A**

The large current standard is achieved by shorting a small current H-Bridge across two ICs. In addition, if the thermal setting is designed to be within the prescribed thermal range, the initial torque current can be used as the normal operating current.

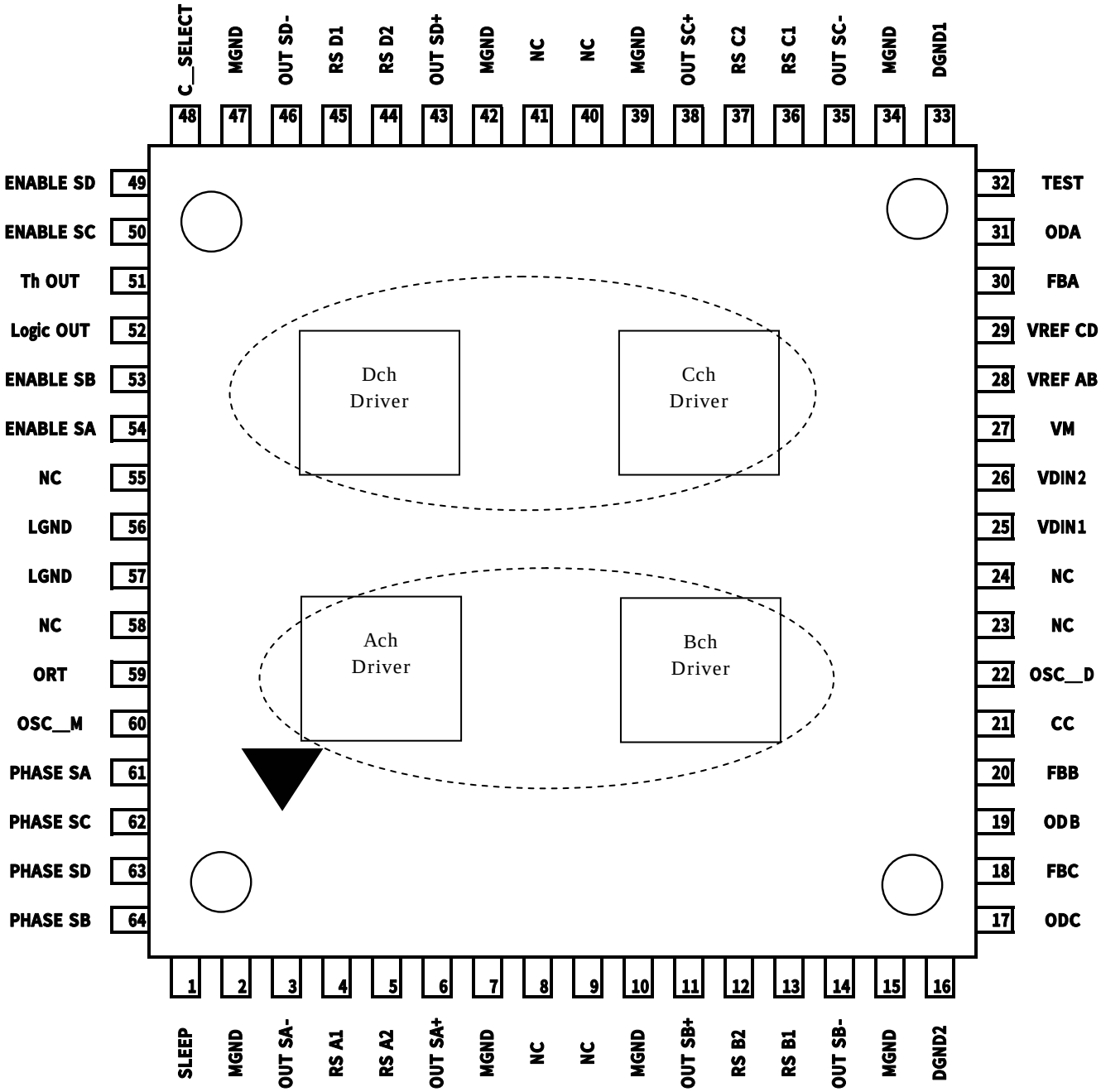
- It is possible to supply external voltage by incorporating three step-down 1.5 V to 5.0 V variable DC-DC converters.
- A Reset function has been added making it possible to deliver an external reset signal.
- The DMOS motor driver output of this monolithic BiCD IC is capable of achieving a low ON resistance of Ron = 0.6 Ω (@T_j = 25°C, 0.6A: typ.)
- With two sets of internal 16-bit shift register and latch, the IC can drive stepping motors using a 4-bit micro step.
- Equipped protection circuits: DC-DC converter over current/increased voltage protection, motor over current protection and total IC over temperature protection.
  In addition, equipped with Power On Reset circuit for initializing the IC when the power is turned on and off.
- Package: 64-pin Pb-free QFP package with a heat sink (THQFP64-P-1010-0.50)
- Motor maximum output pressure: 50 V
- On-chip Mixed Decay Mode enables specification of four-stage attenuation ratio.
- Chopping frequency can be set by external oscillator. High-speed chopping is possible at 100 kHz or higher.

Note: When using the IC, exercise great care in regard to thermal conditions.

This device is easy damaged by high static voltage (ESD).
For this reason, please handle with care.

Please Insert an SBD (Schottky Barrier Diode : Recommended "TSB CRS04") between "ODB" pin and "D-GND" pin ,
if using C channel.

* **Pin Layout** (4-channel DC Motor Mode , example)



T-HQFP64-1010-P-0.50

Combinations enclosed in the blue dashed lines are used when in DC (L) mode (A- and B-axis drivers in a pair, and C- and D-axis drivers in a pair).

Cautions on connection to the IC pins

Note1 Connect all NC pins (pins left unused) to the lowest potential level (usually to GND).

Note2 Connect any unused Vref pins (28pin,29pin) to GND.

Note3 Unused DATA, CLOCK, and STROBE input pins are pulled down internally, so connect them to GND. Please ensure that noise is not introduced into the external circuit

Note4 Connect any unused RS pins to VM.

Note5 Connect the feedback pins (FBA, FBB, and FBC) to GND if the corresponding DC-DC converter is not used.

Note6 Always connect the TEST pin to the lowest potential level (usually to GND).

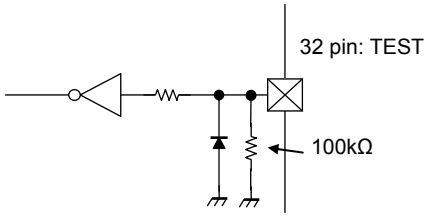
Note7: TEST pin

The TB62217FG has a test mode function for inspection at the factory. The test mode reduces the “initial and normal protection mask time” and “ORT output time” to 1/1024 of the respective ratings so as to make the inspection easier.

To maintain normal operation, therefore, be sure to connect pin 32 to a ground so that it will not be used.

Conditions to use the test mode

Input level	32
High	standard operation
Low	TEST Mode



Note 8 If the IC is inserted in an incorrect orientation, it will be damaged because a high voltage is applied to low-voltage blocks. To avoid such damage, always confirm the position of pin 1 and the position and dimensions of each lead when installing the IC.

Note 9 The IC has no on-chip over voltage protection circuit. Avoid applying a voltage higher than any rated voltage (such as maximum ratings) to the IC.

Note 10 Solder the heat sink provided on the bottom surface of the IC to a ground-level pattern arranged for heat release so as to ensure stable operation and efficient heat release.

Note11 Once set up, since the IC is not affected by a logical input from a “Don’t care” pin even if a voltage is applied to the pin, as long as the applied voltage is not higher than its rating, no problem (such as a malfunction) will occur.

Pin Descriptions (initial setup mode)

SLEEP = Low supports a write mode for the initial setup or extended setup mode data.

(1) Pin description (SETUP mode, that is, initial setup or extended setup mode)
(2) Pin description (dual axis stepping motor mode)
(3) Pin description (single axis stepping motor and single axis DC (L) mode)
(4) Pin description (single axis stepping motor and dual axis DC (S) mode)
(5) Pin description (dual axis DC (S) and single axis DC (L) mode)
(6) Pin description (dual axis DC (L) mode)
(7) Pin description (quadruple axis DC (S) mode)

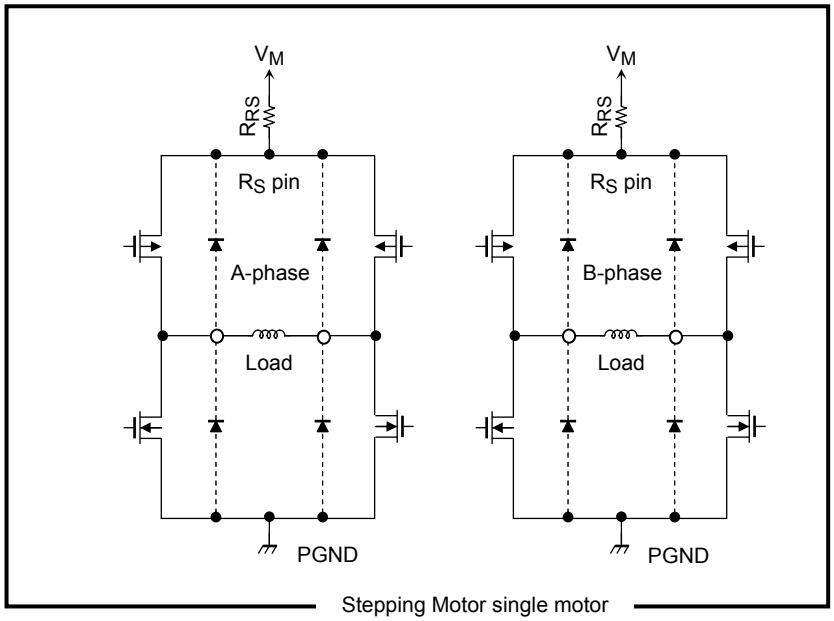
Pin Name Assignment Table

	(1)	(2)	(3)	(4)	(5)	(6)	(7)	
	SETUP MODE	STEP (Dual)	STEP + DC (L)	STEP+ Dual DC (S)	DC (L)+ Dual (DC (S)	Dual DC (L)	4ch DC (S)	Remark
1	SLEEP (L)	SLEEP (H)	SLEEP (H)	SLEEP (H	SLEEP (H	SLEEP (H	SLEEP (H	
2	MGND	MGND	MGND	MGND	MGND	MGND	MGND	
3	(OUT A-	OUT A-	OUT A-	OUT A-	OUT LAB-	OUT LAB-	OUT SA-	
4	(RS A1)	RS A1	RS A1	RS A1	RS A1	RS A1	RS A1	
5	(RS A2)	RS A2	RS A2	RS A2	RS A2	RS A2	RS A2	
6	(OUT A(+)	OUT A+	OUT A+	OUT A+	OUT LAB+	OUT LAB+	OUT SA+	
7	MGND	MGND	MGND	MGND	MGND	MGND	MGND	
8	NC	NC	NC	NC	NC	NC	NC	
9	NC	NC	NC	NC	NC	NC	NC	
10	MGND	MGND	MGND	MGND	MGND	MGND	MGND	
11	(OUT B+)	OUT B+	OUT B+	OUT B+	OUT LAB+	OUT LAB+	OUT SB+	
12	(RS B2)	RS B2	RS B2	RS B2	RS B2	RS B2	RS B2	
13	(RS B1)	RS B1	RS B1	RS B1	RS B1	RS B1	RS B1	
14	(OUT B–)	OUT B–	OUT B–	OUT B–	OUT LAB–	OUT LAB–	OUT SB–	
15	MGND	MGND	MGND	MGND	MGND	MGND	MGND	
16	DGND2	DGND2	DGND2	DGND2	DGND2	DGND2	DGND2	
17	(ODC)	ODC	ODC	ODC	ODC	ODC	ODC	
18	(FBC)	FBC	FBC	FBC	FBC	FBC	FBC	
19	(ODB)	ODB	ODB	ODB	ODB	ODB	ODB	
20	(FBB)	FBB	FBB	FBB	FBB	FBB	FBB	
21	CC	CC	CC	CC	CC	CC	CC	
22	OSC_D	OSC_D	OSC_D	OSC_D	OSC_D	OSC_D	OSC_D	
23	NC	NC	NC	NC	NC	NC	NC	
30	NC	NC	NC	NC	NC	NC	NC	
25	VDIN1	VDIN1	VDIN1	VDIN1	VDIN1	VDIN1	VDIN1	
26	VDIN2	VDIN2	VDIN2	VDIN2	VDIN2	VDIN2	VDIN2	
27	VM	VM	VM	VM	VM	VM	VM	
28	(VREF AB)	VREF AB	VREF AB	VREF AB	VREF LAB	VREF LAB	VREF SAB	
29	(VREF CD)	VREF CD	VREF LCD	VREF SCD	VREF SCD	VREF LCD	VREF SCD	
30	(FBA)	FBA	FBA	FBA	FBA	FBA	FBA	
31	(ODA)	ODA	ODA	ODA	ODA	ODA	ODA	

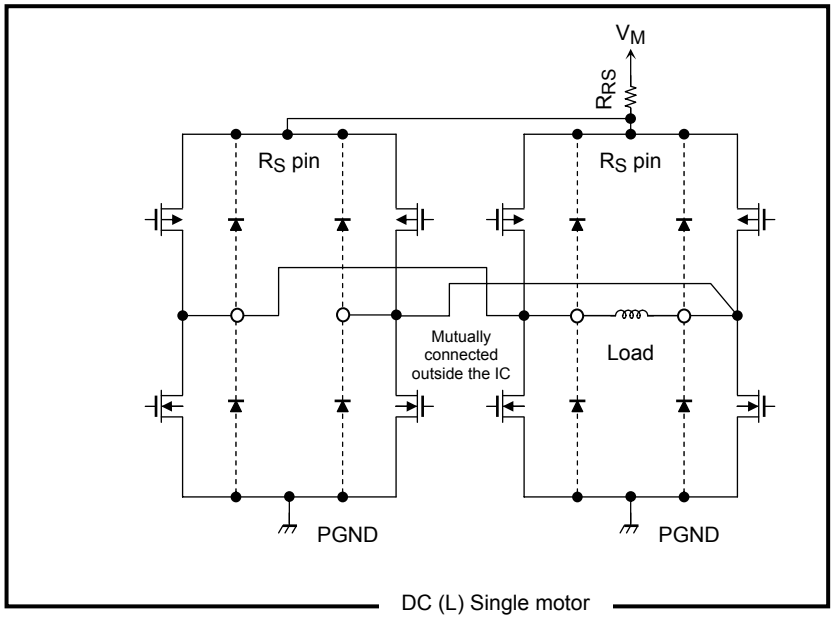
	(1)	(2)	(3)	(4)	(5)	(6)	(7)	
	SETUP MODE	**STEP (Dual)**	**STEP + DC (L)**	**STEP+ Dual DC (S)**	**DC (L)+ Dual (DC (S)**	**Dual DC (L)**	**4ch DC (S)**	**Remark**
32	**TEST**	**TEST**	**TEST**	**TEST**	**TEST**	**TEST**	**TEST**	Connect to GND
33	DGND1	DGND1	DGND1	DGND1	DGND1	DGND1	DGND1	
34	MGND	MGND	MGND	MGND	MGND	MGND	MGND	
35	(OUT C–)	OUT C–	OUT LCD–	OUT SC–	OUT SC–	OUT LCD–	OUT SC–	
36	(RS C1)	RS C1	RS C1	RS C1	RS C1	RS C1	RS C1	
37	(RS C2)	RS C2	RS C2	RS C2	RS C2	RS C2	RS C2	
38	(OUT C+)	OUT C+	DOUT LC(	OUT SC(	OUT SC(	OUT LCD(	OUT SC(	
39	MGND	MGND	MGND	MGND	MGND	MGND	MGND	
40	NC	NC	NC	NC	NC	NC	NC	
41	NC	NC	NC	NC	NC	NC	NC	
42	MGND	MGND	MGND	MGND	MGND	MGND	MGND	
43	(OUT D()	OUT D(	OUT LCD(	OUT SD(	OUT SD+	OUT LCD+	OUT SD+	
44	(RSD1)	RSD1	RSD1	RSD1	RSD1	RSD1	RSD1	
45	(RSD2)	RSD2	RSD2	RSD2	RSD2	RSD2	RSD2	
46	OUT D-	OUT D-	OUT LCD-	OUT SD-	OUT SD-	OUT LCD-	OUT SD-	
47	MGND	MGND	MGND	MGND	MGND	MGND	MGND	
48	C_SELECT	C_SELECT	C_SELECT	C_SELECT	C_SELECT	C_SELECT	C_SELECT	
49	-	-	-	ENABLE SD	ENABLE SD	-	ENABLE SD	
50	-	STROBE CD	ENABLE LCD	ENABLE SC	ENABLE SC	ENABLE LCD	ENABLE SC	
51	TH_OUT	TH_OUT	TH_OUT	TH_OUT	TH_OUT	TH_OUT	TH_OUT	
52	LOGIC OUT	LOGIC OUT	LOGIC OUT	LOGIC OUT	LOGIC OUT	LOGIC OUT	LOGIC OUT	
53	-	-	-	-	-	-	ENABLE SB	
54	STROBE AB	STROBE AB	STROBE AB	STROBE AB	ENABLE LAB	ENABLE LAB	ENABLE SA	
55	NC	NC	NC	NC	NC	NC	NC	
56	LGND	LGND	LGND	LGND	LGND	LGND	LGND	AGND (LGND)
57	LGND	LGND	LGND	LGND	LGND	LGND	LGND	AGND (LGND)
58	NC	NC	NC	NC	NC	NC	NC	
59	ORT	ORT	ORT	ORT	ORT	ORT	ORT	
60	OSC_M	OSC_M	OSC_M	OSC_M	OSC_M	OSC_M	OSC_M	
61	-	DATA CD	-	PHASE SD	PHASE SD	-	PHASE SA	
62	**-**	**CLK CD**	**PHASE LCD**	**PHASE SC**	**PHASE SC**	**PHASE LCD**	**PHASE SC**	
63	**DATA AB**	**DATA AB**	**DATA AB**	**DATA AB**	**-**	**-**	**PHASE SD**	
64	**CLK AB**	**CLK AB**	**CLK AB**	**CLK AB**	**PHASE LAB**	**PHASE LAB**	**PHASE SB**	

-: Don't care

(Note:H-bridge combination (connection method) for each type of motor driver



Stepping Motor single motor

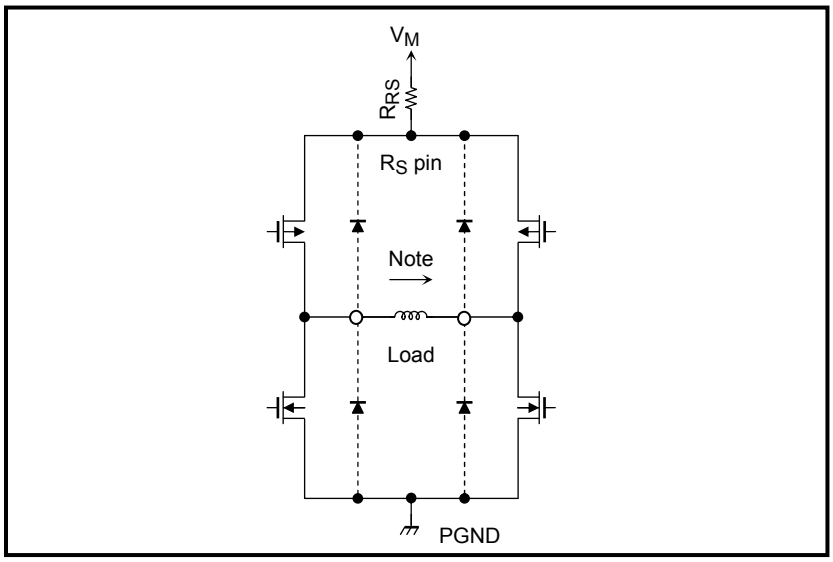


DC (L) Single motor

○ ⋯ The white circle indicates an IC pin.

Note1: When driving a DC motor in DC (L) mode, avoid an impedance difference outside the IC.

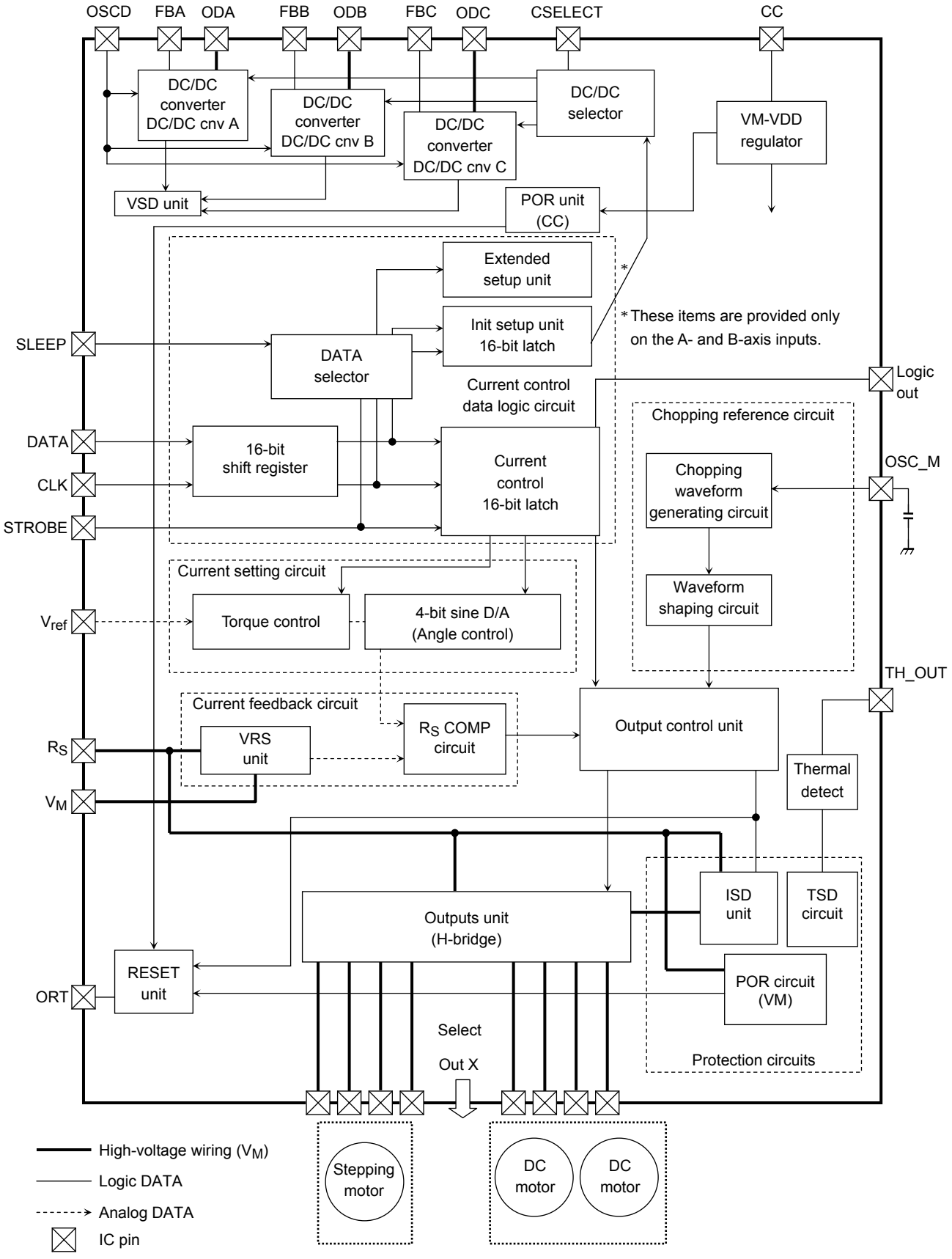
Note2: If the impedance of wiring to mutually connected output transistors is unbalanced, the current that flows through the transistor also becomes unbalanced and may exceed the maximum rating of the transistor, thus damaging the transistor.



DC (S) Single motor

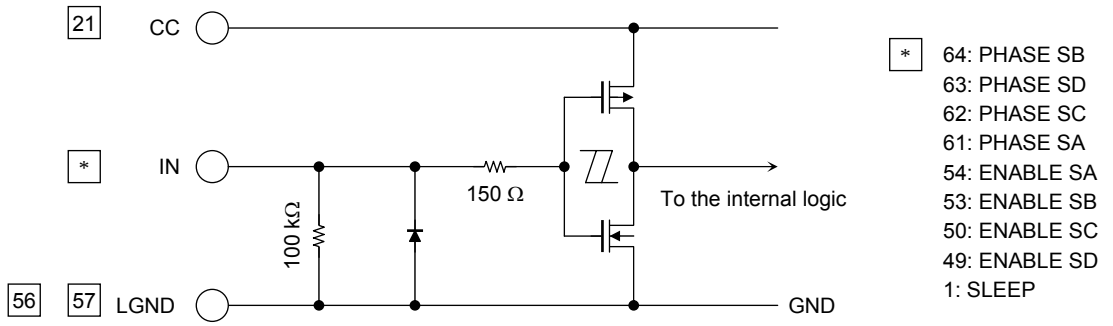
○ ··· The white circle indicates an IC pin.

1. Overall Block Diagram

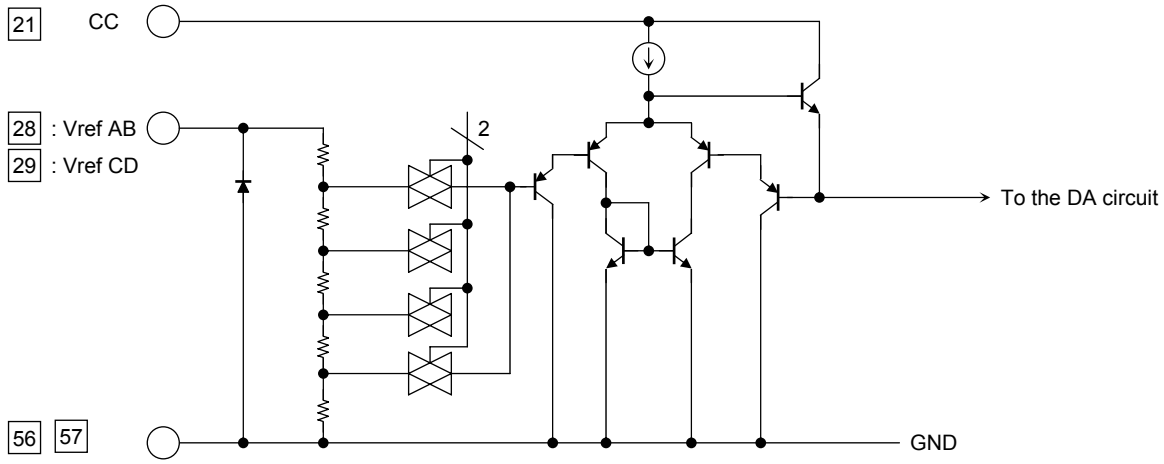


2-1. Input Equivalent Circuits

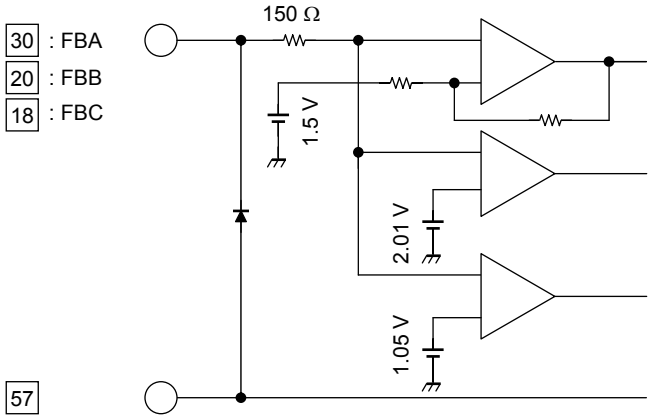
(1) Logic Input Pin



(2) Vref Input Pin



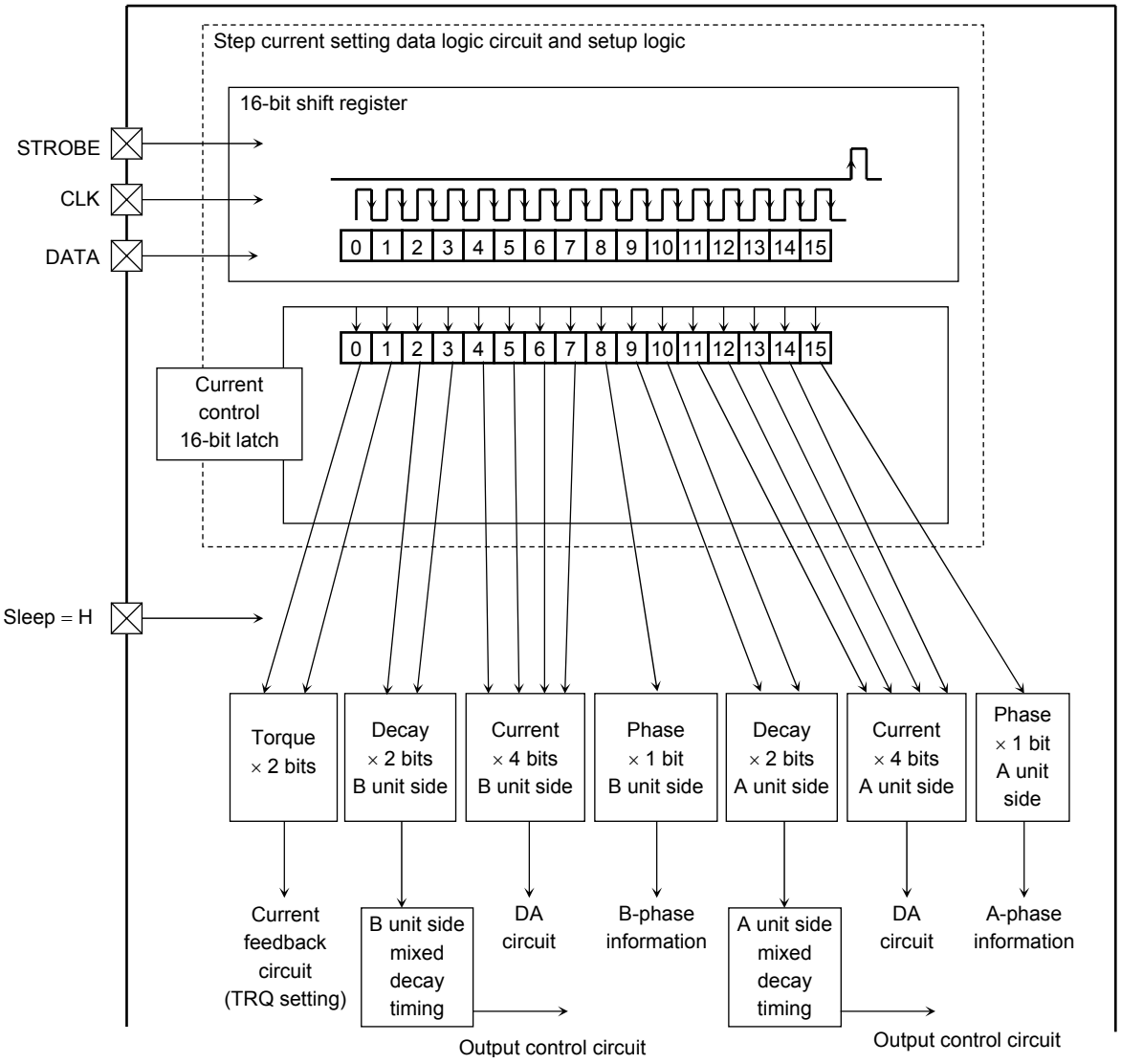
(3) DC/DC Feed Back Pin (FBx)



2-2. Stepping Motor Logic Unit (with the same functions for both an A-/B-axis pair and a C-/D-axis pair)

Function

This circuit receives step current setting data entered from the DATA pin and transfers it to the subsequent stage. It is enabled when the SLEEP pin is high. (If the SLEEP pin is low, the IC enters the initial setup or extended setup mode.)



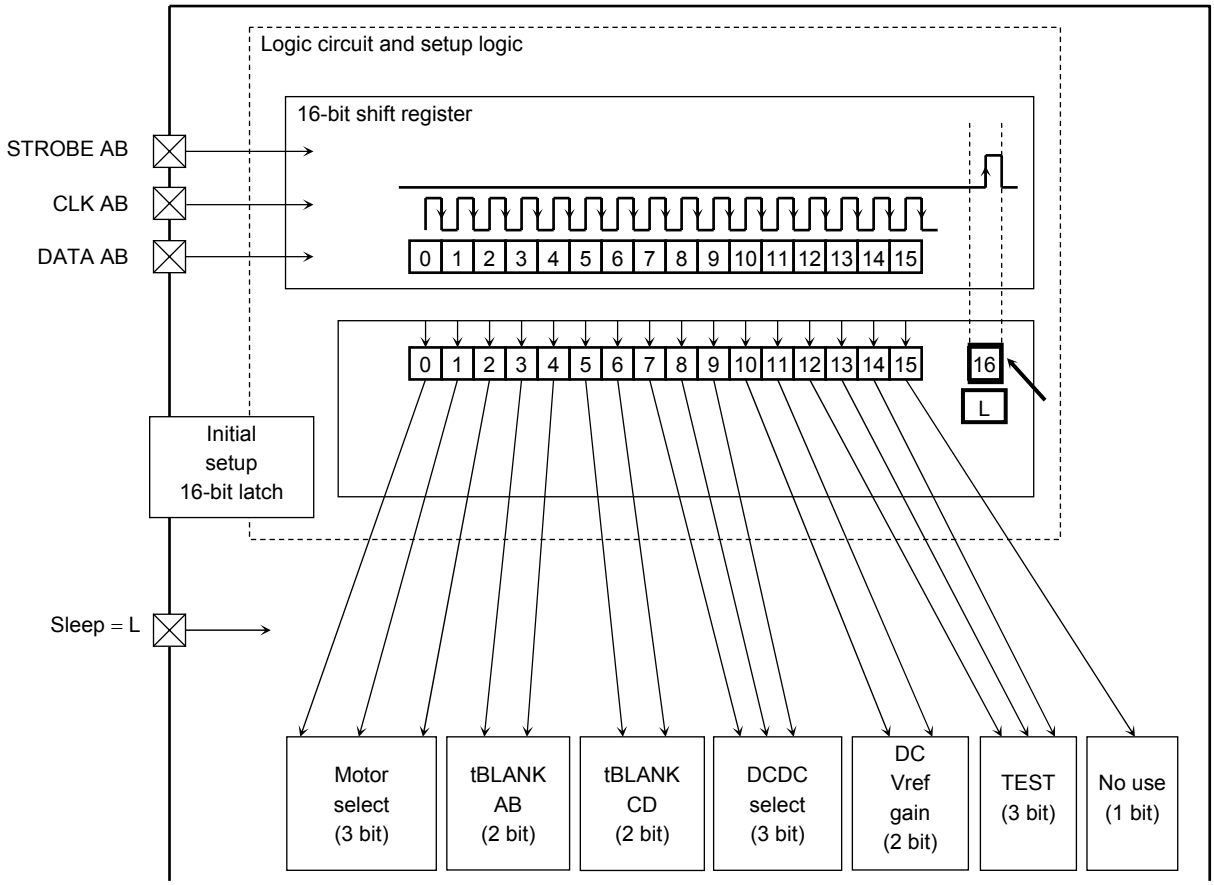
Once ORT is released, driving the SLEEP pin high puts the IC in a write mode for stepping motor current control data. Driving the SLEEP pin from high to low and back to high clears any latched motor control data (to all low).

2-3. Initial Setup Logic Unit (available only for the A- / B-axis pair)

Function

This circuit is used to set up driver functions (initial setup) according to signals entered from the DATA pin. The functions that can be set up include motor re-configuration, digital tBLANK, DC-DC converter ON/OFF setting, and DC motor mode Vref (gain) setting.

Note: Do not use the TEST mode. Keep all the corresponding bits and any unused pins at a low level.

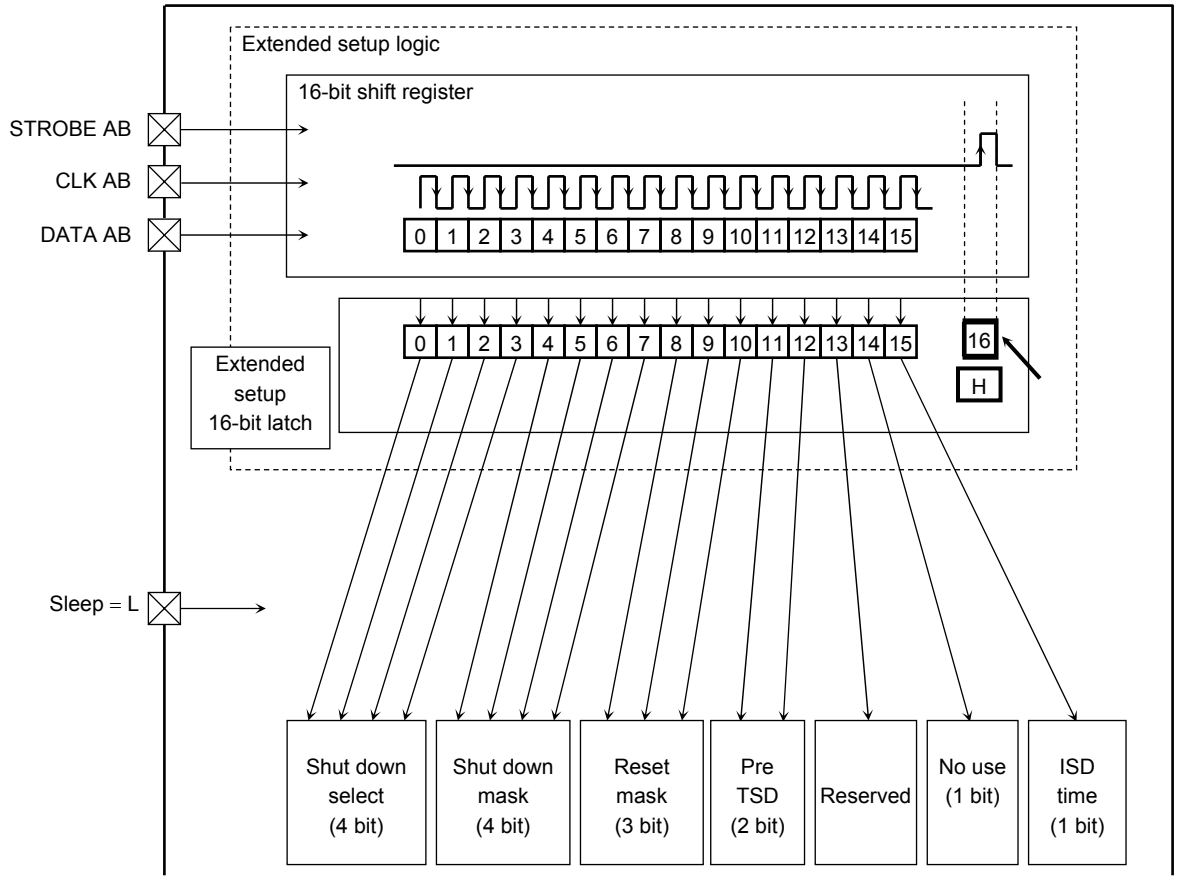


Note: The setting entered in initial setup mode is in effect if the DATA signal is low when the STROBE signal is supplied. The initial setup mode data is cleared at POR (power-on reset).

2-4. Extended Setup Logic Unit (available only for the A- and B-axis pair)

Function

This circuit sets up the monitor functions of the driver IC internal circuits according to a signal entered from the DATA pin.

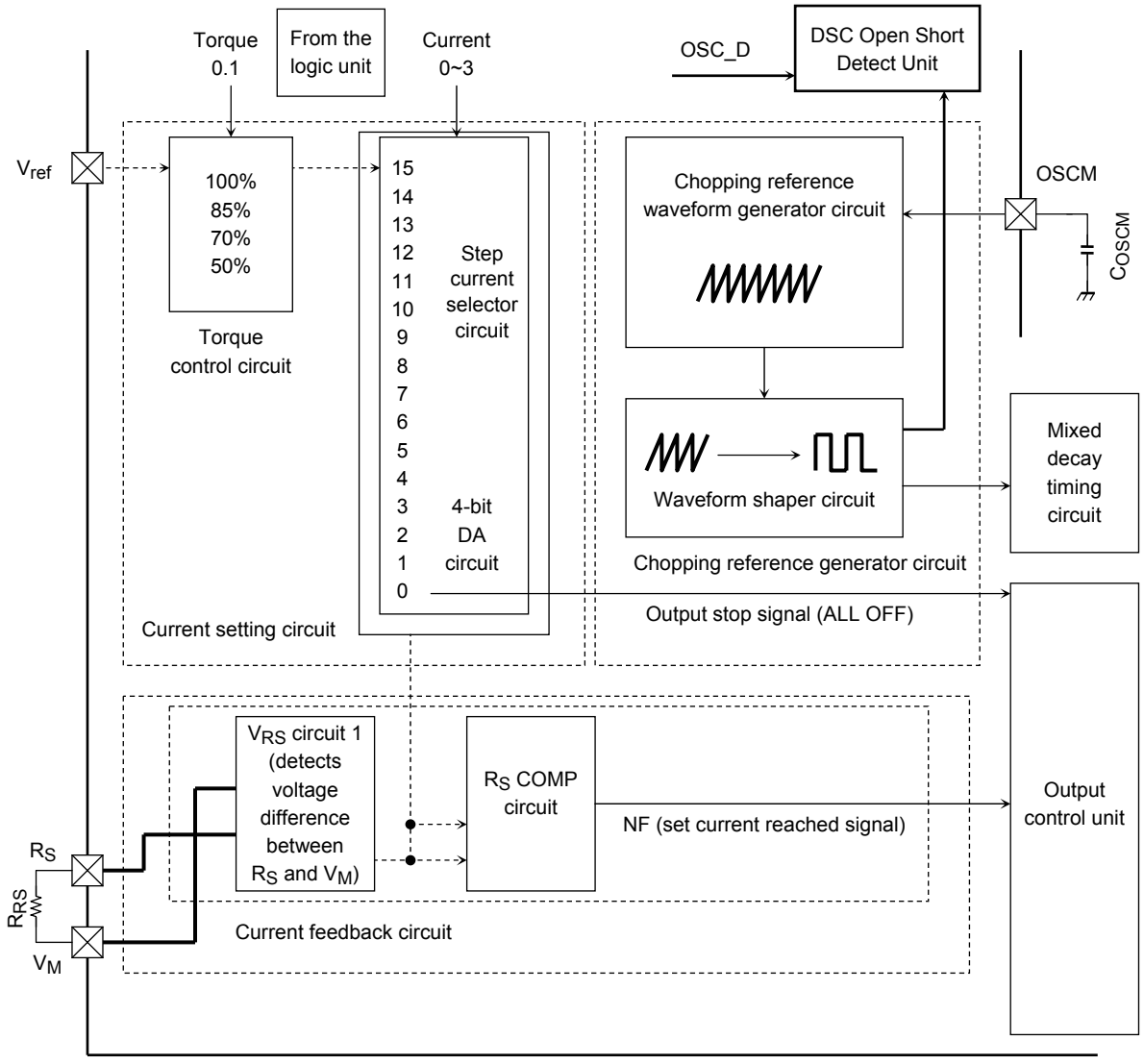


Note: The internal-signal monitoring setting (entered in extended setup mode) is in effect if the DATA signal is high when the STROBE signal is supplied. Data for the extended setup mode is cleared at POR (power-on reset).

3. Current Feedback Circuit and Current Setting Circuit for Motor Driver

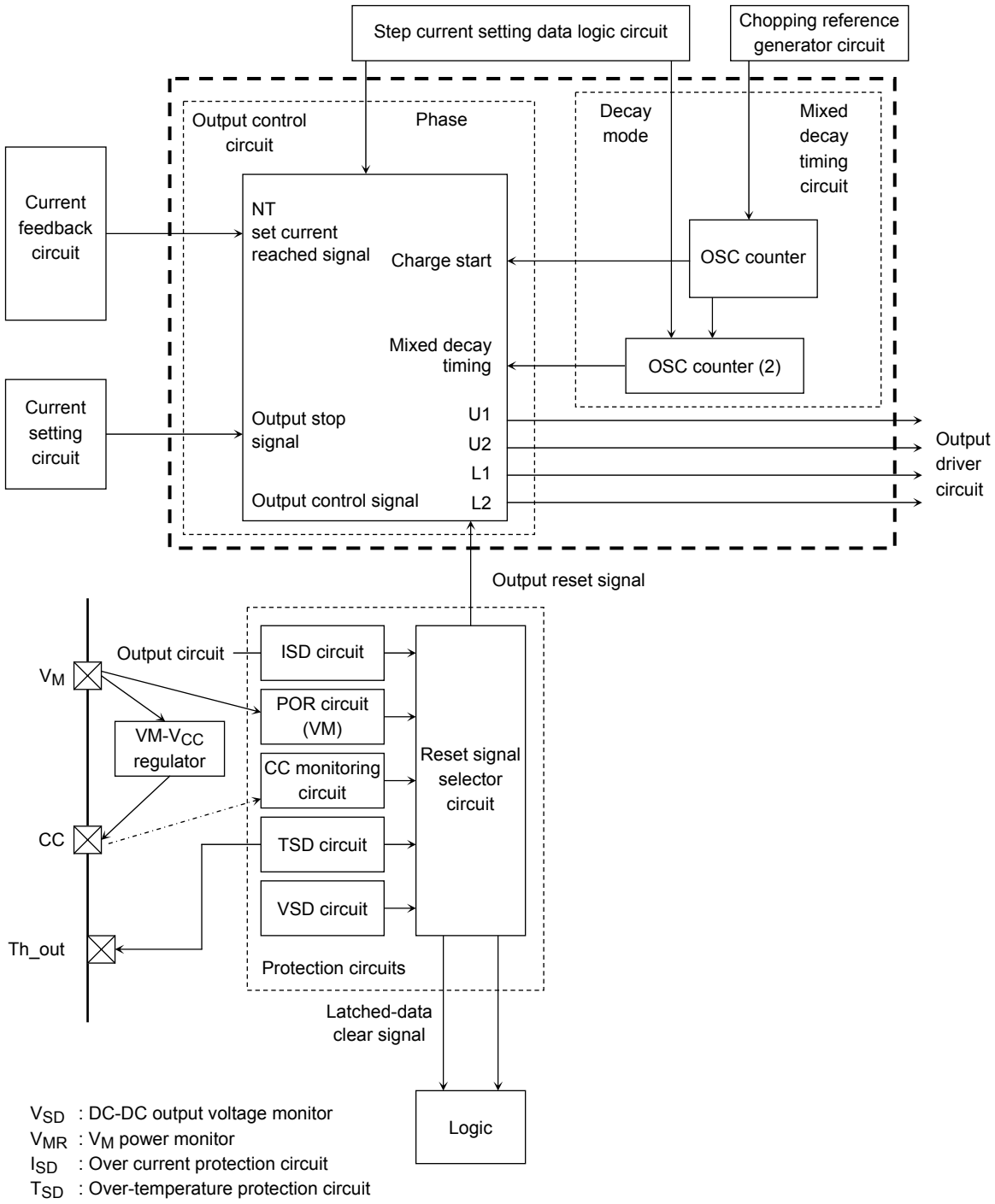
Function

The current setting circuit is used to set the reference voltage of the output current using the step current setting data entered from the serial input pin.
The current feedback circuit is used to deliver a signal to the output control circuit when the output current reaches the set current. This is done by comparing the reference voltage delivered from the current setting circuit with the potential difference generated when current flows through the current sense resistor (RRS) connected between RS and VM.
The chopping waveform generator, to which a capacitor is connected, generates the OSC M (OSC-CLK) as a chopping frequency reference.
If the Osc_M pin becomes open, the open condition detection function works, thus shutting down the IC. If the pin is shorted to GND when the IC starts operating, the detection function also works and the IC does not operate.

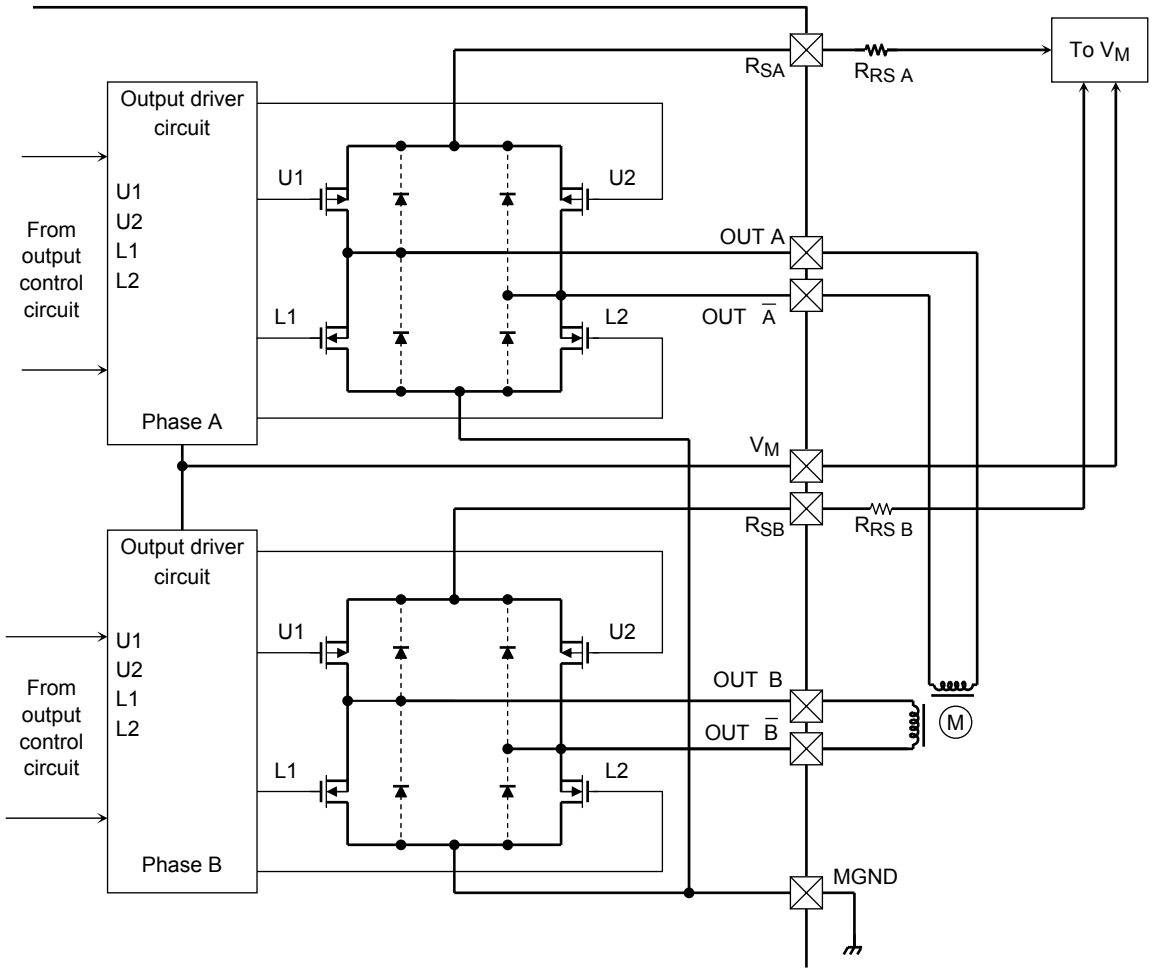


Note: The RE COMP circuit compares the set current with the output current and generates a signal when the output current reaches the set current.

4. Output Control Circuit, Current Feedback Circuit, and Current Setting Circuit for Motor Driver



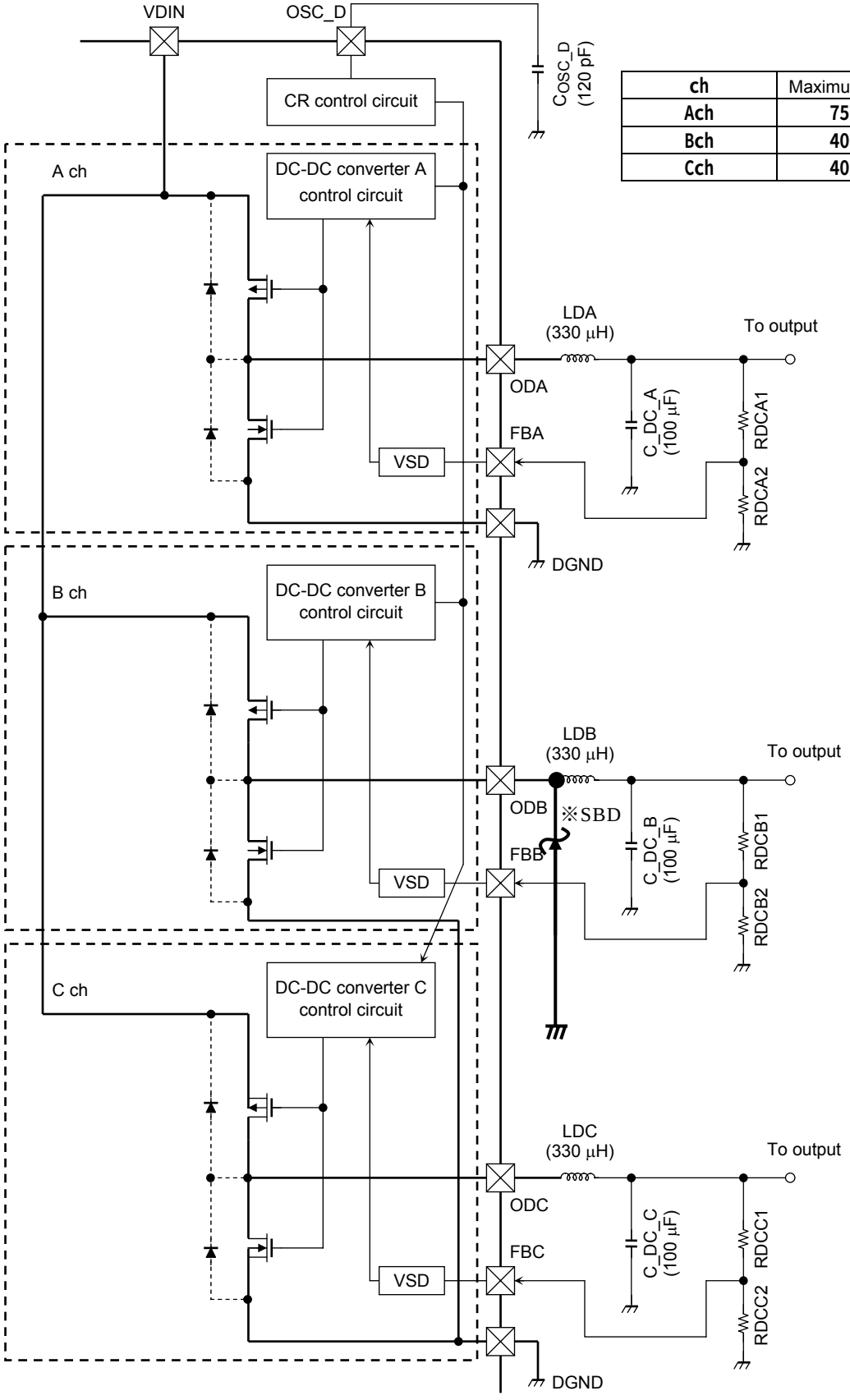
5. Output Equivalent Circuit for Motor Driver



The motor output H switch block consists of the upper P-channel DEMOS FET and lower N-channel DEMOS FET.
Each output DEMOS FET is connected to an over current sense circuit (ISD detection circuit) in parallel.

6. DC-DC Converter Circuit

When an open detection circuit is available, Osc_D pin is set to open, the IC shuts down. If the pin is shorted to GND at startup, the IC fails to start operating. (It does not detect in a default.) In the DC-DC converter operating mode, channel B starts operating before channel A or C.

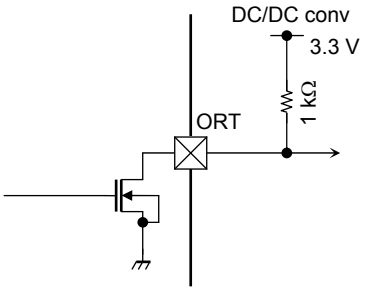


ch	Maximum Rating
Ach	750mA
Bch	400mA
Cch	400mA

※Please Insert a SBD(Schottky Barrier Diode : Recommended "TSB CRS04) between "ODB" Pin to "D-GND" pin.

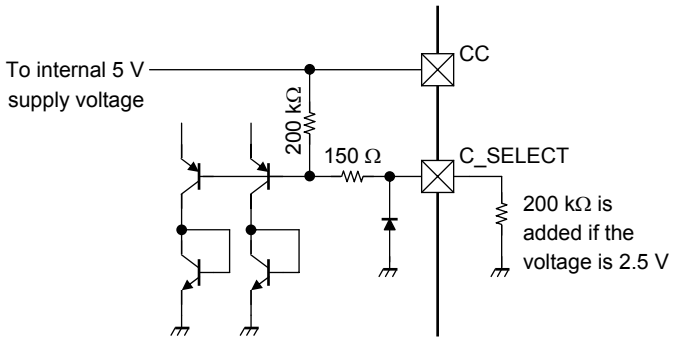
7. Reset Circuit (ORT)

This circuit has an open-drain output. If the output is pulled up with a resistor to the supply voltage, its level becomes low (internally on) at reset and high (internally Hi-Z) during normal operation (at a non-reset).

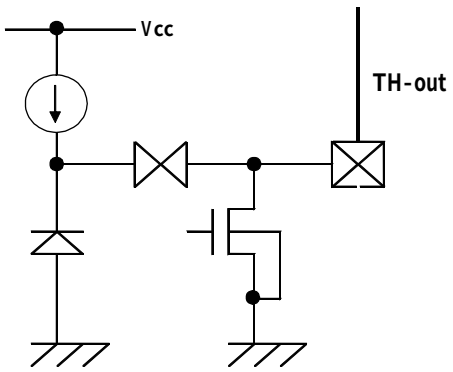


8. DC-DC Converter Select Circuit (C_SELECT)

*: Each internal circuit resistance varies by ±30%.



9. Set Temperature Detection Output Pin (TH-OUT)



It is not necessary to connect a pull-up resistor when choosing ANALOG output mode (terminal :OPEN)

10. Internal Logic Signal Select Output Pin (LOGIC OUT)

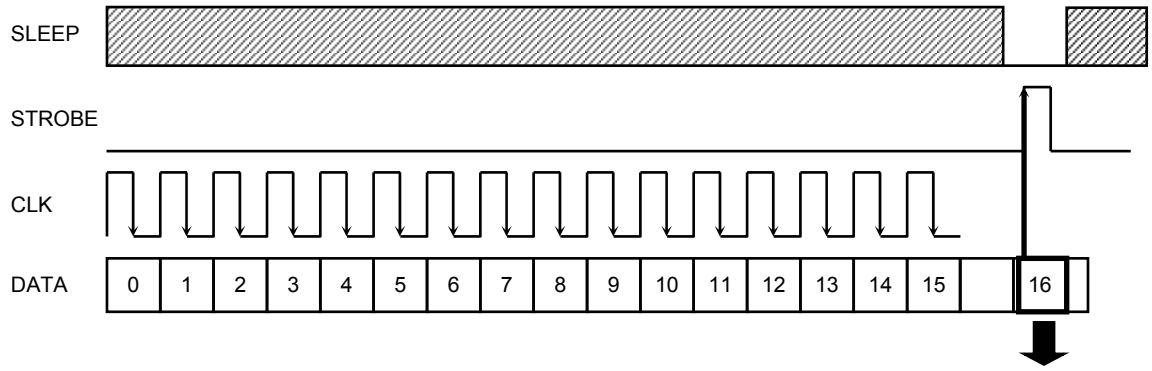
Both the TH-OUT and LOGIC OUT circuits have the same open-drain circuit as the ORT circuit.
If their output pins are pulled up with a resistor to the supply voltage, their levels become low (internally on) at reset and high (internally Hi-Z) during normal operation (at non-reset).

16-Bit Serial Input Signals

Three different pieces of data can be entered and set up by combining the CLK, DATA, STROBE and SLEEP pin inputs.

(1) Extended setup mode (for setting up protection circuits)
(2) Initial setup mode (for setting up motor drive modes)
(3) Stepping motor drive mode (normal drive mode)

Setup Mode Specifications (Initial setup and extended setup modes)



Note: The internal-signal monitoring setting (entered in extended setup mode) is in effect if the DATA signal is high when the STROBE signal is supplied. If the DATA signal is low, initial setup is in effect (initial setup mode).

(1) Extended Setup Mode Function (write enabled only when SLEEP = L and Setup Select = H)

- In the extended setup mode, the protection circuits are set up and a monitor setup (output of a Lo_out pin) of a shutdown signal etc. is performed.

Data Bit	Name	Function	Setting	Default Value
0	SD SELECT 0	Selecting a signal at shut-down	These 4 bits select what shut-down signal to produce. See the next item for explanations about the 4-bit data combinations.	0
1	SD SELECT 1			0
2	SD SELECT 2			0
3	SD SELECT 3			0
4	Unused	—	—	0
5	DCDC VSD SD MASK	Shut-down signal mask	0: Normal operation. See the corresponding item below for explanations about the 3-bit data combinations.	0
6	Motor ISD SD MASK			0
7	TSD SD MASK			0
8	RESET MASK C	Disabling the RESET signal at the shut-down of the corresponding DC-DC converter.	0: Normal operation. 1: If the DC-DC converter concerned is shut down: (1) The RESET signal is not generated. (2) All DC-DC converters other than the DC-DC converter of interest operate normally. (3) The DC-DC converter concerned returns to normal when the SLEEP signal changes from low to high.	0
9	RESET MASK B			0
10	RESET MASK A			0
11	PRE TSD 0	Generating a low signal at the Th_out pin at a temperature of the TSD temperature − X.	12 11 (← bit) 0 0: TSD-20°C 0 1: TSD-30°C 1 0: TSD-40°C 1 1: Analog	0
12	PRE TSD 1			0
13	Unused	Unused	—	0
14	OSCM/D Watch Dog Setting	Specifying whether to cause OSC_M and OSC_D to run.	0: OFF (watchdog disabled) 1: ON (watchdog enabled)	0
15	Unused	Unused	—	0

[Shut-down signal output (SD select)]

These 4 bits are used to select what shut-down signal to generate. Alternatively, they are used to indicate vendor or version code.

The shut-down select signals are released when the SLEEP signal changes form low to high.

Data				Function
Data (3)	Data (2)	Data (1)	Data (0)	Bit
L	L	L	L	Generate the shut-down signal when the channel A DC-DC converter is shut down with DC-DC VSD_H or DC-DC VSD_L.
L	L	L	H	Generate the shut-down signal when the channel B DC-DC converter is shut down with DC-DC VSD_H or DC-DC VSD_L.
L	L	H	L	Generate the shut down signal when the channel C DC-DC converter is shut down with DC-DC VSD_H or DC-DC VSD_L.
L	L	H	H	Unused
L	H	L	L	Generate the shut-down signal when the DC-DC converter is shut down with “DC-DC VSD_H”.
L	H	L	H	Generate the shut-down signal when the DC-DC converter is shut down with “DC-DC VSD_L”.
L	H	H	L	Generate the shut-down signal when the DC-DC converter is shut down with “Motor ISD”.
L	H	L	H	Generate the shut-down signal when the DC-DC converter is shut down with “TSD”.
H	L	L	L	Revision (0) Deliver bit 0 of the version code.
H	L	L	H	Revision (1) Deliver bit 1 of the version code.
H	L	H	L	Revision (2) Deliver bit 2 of the version code.
H	L	H	H	Vender code: Always deliver “detected” in the TB62217FG.
H	H	L	L	Unused
H	H	L	H	Unused
H	H	H	L	Unused
H	H	H	H	Unused

*: Data (3 to 0) = “0000” to “0111” are used to indicate a signal filtered in the internal dead-zone time circuit.

[Shut-down mask]

These 3 bits are used to disable the shut-down function concerned. (One bit corresponds to one function. When a bit is high, the corresponding function is disabled. Their default value is “LLLL”.)

Data (7): If this bit is high, “TSD” is disabled.
Data (6): If this bit is high, “Motor ISD” is disabled.
Data (5): If this bit is high, “DC-DC VSD” is disabled.

*: Data (4): Unused.

[RESET output mask]

These 3 bits are used as a signal to specify whether to produce the RESET when the respective DC-DC converters are shut down.

No low signal is produced as the RESET even if Data (X) = H and one DC-DC channel = H. The default value of these bits is “L, L, L”.
(When a DC-DC converter is shut down, the RESET is driven low, and all DC-DC channels are turned off.)

If the DC-DC converter concerned is shut down:

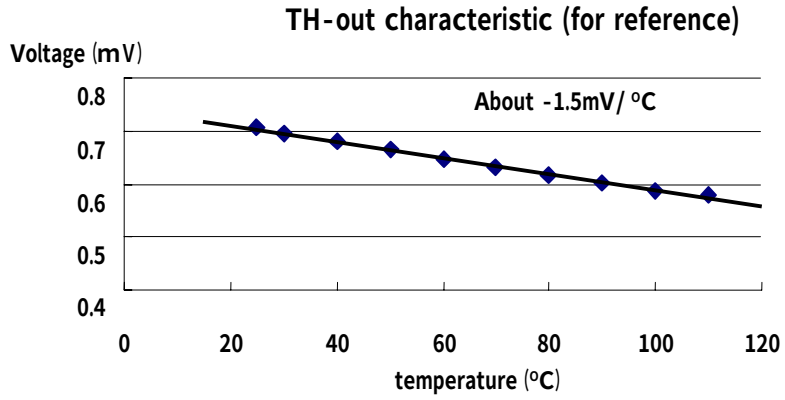
(1) No RESET (ORT) is produced.
(2) All DC-DC converters other than that concerned operate normally (rather than being shut down)
(3) Changing the SLEEP signal from low to high restarts the DC-DC converter.

Data (10): DC-DC converter channel A
Data (9): DC-DC converter channel B
Data (8): DC-DC converter channel C

[PRE TSD]

A low signal is generated at the TH_OUT pin if the current temperature is X degrees lower than the TSD temperature. In analog output mode, a very low voltage proportional to the temperature is generated.
(The analog output mode is dedicated for test use; its specification is not guaranteed and therefore it may not be able to be used in usual operation.)

Data (12, 11) = 0, 0: TH_OUT is generated (low level) at the TSD temperature – 20°C.
Data (12, 11) = 0, 1: TH_OUT is generated (low level) at the TSD temperature – 30°C.
Data (12, 11) = 1, 0: TH_OUT is generated (low level) at the TSD temperature – 30°C.
Data (12, 11) = 1, 1: Analog output mode.



[Revision and vender]

The revision and vendor codes are specific to an individual version of product.

For example: Revision (0, 1, 2) = (L, L, L) and Vendor = (H) for Toshiba #1.0
Revision (0, 1, 2) = (H, L, L) and Vendor = (H) for Toshiba #1.1
Revision (0, 1, 2) = (L, H, L) and Vendor = (H) for Toshiba #1.2
Revision (0, 1, 2) = (H, H, L) and Vendor = (H) for Toshiba #1.3
Revision (0, 1, 2) = (L, L, H) and Vendor = (H) for Toshiba #2.0

[OSC_M/OSC_D open-state detection circuit]

The OSC_M/OSC_D open-state detection circuit tries to detect when a capacitor comes off the OSC_M or OSC_D for some reason by monitoring to see if the frequency gets out of the rated frequency range. When it detects such an event, it shuts down the IC.

The open-state detection circuit is initially off when the power is turned on.
(To cause it to run, a serial signal must be supplied to make the corresponding bit high.)

The frequency range settings are stated below.

(1) Shut down if the current frequency does not fall in the range: OSC_M frequency/64 > OSC_D frequency > OSC_M frequency/2

(2) Shut down if the current frequency does not fall in the range: OSC_D frequency × 32 > OSC_M frequency > OSC_D frequency × 2

Example 1: If the OSC_M frequency is 800 kHz
The IC is shut down when OSC_D frequency > 400 kHz or OSC_D frequency < 12.5 kHz.

2: If the OSC_D frequency is 100 kHz
The IC is shut down when OSC_M frequency > 3200 kHz or OSC_M frequency < 200 kHz.

(2) Initial Setup Mode Select (write enabled only when SLEEP = L and Setup Select = L)

Data Bit	Name	Function	Setting	Default Value
0	Motor Select0	Motor pairing setting (See the corresponding pin assignment table.)	D2 D1 D0 0 0 0: Stepper × 2 0 0 1: Stepper × 1 + DCL × 1 0 1 0: Stepper × 1 + DCS × 2 0 1 1: DCL × 1 + DCS × 2 1 0 0: DCL × 2 1 0 1: DCS × 4	0
1	Motor Select1			0
2	Motor Select2			0
3	TBlank AB 0	Channels A and B Noise rejection dead band time setting (See Note below.)	D4 D3 0 0: (1 ÷ fChop) ÷ 8 × 5 0 1: (1 ÷ fChop) ÷ 8 × 2 1 0: (1 ÷ fChop) ÷ 8 × 3 1 1: (1 ÷ fChop) ÷ 8 × 4	0 0
4	TBlank AB 1			
5	TBlank CD 0	Channels C and D Noise rejection dead band time setting (See Note below.)	D6 D5 0 0: (1 ÷ fChop) ÷ 8 × 5 0 1: (1 ÷ fChop) ÷ 8 × 2 1 0: (1 ÷ fChop) ÷ 8 × 3 1 1: (1 ÷ fChop) ÷ 8 × 4	0 0
6	TBlank CD 1			
7	DC/DC A SW	DC-DC converter channel A operation	0: ON 1: OFF	(Note)
8	DC/DC B SW	DC-DC converter channel B operation	0: ON 1: OFF	(Note)
9	DC/DC C SW	DC-DC converter channel C operation	0: ON 1: OFF	(Note)
10	(A- and B-axis) DC motor Vref (gain)	Channels A and B Internal Vref attenuation ratio setting for constant current in DC motor mode	0: 1/10 1: 1/20	0
11	(C- and D-axis) DC motor Vref (gain)	Channels C and D Internal Vref attenuation ratio setting for constant current in DC motor mode	0: 1/10 1: 1/20	0
12	Test	IC internal test mode setting	Always keep this bit low.	0
13	Test	IC internal test mode setting	Always keep this bit low.	0
14	Test	IC internal test mode setting	Always keep this bit low.	0
15	Unused	—	This bit is not in use. Always keep it low.	0

Note: The initial setting for DATA bits 7, 8, and 9 is determined according to the value of C_SELECT when the VM power is turned on.

tBLANK (noise rejection dead band time)

The TB62217FG incorporates two different dead band times (blanking times) for different motors to be driven so as to prevent malfunction because of switching noise.

(1) Analog tBLANK (for stepping motor mode)

The noise rejection dead band time (analog tBLANK), defined by the motor's AC characteristics, is fixed within the IC. It is used mainly to avoid misjudging Irr (diode recovery time) when a stepping motor is driven with constant current.
It is fixed within the IC; it cannot be altered.

(2) Digital tBLANK (for DC motor mode)

Unlike the analog tBLANK, this tBLANK time, specified when the initial setup mode is selected, is generated digitally from an external chopping period. It is used mainly to avoid misjudging the varistor recovery current that occurs when a DC motor is driven by PWM in the DC motor drive mode.

If the Motor Select signal selects the stepping motor mode, the digital tBLANK is nullified (0 μs), thus enabling only the analog tBLANK time provided within the IC.

Because the digital tBLANK is generated in reference to the OSC_M, it can be changed by altering the OSC_M. (Note that altering the OSC_M also changes other items (motor chopping frequency, dead band time at the time of starting).)

Digital tBLANK time

In the initial setup mode, the tBLANK time can be set to 4 different levels for A-B and C-D pairs as follows:

(1) Immediately after the PHASE has changed
If the PHASE changes, the following time is needed for synchronization with an OSC_M edge and internal synchronization.

tBLANK time = time need for synchronization between OSC_M and PHASE + set tBLANK time = internal processing time (OSC_M × 1) + synchronization time (below OSC_M × 1) + set time

(2) Charging in constant-current operation (limiter operation)
tBLANK time = set tBLANK time

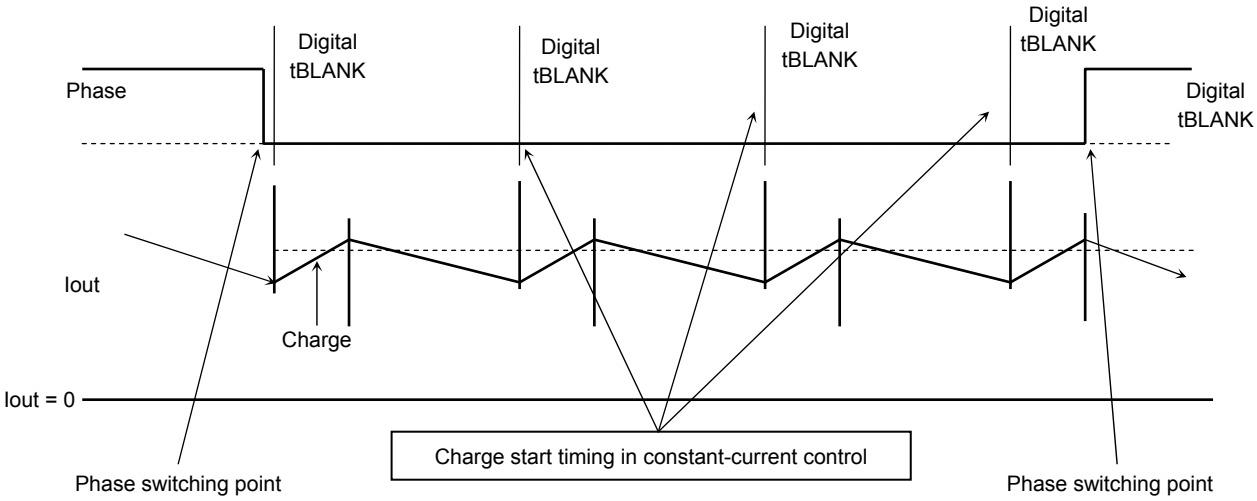
The set tBLANK time is as follows:

tBLANK AB (0, 1) & tBLANK CD (0, 1) =:

0	0: OSC_M period × 5
0	1: OSC_M period × 2
1	0: OSC_M period × 3
1	1: OSC_M period × 4

Caution: For #2.0 and after, tBLANK (0, 0) = OSC_M period × 5.

Digital tBLANK Timing in DC Motor Drive Mode

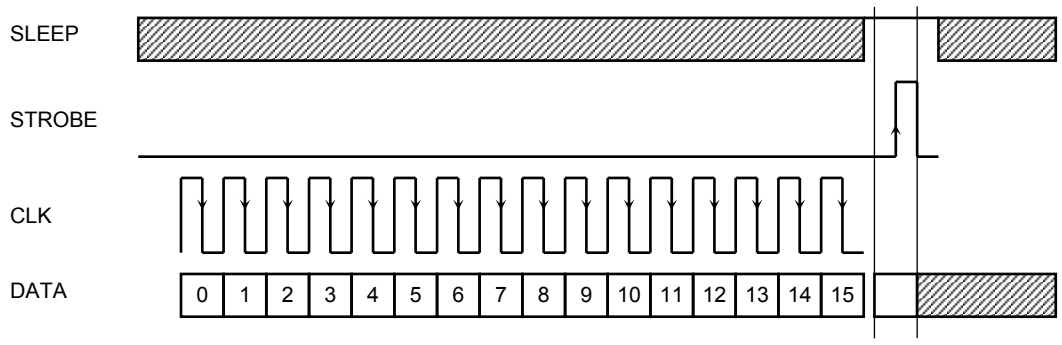


The digital tBLANK time begins immediately after the external PHASE signal is switched or at the charge start timing of the constant-current chopper.
The digital tBLANK is effective only in the DC motor drive mode.
The decay mode for DC motor driving is “Fast Decay”.

(3) Data for Normal Stepping Motor Operation

The TB62217FG signals for normal stepping motor operation can be entered in much the same manner as the drive data of the Toshiba TB62202AF.

Data Bit	Name	Function	Setting
0	Torque A0/B0	Current range setting	A1/B1 A0/B0 0 0 : 50% 0 1 : 70% 1 0 : 85% 1 1 : 100%
1	Torque A1/B1		
2	Decay Mode B0	Channel B current attenuation ratio setting (Mixed Decay Mode)	B1 B0 0 0 : 12.5% Decay Mode 0 1 : 37.5% Decay Mode 1 0 : 75% Decay Mode 1 1 : Fast Decay Mode(100%)
3	Decay Mode B1		
4	Current B0	Channel B current setting 4-bit current data (Using 4 data bits can divide each step into 16.) (“0000”: All-output OFF mode)	See Setting Table (3).
5	Current B1		
6	Current B2		
7	Current B3		
8	Phase B	Channel B current phase information	1: OUT B+ is high. 0: OUT B− is high.
9	Decay Mode A0	Channel A current attenuation ratio setting (Mixed Decay Mode)	A1 A0 0 0 : 12.5% Decay Mode 0 1 : 37.5% Decay Mode 1 0 : 75% Decay Mode 1 1 : Fast Decay Mode(100%)
10	Decay Mode A1		
11	Current A0	Channel A current setting 4-bit current data (Using 4 data bits can divide each step into 16.) (“0000”: All-output OFF mode)	See Setting Table (4).
12	Current A1		
13	Current A2		
14	Current A3		
15	Phase A	Channel A phase information	1: OUT A+ is high. 0: OUT A− is high.



The initial setup latch, extended setup latch, or normal motor latch is selected as a write latch according to the logical level of the SLEEP signal and the polarity of the DATA signal at an STROBE signal edge.
If the SLEEP signal is low, the setup latch is selected when the STROBE changes from low to high (initial setup if DATA = low and extended setup if DATA = high). If the SLEEP is high, the normal motor latch is selected. Don't care the level of the SLEEP during data transfer.
The stepping motor latches (for both A-B and C-D pairs) are initialized when the SLEEP signal changes from high to low or from low to high.
All registers are initialized at POR.
The pins used to write during SLEEP include the DATA AB, CLOCK AB, and STROBE AB pins.

Setting Table (1) D0 and D1

Torque setting

The peak torque current can be switched using 2-bit data. (Switching is the same for both the A-B and C-D pairs.)

Data Bit	Name	Function	Torque 1	Torque 0	Setting Torque (typ.)
0 1	Torque0 Torque1	Sets current range	0	0	50%
			0	1	70%
			1	0	85%
			1	1	100%

Setting Table (2) D2, D3, D9, and D10

Decay mode x1 and x0 settings

A value of 37.5% is recommended for a typical condition. Data of (0, 0) specifies a 12.5% decay mode.

Data Bit	Name	Function	Decay Mode 1	Decay Mode 0	Setting Decay mode
2 3 9 10	Decay Mode A1/A0 Decay Mode B1/B0	Sets mixed decay	0	0	Mixed Decay Mode: 12.5%
			0	1	Mixed Decay Mode: 37.5%
			1	0	Mixed Decay Mode: 75%
			1	1	Fast Decay Mode (100%)

Setting Table (3) D4, D5, D6, and D7

Current B setting

Data Bit	Step	Current B3	Current B2	Current B1	Current B0	Set angle (degrees)	Current (%)
4 5 6 7	16	1	1	1	1	90	100
	15	1	1	1	1	84	100
	14	1	1	1	0	79	98
	13	1	1	0	1	73	96
	12	1	1	0	0	68	92
	11	1	0	1	1	61	88
	10	1	0	1	0	56	83
	9	1	0	0	1	51	77
	8	1	0	0	0	45	71
	7	0	1	1	1	39	63
	6	0	1	1	0	34	56
	5	0	1	0	1	28	47
	4	0	1	0	0	23	38
	3	0	0	1	1	17	29
	2	0	0	1	0	11	20
	1	0	0	0	1	6	10
	0	0	0	0	0	0	0

Setting Table (4) D11, D12, D13, and D14

Current A setting

Data Bit	Step	Current A3	Current A2	Current A1	Current A0	Set angle value (degrees)	Current (%)
11 12 13 14	16	1	1	1	1	90	100
	15	1	1	1	1	84	100
	14	1	1	1	0	79	98
	13	1	1	0	1	73	96
	12	1	1	0	0	68	92
	11	1	0	1	1	61	88
	10	1	0	1	0	56	83
	9	1	0	0	1	51	77
	8	1	0	0	0	45	71
	7	0	1	1	1	39	63
	6	0	1	1	0	34	56
	5	0	1	0	1	28	47
	4	0	1	0	0	23	38
	3	0	0	1	1	17	29
	2	0	0	1	0	11	20
	1	0	0	0	1	6	10
	0	0	0	0	0	0	0

Setting Table (5) D8 and D15

Phase A setting (this table applies also to phase B.)

The polarity of the phase A current of a stepping motor is determined as listed below.

Data Bit	Name	Function	Phase	Setting Phase
8 15	Phase B Phase A	Switches phase	0	OUT A: L, OUT A-: H OUT B: L, OUT B-: H
			1	OUT A: H, OUT A-: L OUT B: H, OUT B-: L

Functions of External Input Pins

(1) PHASE Input Pin (PHASE X)

This pin indicates the polarity of the H switch used in driving a DC motor. PWM can be applied by performing time control (duty control) on this pin.

Pin No.	Name	Function	Logical Level	Setting Phase
61 64 62 63	PHASE SA SB SC SD	Switches phase	L	OUT X: L, OUT X-: H
			H	OUT X: H, OUT X-: L

(2) ENABLE Input Pin (ENABLE X)

This pin indicates whether to supply the power to a DC motor to be driven.

Pin No.	Name	Function	Logical Level	Setting Enable
54 53 50 49	ENABLE SA SB SC SD	Whether to activate the output	L	OFF (All transistors for the H switch are off.)
			H	Active

(3) SLEEP Input Pin

When the level of this pin is switched from high to low or low to high, all motor drive registers are cleared (all bits of the 16-bit latch for selecting a motor drive are cleared to low).
After the IC is shut down in motor ISD operation, changing the SLEEP signal from high to low and to high again causes the IC to return to normal.

Pin No.	Name	Function	Logical Level	Setting Sleep
1	SLEEP	Power saving mode	L	Power consumption reduction mode and initial setup mode
			H	Motor operation mode

(4) C_SELECT Input Pin

This pin determines which DC-DC converter to run (ON-OFF combinations) when the power is turned on.

Pin No.	Name	Function	Logical Level	Setting Phase
48	C_SELECT	DC-DC converter mode at start	Low	A ch: OFF B ch: OFF C ch: OFF
			Mid	A ch: ON B ch: ON C ch: OFF
			High	A ch: OFF B ch: ON C ch: ON

Note: If the C_SELECT pin is on the mid level, channel B is turned on before channel A. If it is high, channel B is turned on before channel C.

Protection Operations

(1) When the RESET output mask is "1" in the extended setup mode

Detected Error and Detection Block					Operation State				Reset Output	Reset Method
DC/DC A	DC/DC B	DC/DC C	Motor	Entire IC	DC/DC A	DC/DC B	DC/DC C	Motor		
VSD	VSD	VSD	ISD	TSD						
Not detected	Not detected	Not detected	Not detected	Not detected	Normal operation	Normal operation	Normal operation	Normal operation	H	—
Detected	Not detected	Not detected	Not detected	Not detected	DCDC OFF	Normal operation	Normal operation	Normal operation	H	SLEEP/POR
Not detected	Detected	Not detected	Not detected	Not detected	Normal operation	DCDC OFF	Normal operation	Normal operation	H	SLEEP/POR
Not detected	Not detected	Detected	Not detected	Not detected	Normal operation	Normal operation	DCDC OFF	Normal operation	H	SLEEP/POR
Not detected	Not detected	Not detected	Detected	Not detected	Normal operation	Normal operation	Normal operation	OFF	L pulse	SLEEP/POR
Not detected	Not detected	Not detected	Not detected	Detected	Shut down	Shut down	Shut down	Shut down	L	POR

Stop state in the protection operations listed above

- Shut-down = all the functions stop as a failure related to the entire system occurs. They can be restarted only by initializing using the POR when the VM power is turned on again.
- OFF = only the motor block stops operating. It can be restarted by changing the SLEEP signal from high to low and to high again.
- L Pulse: The ORT keeps producing low pulses for 40 ms (if OSCM = 800 kHz).
- DC-DC OFF = only the DC-DC converter concerned stops operating. It can be restarted as stated below depending on the logic level on which the SLEEP signal is when the converter stops operating.

  (1) If the SLEEP is low when the DC-DC converter stops, it can be restarted by changing the SLEEP signal from low to high.
  (2) If the SLEEP is high when the DC-DC converter stops, it can be restarted by changing the SLEEP signal from high to low and to high again.

(2) When the RESET output mask is "0" in the extended setup mode

Detected Error and Detection Block					Operation State				Reset Output	Reset Method
DC/DC A	DC/DC B	DC/DC C	Motor	Entire IC	DC/DC A	DC/DC B	DC/DC C	Motor		
VSD	VSD	VSD	ISD	TSD						
Not detected	Not detected	Not detected	Not detected	Not detected	Normal operation	Normal operation	Normal operation	Normal operation	H	—
Detected	Not detected	Not detected	Not detected	Not detected	Shut Down	Shut Down	Shut Down	Shut Down	L	POR
Not detected	Detected	Not detected	Not detected	Not detected	Shut Down	Shut Down	Shut Down	Shut Down	L	POR
Not detected	Not detected	Detected	Not detected	Not detected	Shut Down	Shut Down	Shut Down	Shut Down	L	POR
Not detected	Not detected	Not detected	Detected	Not detected	Normal operation	Normal operation	Normal operation	OFF	L Pulse	SLEEP/POR
Not detected	Not detected	Not detected	Not detected	Detected	Shut Down	Shut Down	Shut Down	Shut Down	L	POR

Stop state in the protection operations listed above

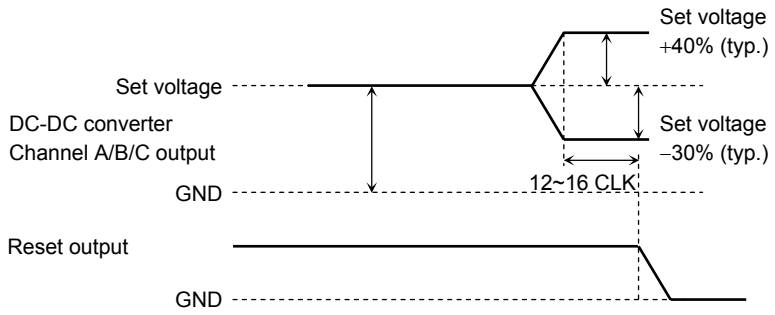
- Shut-down = all the functions stop as a failure related to the entire system occurs. They can be restarted only by initializing using the POR when the VM power is turned on again.
- OFF = only the motor block stops operating. It can be restarted by changing the SLEEP signal from high to low and to high again.
- Low Pulse: Low pulses are generated for 40 ms (if OSCM = 800 kHz).

Protection Circuit Dead Band Time
(example in which the reference clock (Osc_M) frequency is 800 kHz)

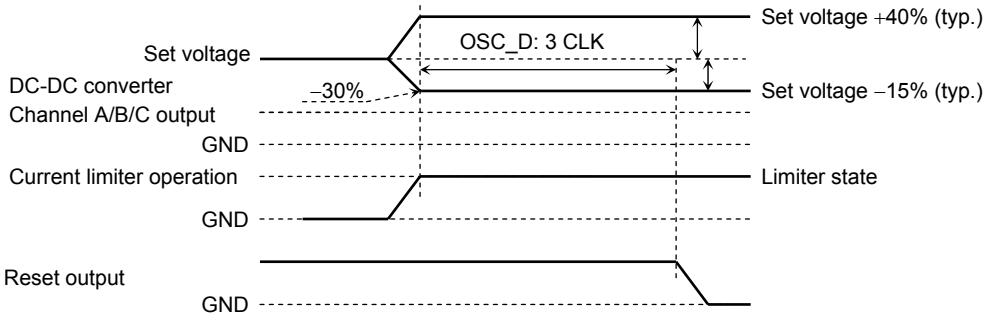
Protection Function	Block Detected	Protection Mask Width	Example: Time for OSCM = 800 kHz	Reset Method
TSD	Entire IC	12 to 16CLK	15 to 20 μs	Supplying VM power again
ISD	DC-DC converter	No function is available	—	—
	Motor	4 to 8CLK	5 to 10 μs	Driving the SLEEP pin low or supplying VM power again
VSD	DC-DC converter	12 to 16CLK	15 to 20 μs	Supplying VM power again

Note: To put protection into effect, the protection circuit must keep operating for at least the time stated above.

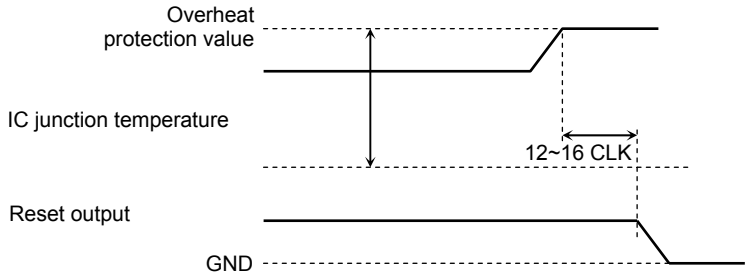
(1) Extreme Voltage Drop Protection Function VSD (when detected, the IC is shut down)



(2) Extreme Voltage Drop Protection Function VSD During Current Limiter Operation (when detected, the IC is shut down)

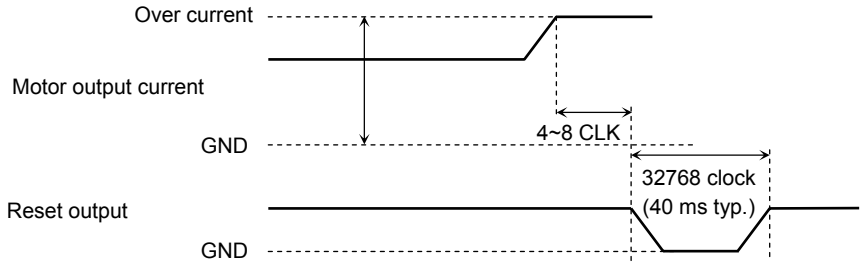


(3) IC Overheat Protection Function (TSD) (when detected, the IC is shut down)



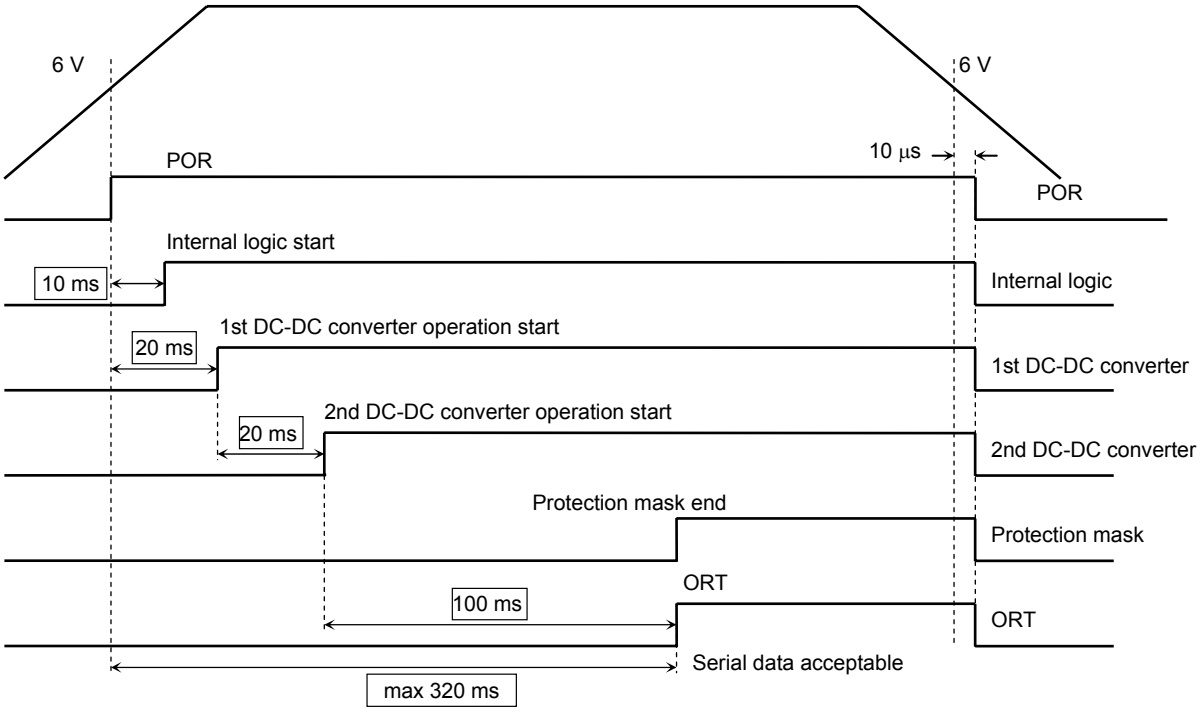
Note: A low-pulse period of 40 ms is applied when OSC_DM frequency = 800 kHz and clock = 1.25 μs.

4) Motor Over Current Protection Function (when detected, only the motor is stopped)



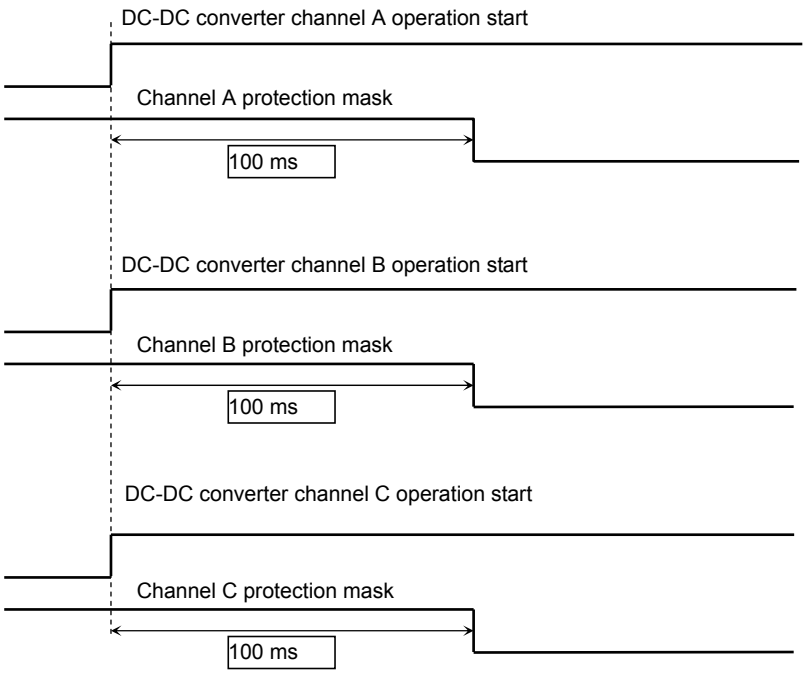
Power Supply Sequence

If the C_SELECT pin is driven mid or high
The 1st DC-DC converter represents channel B, and the 2nd DC-DC converter, channel A or C.



Note: If the C_SELECT pin specifies that all DC-DC converters be off, the ORT reset time is 320 ms.

If serial data specifies DC-DC converters be turned on after the power is turned on (C_SELECT: Low)



Maximum Ratings (Ta = 25°C)

Characteristics	Symbol	Rating	Unit	Remark
Motor output voltage	V_M	50	V	
Motor output current	I_{OST}	1.3	A/phase	Stepper
(Note 1)	I_{OSAP}	8 ?	A	DC motor S (500 ns)
(Note 2)	I_{OSAE}	3	A	DC motor S (100 ms)
DC-DC converter output current	$I_{CO\ A}$	750	mA	
	$I_{DC\ B}$	400	mA	
	$I_{DC\ C}$	400	mA	
Current detection pin voltage	V_{RS}	VM ± 4.5	V	
Reset pin supply voltage	V_{RST}	5	V	
Reset output current	I_{RST}	−60	mA	
Logic input voltage	V_{IN}	−0.4 to 6.0	V	
Power dissipation	P_D	1.25	W	When Ta exceeds 25°C, this figure must be de-rated by 10.0mW /°C. (Note 3)
		4.2	W	When Ta exceeds 25°C, this figure must be de-rated by 33.65mW /°C. (Note 4)
Operating temperature	T_{opr}	−40 to 85	°C	
Storage temperature	T_{stg}	−55 to 150	°C	
Junction temperature	T_j	150	°C	

Note 1: See other tables for pairing.

Note 2: Peak maximum during DC motor drive (below 500 ns)

Note 3: Stand-alone measurement (Ta = 25°C)

Note 4: When the IC is mounted on a dedicated board (Ta = 25°C)
Ta: IC ambient temperature
Topr: IC ambient temperature during operation
T_j: IC chip temperature during operation
The maximum T_j value is limited by the TSD (thermal shut-down circuit) temperature

Recommended Operating Conditions (Ta = 0 to 85°C)

Characteristics	Symbol		Test Condition	Min	Typ.	Max	Unit
VM supply voltage	V_M		Excluding motor block	6 (Note 1)	27	40	V
			Motor block	18	27	40	
Output current	I_{OLA}	Stepper	Per phase (in single-axis drive) at Ta = 25°C	—	0.6	1.0	A
	I_{OSL}	DC	Per H-bridge with peak of 500 ns at Ta = 25°C	—	0.8	6.4	
			Per H-bridge with pulse of 100 ms at Ta = 25°C	—	0.8	2.4	
DC-DC converter initial output current	$I_{DCi\ A}$ (Note 2)		Before the ORT signal is output	—	—	100	mA
	$I_{DCi\ B}$ $I_{DCi\ C}$ (Note 2)		Before the ORT signal is output	—	—	100	mA
DC-DC converter output current	$I_{DC\ A}$		After the ORT signal is output	—	—	600	mA
	$I_{DC\ B}$ $I_{DC\ C}$		After the ORT signal is output	—	—	300	mA
Logic input voltage	V_{IN}		—	GND	3.3	5.0	V
Clock frequency	f_{CLK}		VM = 40 V	1.0	—	25	MHz
Motor chopping frequency range	fchop			—	100	—	kHz
—	—			—	800	—	—
Vref reference voltage input range	V_{ref}			0.8	2.0	3.0	V

Note 1: A voltage of 7 V or higher is recommended for typical use. A VM voltage range between 6 V (POR voltage) and 7 V inclusive allows the DC-DC converter to exhibit much the same characteristics as when VM = 7 V (except that the voltage error becomes ±10%). However, it is recommended to use the IC at 7 V or higher (partly to allow for a margin of stability), because both the rising POR (power-on reset voltage) and falling POR (shut-down voltage) are 6 V.

Note 2: When the power is turned on, soft start is put in effect by limiting the current to the DC-DC converter input block. The limited current results in the output current being limited. If an attempt is made to turn on the power with a load current flowing, it is likely that the DC-DC converter may fail to start or that the output voltage may abruptly increase when the soft-start current is switched.

Motor Block Electrical Characteristics 1
(unless otherwise specified, Ta = 25°C and VM = 18V ~ 40 V)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Logic input voltage	HIGH	VIH	DC	CLK, STROBE, DATA, ENABLE, SLEEP, and PHASE logic input pins	2.0	—	—	V
	LOW	VIL			—	—	0.8	
Logic input clamp voltage		VIK		IIK = −10 mA	—	—	−0.4	
Logic input hysteresis		VIN(HIS)	DC	CLK, STROBE, DATA, ENABLE, and SLEEP input pins	0.1	0.2	0.3	V
Logic input current		IIN(H)	DC	Vin = 3.3 V at each of the CLK, STROBE, DATA, ENABLE, and SLEEP logic input pins	—	—	60	μA
		IIN(L)			—	—	60	
Operating current (VM pin)		IM1	DC	Sleep Mode Sleep = L, ALL DC/DC = OFF (IC bias Current)	—	—	2	mA
		IM2		Sleep = H OSC_D = 100 kHz, Motor = OFF DC/DC_A = OFF DC/DC_B = 1.5 V DC/DC_C = 3.3 V Iout_chB + Iout_chC = 10 mA	—	—	15	
Output standby current	Upper side	IOH	DC	VRS = VM = 40 V, Vout = 0 V, Output OFF Mode	0	—	1	μA
Output leakage current	Lower side	IOL		VRS = VM = Vout = 40 V Output OFF Mode	−1	—	1	
Comparator reference voltage ratio	HIGH (reference)	VRS (HH)	DC	Vref = 2.0 V, Vref (gain) = 1/10, TORQUE = (H.H) = 100%	—	100	—	%
	MIDDLE HIGH	VRS (HL)		Vref = 2.0 V, Vref (gain) = 1/10, TORQUE = (L.H) = 85%	83	85	87	
	MIDDLE LOW	VRS (LH)		Vref = 2.0 V, Vref (gain) = 1/10, TORQUE = (H.L) = 70%	68	70	72	
	LOW	VRS (LL)		Vref = 2.0 V, Vref (gain) = 1/10, TORQUE = (L.L) = 50%	48	50	52	
Output current difference between channels in constant-current mode		ΔIout1	DC	Output current difference between adjacent channels at Iout = 600 mA	−5	—	5	%
Constant-current output setting difference		ΔIout2	DC	Iout = 600 mA	−5	—	5	%
RS pin current		IRS	DC	VRS = 40 V, VM = 40 V	—	—	10	μA
On-state resistance between motor output transistor drain and source		RON (D-S) 1	DC	Iout = 0.6 A, T_j = 25°C, normal direction	—	0.6	0.72	Ω
		RON (D-S) 1		Iout = 0.6 A, T_j = 25°C, reverse direction	—	0.6	0.72	
		RON (D-S) 2		Iout = 0.6 A, T_j = 105°C, normal direction	—	0.78	1.01	
		RON (D-S) 2		Iout = 0.6 A, T_j = 105°C, reverse direction	—	0.78	1.01	

Motor Block Electrical Characteristics 2
(unless otherwise specified, Ta = 25°C and VM =18V ~ 40 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Vref input voltage	Vref	DC	When motor output is active	0.8	—	3.0	V
Vref input current	Iref	DC	When motor output is inactive and Vref = 2.0 V	—	—	1.0	μA
Vref attenuation ratio	Vref (Gain10)	DC	When motor output is active and Vref = 2 V	1/9.6	1/10	1/10.4	—
	Vref (Gain20)			1/19.2	1/20	1/20.8	
Motor power return voltage	VMR (Up)	DC	—	—	14	15	V
	VMR (Down)			13	14	—	
Recommended capacitance for OSC_M pin	Cosc_M	—	External capacitance at fosc_M = 800 kHz	—	220	—	pF
Operating current for motor over current protection circuit	ISD (Note)	DC	fchop = 100 kHz	3.0	5.0	6.0	A

Note: Over current protection circuit

If an abnormal current higher than the corresponding rating flows through a motor, the overcurrent protection circuit triggers the internal shut-down circuit to turn off the output block. In this case, the currently latched function data is cleared.

The overcurrent protection circuit is kept tripped for the motor block until (1) the power is turned on again or (2) the SLEEP returns to a high level.

If ISD comes in effect, the output becomes inactive (ALL OFF state) and is kept so until a normal condition is recovered. However, be sure to insert a fuse into the power supply for sake of fail-safe.

Electrical Characteristics DC_3
(unless otherwise specified, Ta = 25°C, VM =18V ~ 40 V, and motor Iout = 1.0 A)

Characteristics	Symbol	Test Circuit	Test Condition		Min	Typ.	Max	Unit
Chopper current vector	—	DC	θA = 90 (θ16)		—	100	—	
			θA = 84 (θ15)		—	100	—	
			θA = 79 (θ14)		93	98	—	
			θA = 73 (θ13)		91	96	—	
			θA = 68 (θ12)		87	92	97	
			θA = 62 (θ11)		83	88	93	
			θA = 56 (θ10)		78	83	88	
			θA = 51 (θ9)		72	77	82	
			θA = 45 (θ8)		66	71	76	
			θA = 40 (θ7)		58	63	68	
			θA = 34 (θ6)		51	56	61	
			θA = 28 (θ5)		42	47	52	
			θA = 23 (θ4)		33	38	43	
			θA = 17 (θ3)		24	29	34	
			θA = 11 (θ2)		15	20	25	
			θA = 6 (θ1)		5	10	15	
			θA = 0 (θ0)		—	0	—	

Electrical Characteristics DC_4 (unless otherwise specified, Ta = 25°C and VM = 40 V)

Characteristics	Symbol		Test Circuit	Test Condition	Min	Typ.	Max	Unit
Internal logic supply voltage	Vcc		DC	(Automatically created within the IC) External capacitance: Under consideration	4.5	5.0	5.5	V
TSD operating temperature	T_jTSD (Note 1)		DC	—	130	150	170	°C
PRE TSD detection temperature	PRE TSD		DC	−20°C (serial setting)	110		150	°C
				−30°C (serial setting)	100		140	
				−30°C (serial setting)	90		130	
Th_out output voltage	VTHO (H)	H		When pull up to 3.3 V with an external resistance of 1 kΩ	3.2	—	—	V
	VTHO (L)	L			0	—	0.4	
LOGIC OUT	LO (H)	H			3.2	—	—	V
	LO (L)	L			0	—	0.4	

Note: The maximum T_j should not exceed 120°C.

Thermal shut-down (TSD) circuit

TSD comes in effect if the IC junction reaches a rated temperature. It causes the internal reset circuit to operate, thus turning off the output block. (Only one TSD circuit is mounted on the IC.)

The TSD operating temperature can be set anywhere in a range between 130°C (min) and 170°C (max). When TSD comes in effect, the currently latched function data is initialized and the output is stopped.

Once the supply voltage drops to or below the POR voltage to shut down the IC, increasing the supply voltage above the POR reset voltage initializes and restarts the IC.

DC-DC Converter Block Electrical Characteristics (T_j = 0 to 120°C and VM = 7 to 40 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output voltage error	ΔVout	DC	VM = 6.5 V~40 V T_j = 0~120°C 0.5 mA~600 mA (large) 0.5 mA~300 mA (small) DCDC output = 1.5 to 5 V	−7.0	0	7.0	%
DC-DC converter output-off leakage current	IOL_DC	DC	VM = 40 V, upper side	−0.1	—	0.1	μA
			VM = 40 V, lower side	−0.1	—	0.1	
On-state resistance between output transistor drain and source (large DCDC Unit: Ach)	RON (DS) A1	DC	Iout = 300 mA, T_j = 25°C, reverse direction	—	0.7	0.84	Ω
	RON (DS) A2		Iout = 300 mA, T_j = 105°C, reverse direction	—	0.9	1.1	
On-state resistance between output transistor drain and source (small DCDC Unit: B, Cch)	RON (DS) BC1	DC	Iout = 150 mA, T_j = 25°C, reverse direction	—	1.4	1.7	Ω
	RON (DS) BC2		Iout = 150 mA, T_j = 105°C, reverse direction	—	1.8	2.2	
Current limiter value (steady state)	ILIM (L) DC (large)	DC	—	0.8	1.2	1.6	A
	ILIM (S) DC (small)			0.5	0.6	0.85	
Current limiter value (starting)	ILIM (L) DC (large)		—	0.2	0.3	0.4	A
	ILIM (S) DC (small)			0.2	0.3	0.4	
Abnormal-voltage protection circuit	VSD (U)		In reference to the set voltage. The current limiter is inactive.	+30	+40	+50	%
	VSD (L)			−40	−30	−20	
	VSD (LU)		In reference to the set voltage. The current limiter is active.	+30	+40	+50	%
	VSD (LL)			−20	−15	−5	
OSC_D capacitor value	Cosc_D	—	External capacitor value	47	120	—	pF
Feedback voltage	VFB	DC	—	—	1.5	—	V
C_SELECT voltage	VC_sel	DC	DC/DC A, B, Cch All OFF	—	0	0.8	V
			DC/DC A, Bch ON	1.25	2.5	3.75	
			DC/DC Bch, Cch ON	4.5	5.0	—	

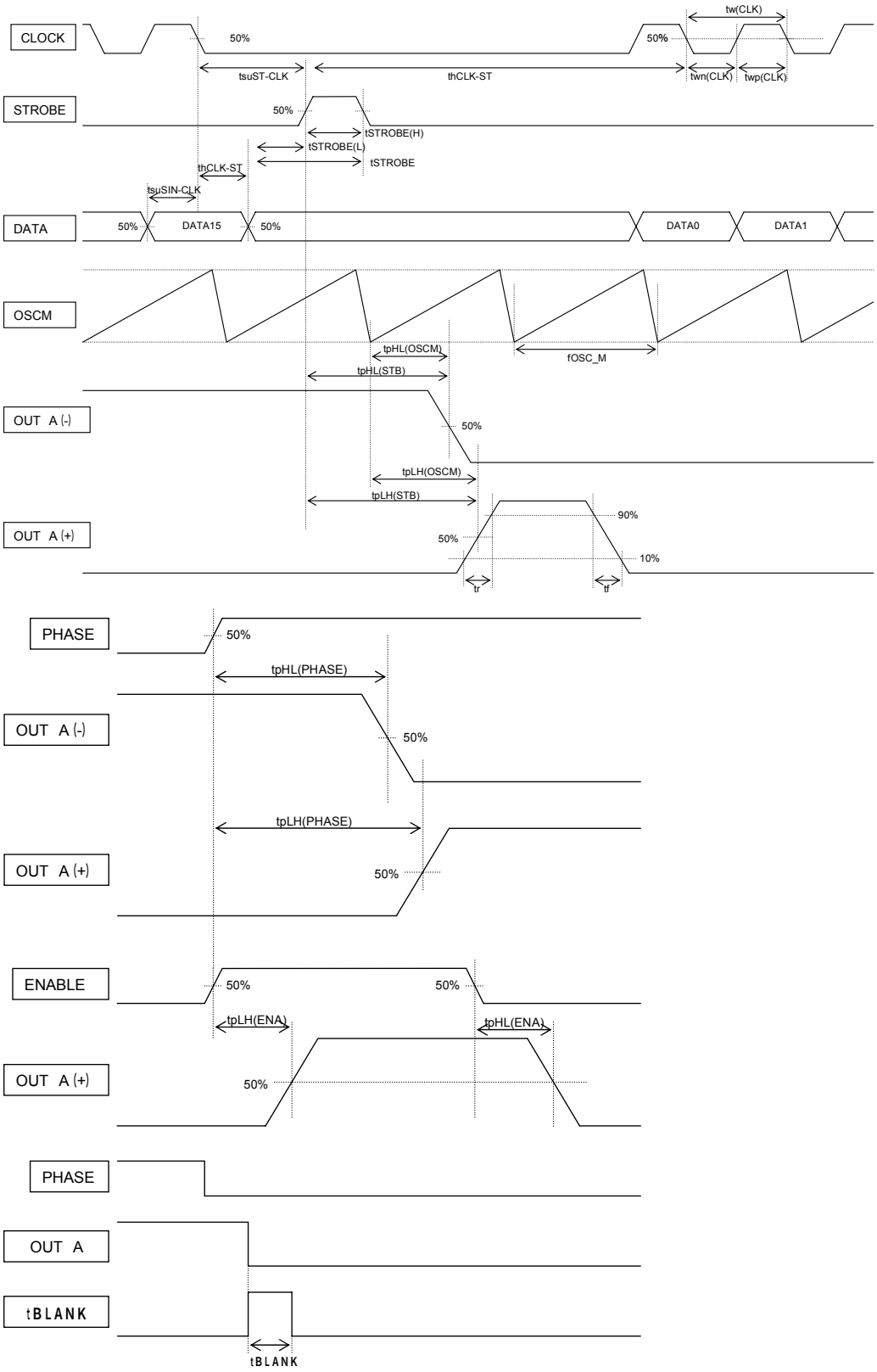
Reset Block Electrical Characteristics DC (T_j = 0 to 120°C and VM = 7 to 40 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
POR output voltage for VM supply voltage detection	V_{MR} (ALL, Up)	DC	Rising side. All functions change from OFF to ON.	5.2	—	6.0	V
	V_{MR} (ALL, Down)		Falling side. All functions change from ON to OFF.	5.2	—	6.0	
ORT signal output current	I_{RST}	DC	Reset pin voltage = 0.4 V	2	—	—	mA
ORT output pin voltage	Vort (H)	DC	Pulled up to 3.3 V with an external resistance of 1 kΩ	3.2	—	—	V
	Vort (L)			0	—	0.4	

Motor Block AC Electrical Characteristics
(Ta = 25°C, VM = 40 A, and motor impedance = 6.8 mH/5.7 Ω)

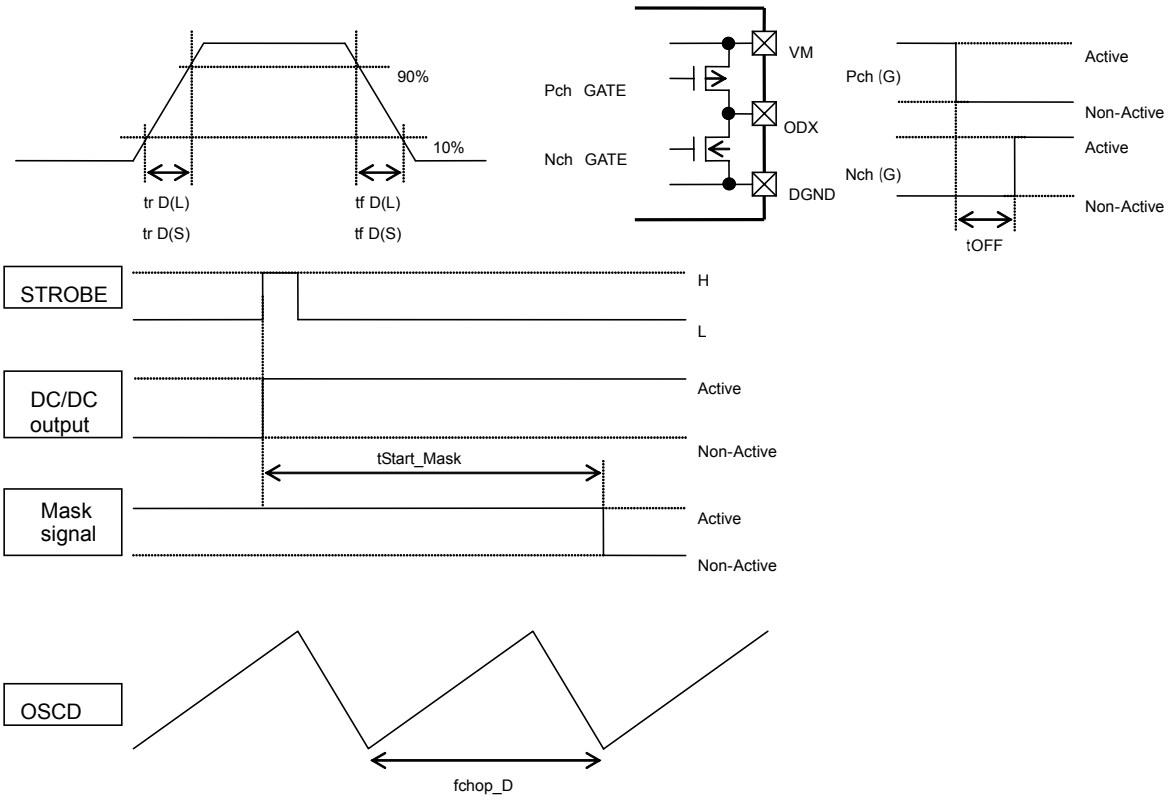
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input clock frequency	fCLK	AC	Vin = 3.3 V CLK input pin	1.0	—	25	MHz
Minimum clock pulse width	tw (CLK)	AC	Vin = 3.3 V	40	—	—	ns
	twp (CLK)			20	—	—	
	twn (CLK)			20	—	—	
Minimum STROBE pulse width	tSTROBE	AC	Vin = 3.3 V	40	—	—	ns
	tSTROBE (H)			20	—	—	
	tSTROBE (L)			20	—	—	
Data setup time	tsuSIN-CLK	AC	Vin = 3.3 V	10	—	—	ns
	tsuST-CLK			10	—	—	
Data hold time	thSIN-CLK	AC	Vin = 3.3 V	10	—	—	ns
	thCLK-ST			10	—	—	
Output switching time	Tr(s)	AC	6.8 mH/5.7 Ω load (Small mode)	0.1	0.3	0.5	μs
	Tf(s)			0.1	0.3	0.5	
	Tr(L)		6.8 mH/5.7 Ω load (Large mode)	0.1	0.3	0.5	
	Tf(L)			0.1	0.3	0.5	
	tpLH (STB)		Step Motor mode 6.8 mH/5.7 Ω load between STROBE (↑) and OUT	—	15	—	
	tpHL (STB)			—	10	—	
	tpLH (OscM)		Step Motor mode 6.8 mH/5.7 Ω load between Osc down edge and OUT	—	1.2	—	
	tpHL (OscM)				2.5		
	tpLH (ENA)		DC Motor mode Between ENABLE edge and OUT	0.3	—	0.9	
	tpHL (ENA)			0.3	—	0.9	
	tpLH (PHASE)		DC Motor mode Between PHASE edge and OUT	0.3	—	0.9	
	tpHL (PHASE)			0.3	—	0.9	
Noise rejection analog dead band time	tBLANK (Analog)	AC	Iout = 0.6 A	200	300	400	ns
Motor chopper reference signal oscillation frequency	f_{OSC_M}	AC	C_OSC_M = 220 pF	600	800	1000	kHz
Frequency range in which motor chopping is supported	fchop (Min)	AC	Output active (Iout = 0.6 A) with fixed steps	40	100	150	kHz
	fchop (Typ.)						
	fchop (Max)						
Motor chopping setting frequency	fchop (M)		Output active (Iout = 0.6 A) M_osc CLK = 800 kHz	—	100	—	kHz

Control signal timing chart



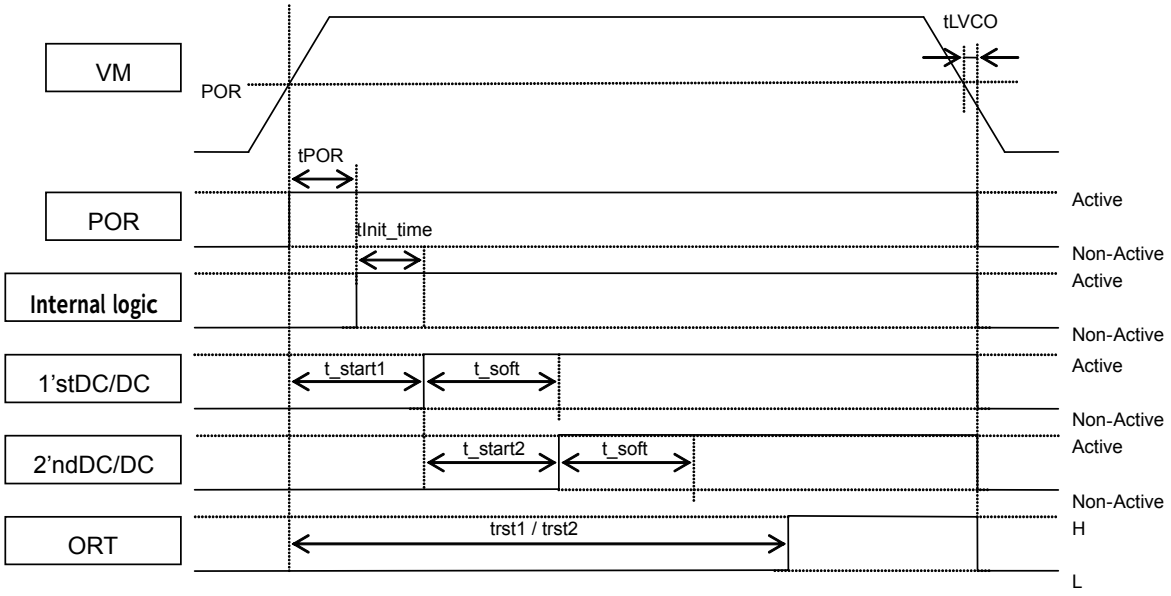
DC-DC Converter AC Electrical Characteristics (T_j = 0 to 120°C and VM = 40 V)

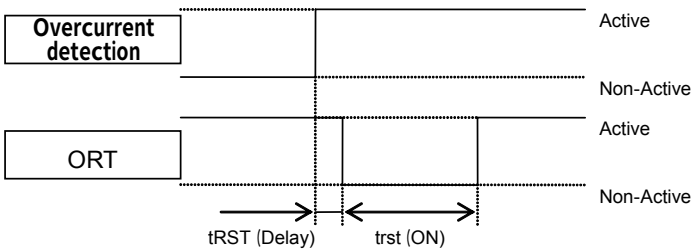
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Output transistor switching characteristic (large)	tr_D(L)	AC	VM = 40 V, DCDC Ach (Large)	—	0.1	—	μs
	tf_D(L)			—	0.1	—	
Output transistor switching characteristic (small)	tr_D(S)	AC	VM = 40 V, DCDC B/Cch (small)	—	0.1	—	
	tf_D(S)			—	0.1	—	
Output transistor feed-through prevention time	tOFF	AC	VM = 40 V	100	300		ns
DC-DC setting frequency	fchop_D (OSC_D)	AC	—	—	100	200	kHz
Protection circuit dead band (MASK) time at startup	tStrart _Mask	AC	The DC-DC converter is turned on independently of others, using serial data. fosc_M = 800 kHz and after the STROBE signal has been accepted	—	100	—	ms
Initial startup delay time	tstart1	AC	At fosc_M = 800 kHz and after VM becomes 6 V or higher but before the first DC-DC converter starts.	—	20	—	ms
Initial startup delay time 2	tstart2	AC	At fosc_M = 800 kHz and after the first DC-DC converter has started but before the second DC-DC converter starts.	—	20	—	ms
Startup soft mode period	tsoft	AC	fosc_M = 800 kHz	—	20	—	ms
LVCO detection dead band time	tLVCO	AC	At fosc_M = 800 kHz and after VM becomes 6 V or lower but before the ORT becomes low.	—	10	—	μs
POR detection dead band time	tPOR	AC	At fosc_M = 800 kHz and after VM becomes 6 V or lower but before the internal logic starts.	—	10	—	ms



Other Electrical Characteristics AC (T_j = 0 to 120°C and VM = 7 to 40 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Startup reset release time 1 (Protection mask time)	trst1 (Init)	AC	From VM power-on POR release fosc_M = 800 kHz (114688 clock pulses)	—	140	—	ms
Startup reset release time 2 (with no DC-DC converter in use)	trst2 (DCDC OFF)	AC	From VM power-on POR release fosc_M = 800 kHz (262144 clock pulses)	—	320	—	ms
ORT output low-pulse width when the motor ISD is active	trst(ON)	AC	fosc_M = 800 kHz (32768 clock pulses)	40	—	—	ms
ORT signal output delay time	tRST (Delay)	AC	IRST = 20 mA Pulled up to CC with a resistance of 200 Ω Ccc = 0.1 μF	—	50	—	ns
Internal initial setup timing	tInit_time	AC	fosc_M = 800 kHz After POR release	—	10	—	ms
SLEEP pulse width	tSleep (ON)	AC	fosc_M = 800 kHz	10	—	—	μs
SLEEP release delay time	tSleep (delay)	AC	fosc_M = 800 kHz	—	—	10	μs





Calculating the Motor Setting Constant Current

The motor setting current value is determined by R_{RS} and Vref as follows:

$$\text{Iout (max)} = \text{Vref (gain)} \times \text{Vref (V)} \times \frac{\text{Torque (Torque} = 100, 85, 70, 50\%: \text{input serial data}}{R_{RS}\,(\Omega) \times 100\%}$$

Assume, for example:

Vref (gain) = 1/10: The attenuation ratio is typically 1/10 when Vref = 1/10.
Vref =2 (V)
Torque =100 (%)

Producing Iout = 1.0 A requires R_{RS} = 0.20 Ω (at least 0.2 W).

The Vref (gain) is fixed at 1/10 for stepping motors and selectable from 1/10 and 1/20 for DC motors.

The error of constant current setting is 5 % when excluding Vref and Rs .

Calculating the Oscillation Frequency (chopping reference frequency) for the Motor and DC-DC Converter Blocks

(1) Calculating the OSC Reference Frequency for the Motor Block (typical)

$$\text{fosc\_M} = 61820 \times \text{C (pF)} \wedge -0.8043 \text{ (kHz)}$$

Hence, the OSC frequency for the motor block is about 810 kHz when Cosc_M = 220 pF.
The chopping frequency for stepping motors is about 1/8 the above frequency, that is, 810/8 (= 101) kHz.
In addition, only the fast decay mode is available for DC motor drive.

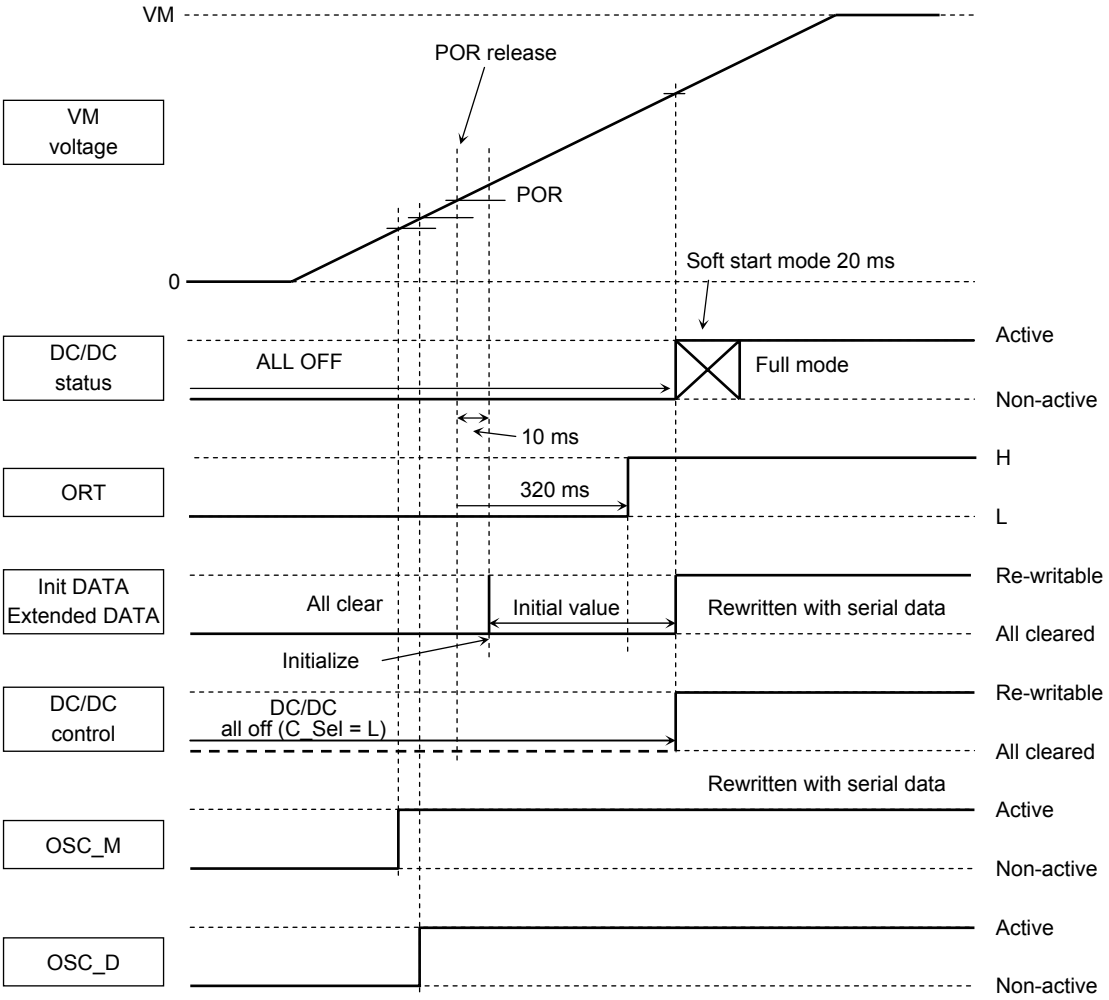
(2) Calculating the OSC Frequency for the DC-DC Converter Block (typical)

$$\text{f OSCD} = 5315.3 \times \text{C (pF)} \wedge -0.8341 \quad \text{(kHz)}$$

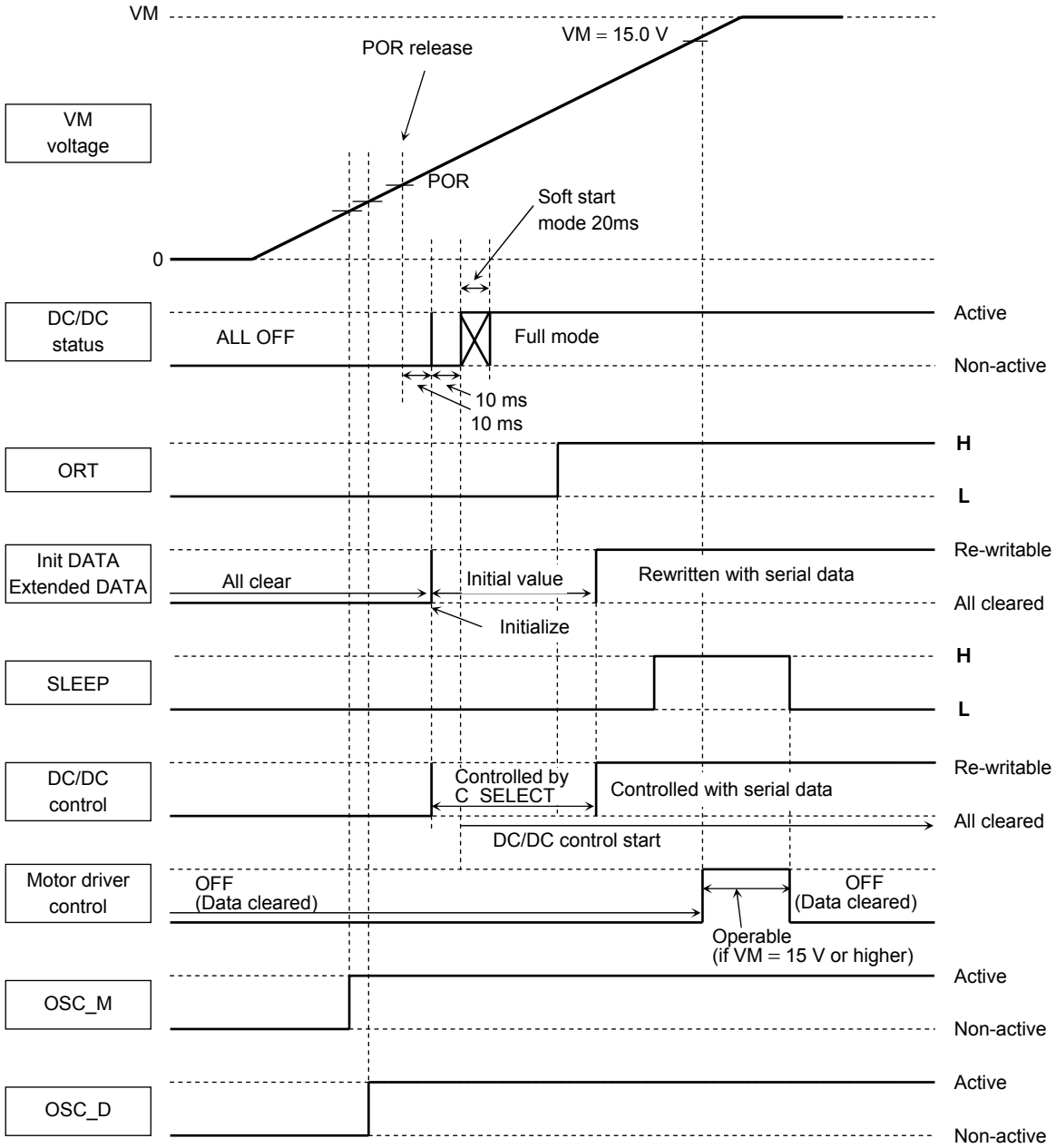
Hence, the OSC frequency for the DC-DC converter block is about 100 kHz when Cosc_D = 120 pF.

Power Supply Sequence

(1) If C_SELECT = low

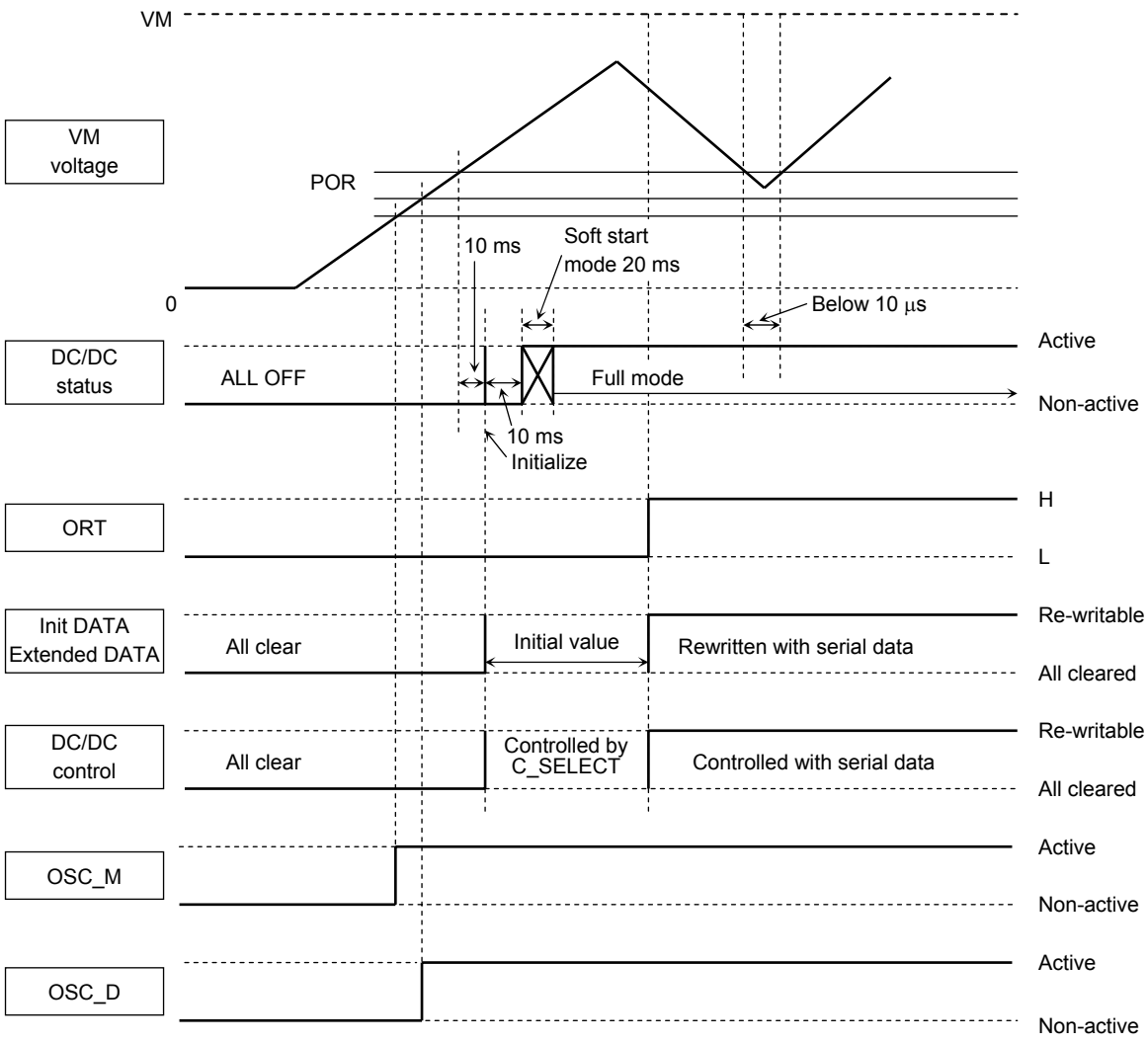


(2) Normal Start (C_SELECT = mid or high)

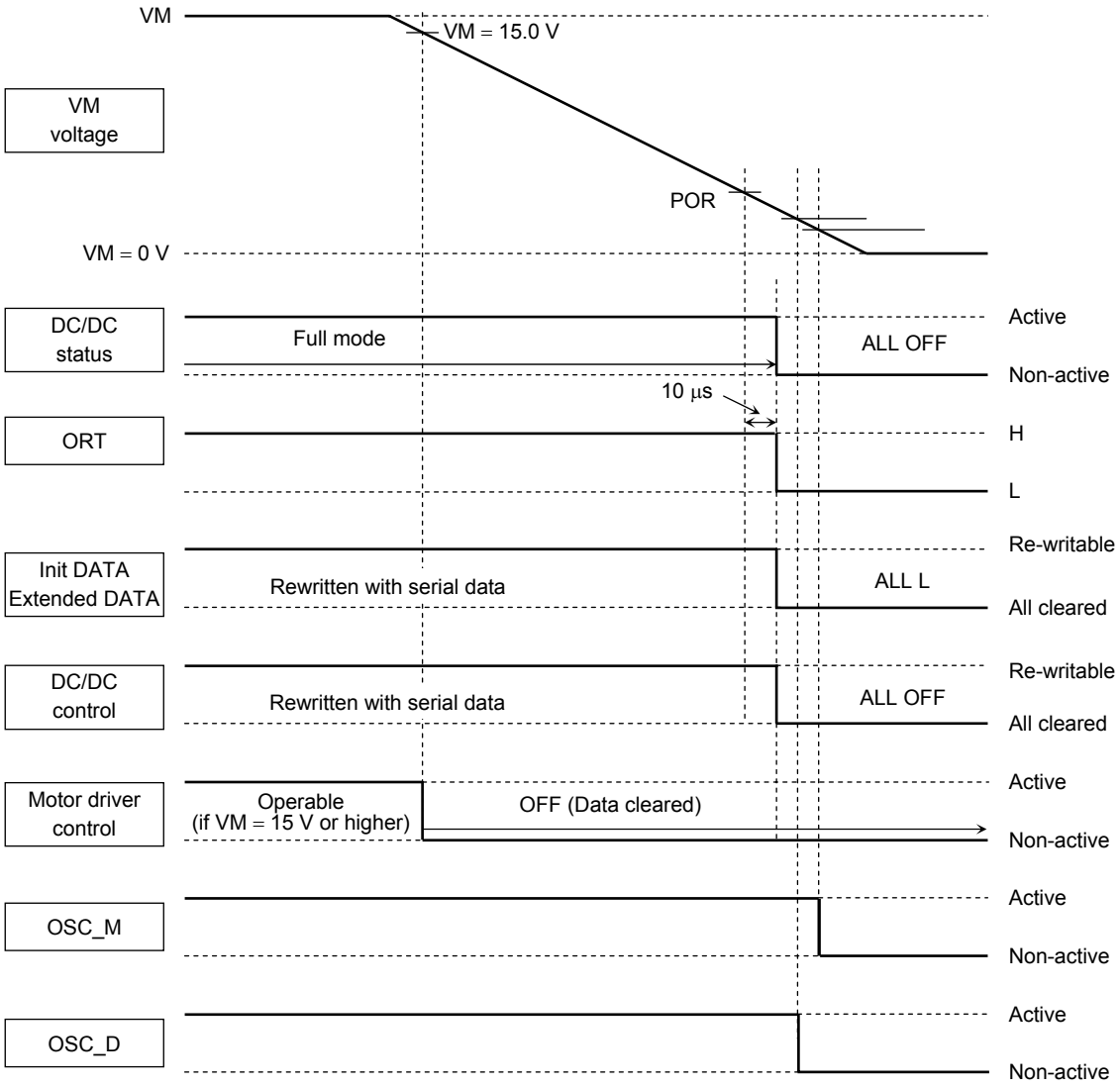


Note: POR release → Initialize 10 ms
Initialize → first DCDC start 10 ms
DCDC soft start mode 20 ms

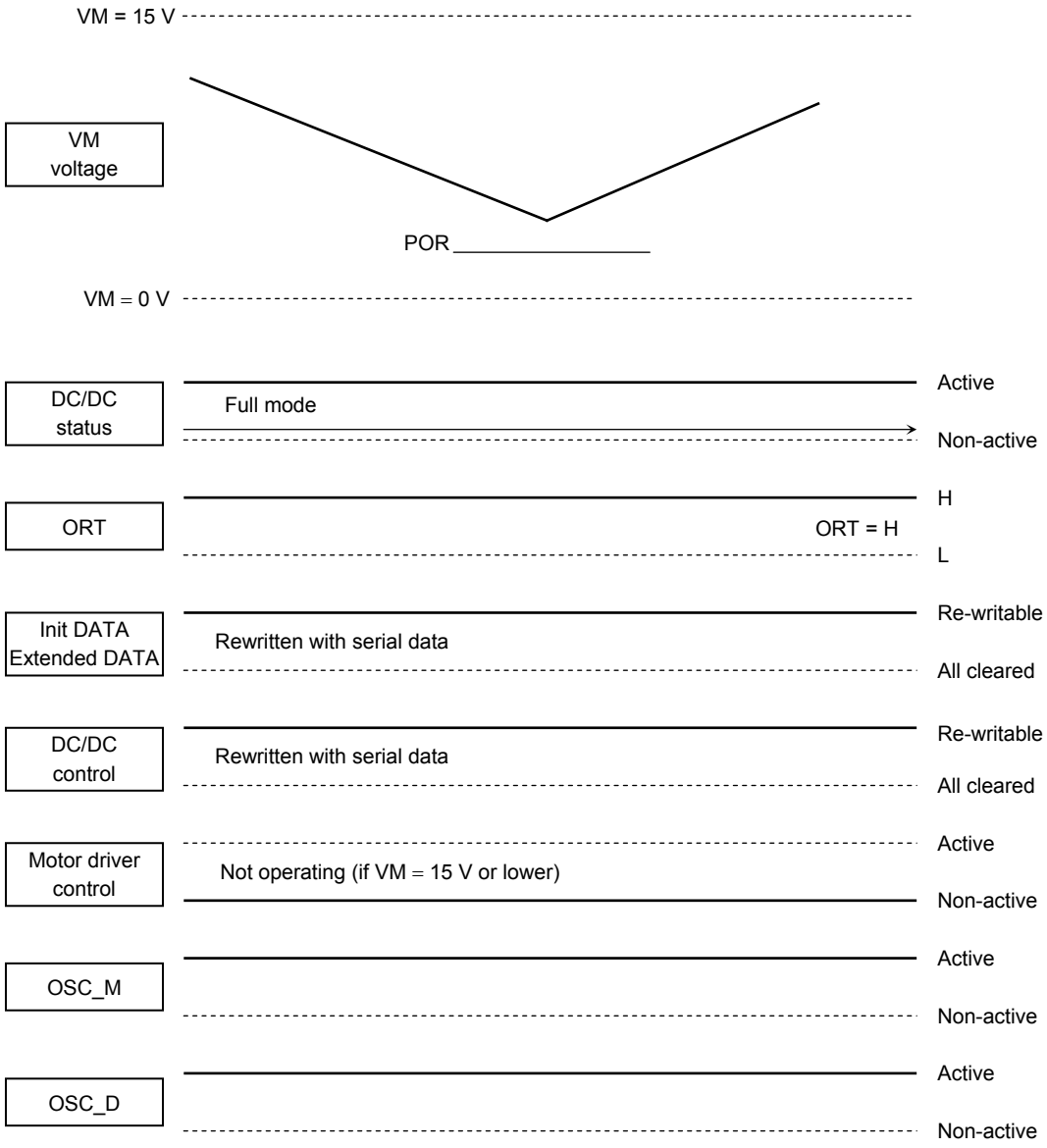
(3) If VM Voltage Drops at Startup (C_SELECT = mid or high)



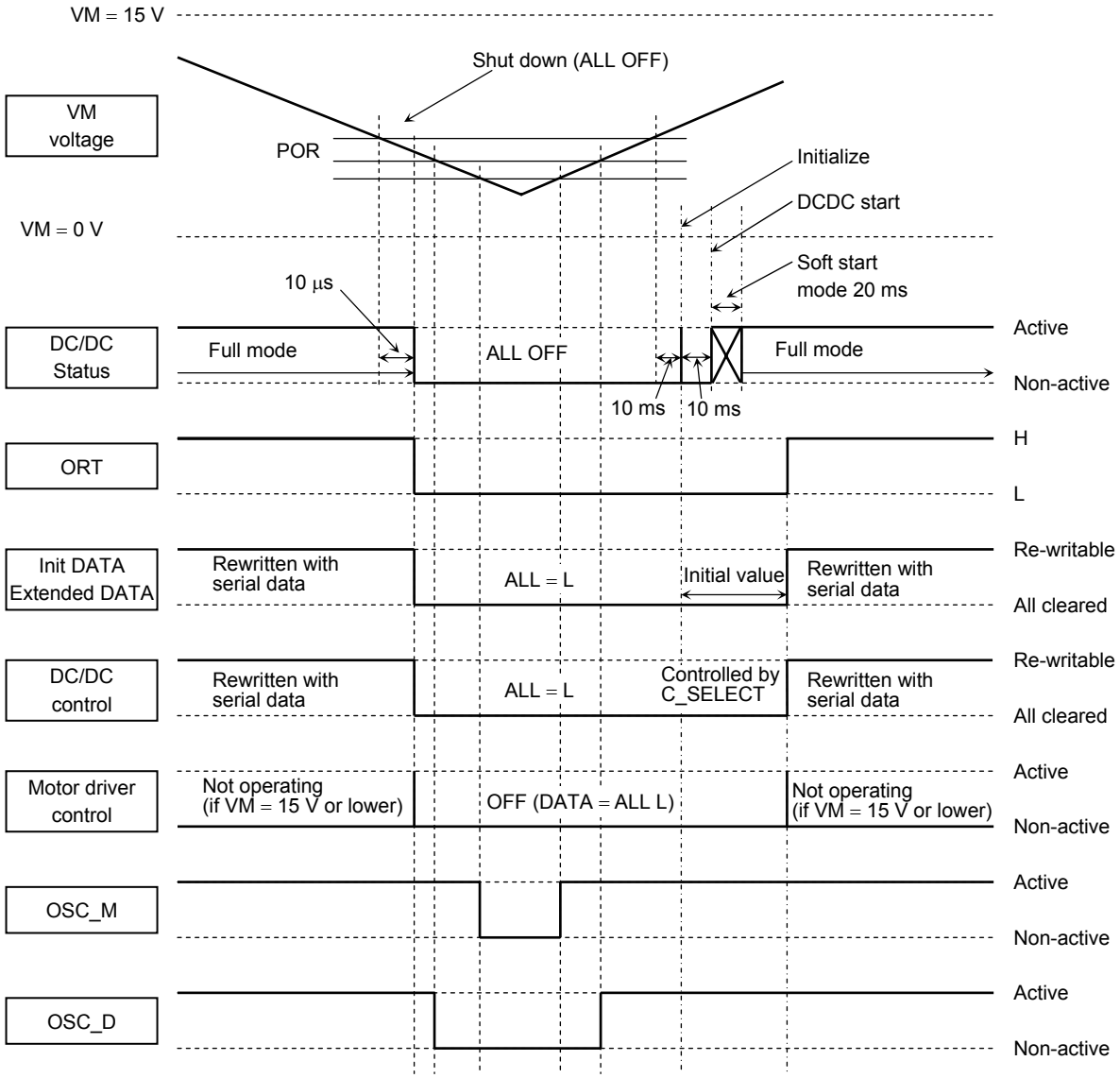
(4) VM Voltage Drop (normal)



(5) Supply Voltage Drop (if the VM supply voltage does not cross the POR level)



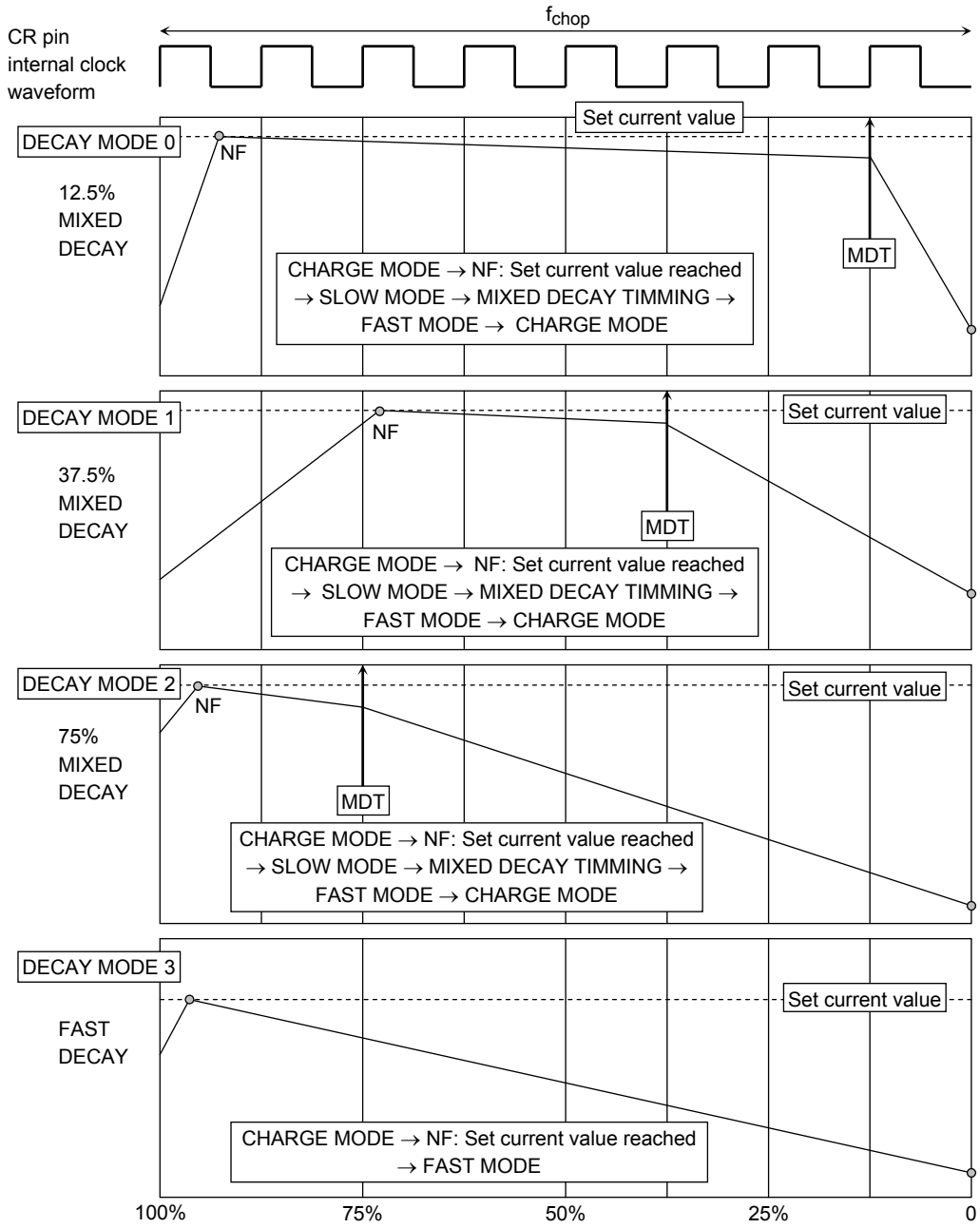
(6) Supply Voltage Drop (if the VM supply voltage crosses the POR level)



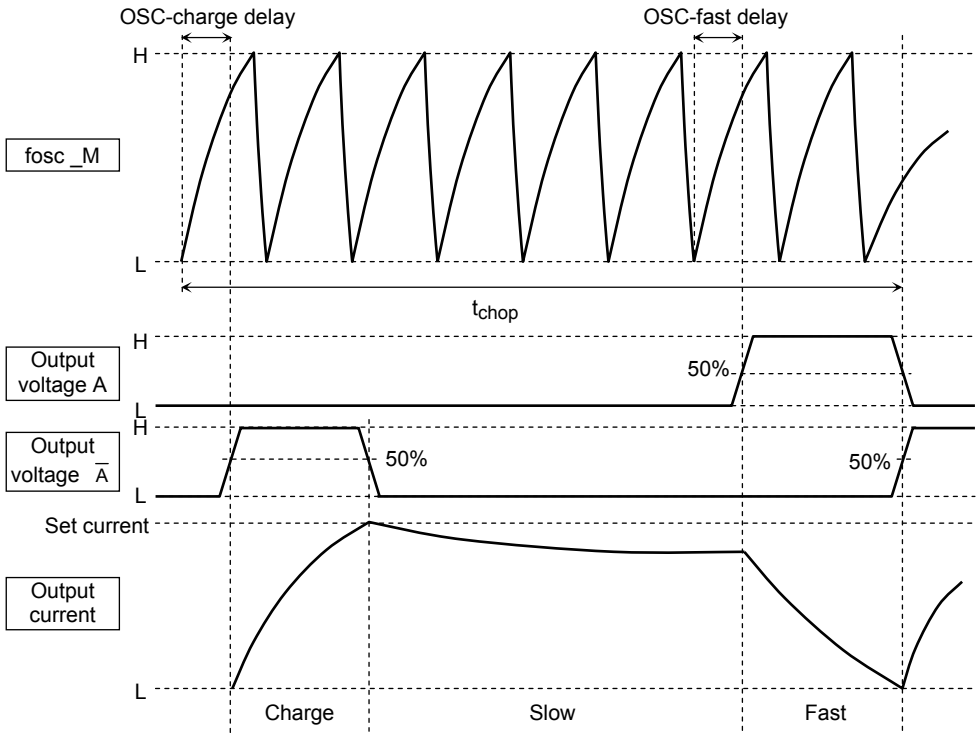
Mixed decay Mode Current Waveform and Setting

In constant-current control, the current fluctuation width (current pulsating component) decay mode can be set to any of four points, 0 to 3, using 2-bit serial data.

The abbreviation “NF” stands for “negative feedback”. It refers to a point where the output current has reached the set current value. The lower the mixed decay timing value, the lower is the current ripple component (current crest value), leading to a lower current decay ability.

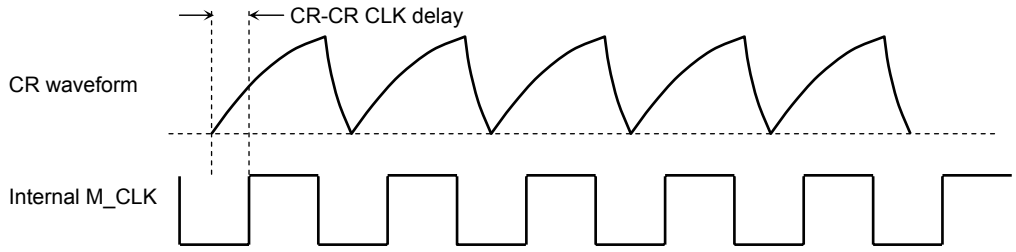


Relationships Between the OSC_M and Output Drive Timing



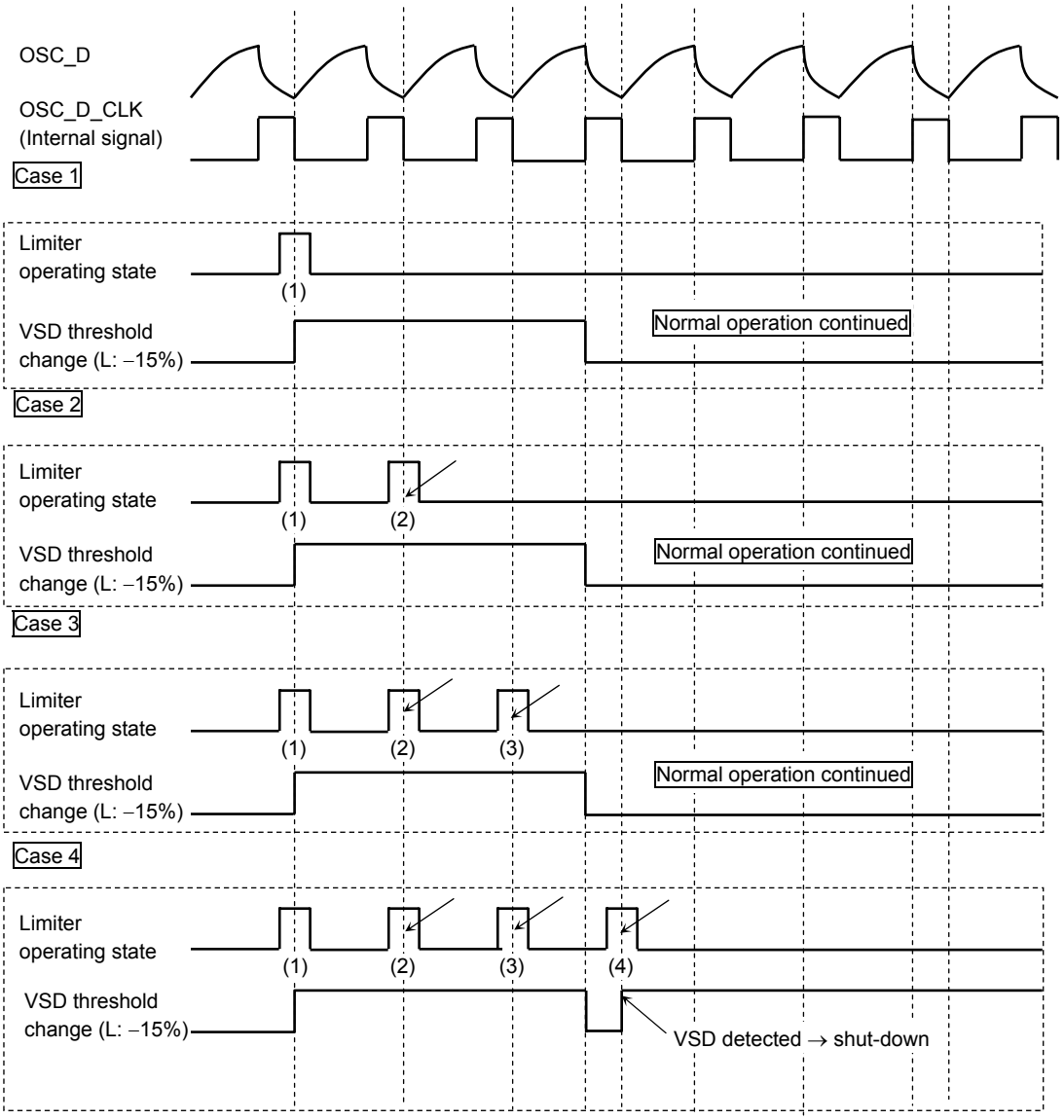
OSC_M and Charge Delay

A delay of up to 1.25 ns (when f_{chop} = 100 kHz and f_{CR} = 800 kHz) can occur between the OSC waveform and internal OSC_M CLK, because the rising level of the OSC waveform is used in converting the OSC waveform to the internal M_CLK.

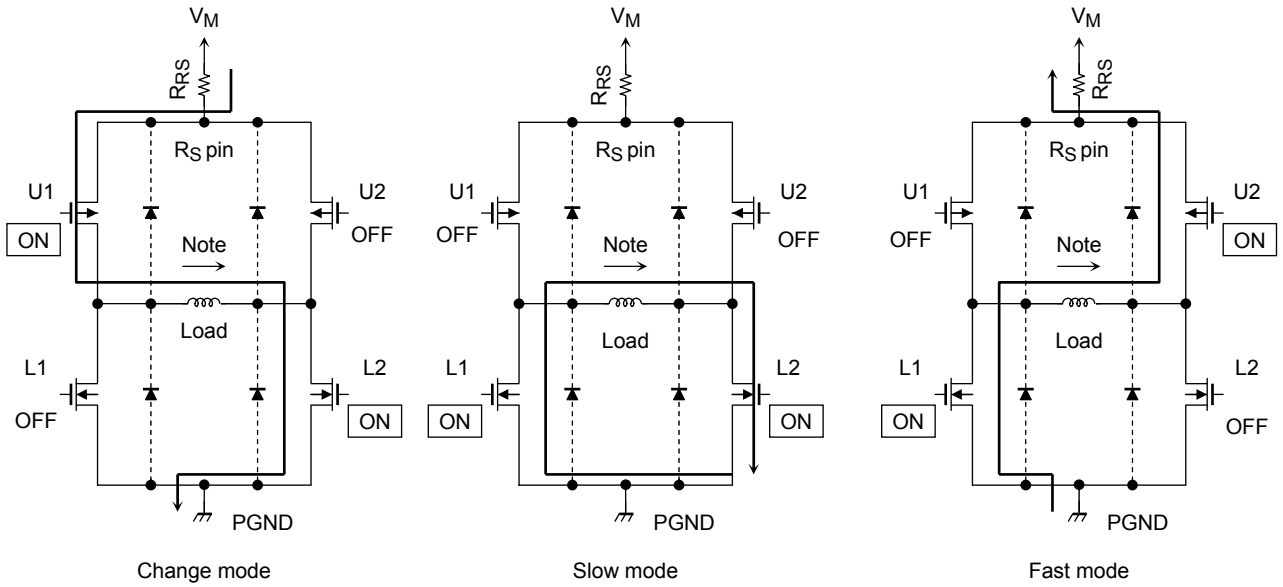


VSD Threshold Change Timing During DC-DC Converter Block Current Limiter Operation

When the limiter enters an operating state, the VSD circuit starts operating if this state continues for 3 OSC_D periods.



Output-stage Transistor Operation Mode



Output-stage Transistor Operation Functions

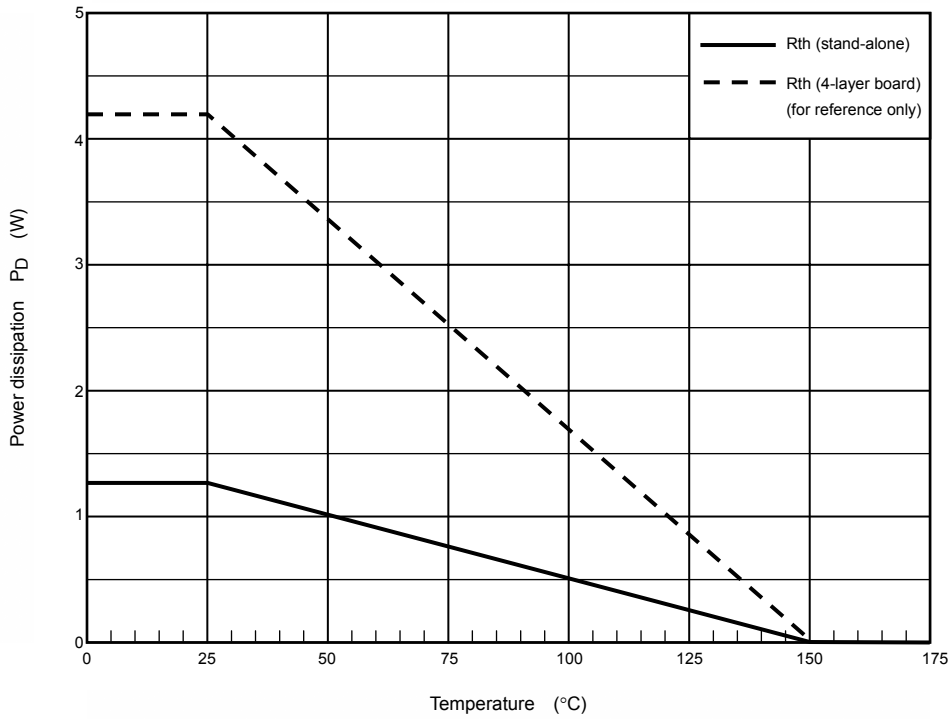
CLK	U1	U2	L1	L2
CHARGE	ON	OFF	OFF	ON
SLOW	OFF	OFF	ON	ON
FAST	OFF	ON	ON	OFF

Note: The above table summarizes how each transistor behaves when the current flows in the indicated direction. The table below summarizes how each transistor behaves when the current flows in the opposite direction.

CLK	U1	U2	L1	L2
CHARGE	OFF	ON	ON	OFF
SLOW	OFF	OFF	ON	ON
FAST	ON	OFF	OFF	ON

PD-Ta (package power dissipation) **This item to be revised once package characteristics are fixed.**

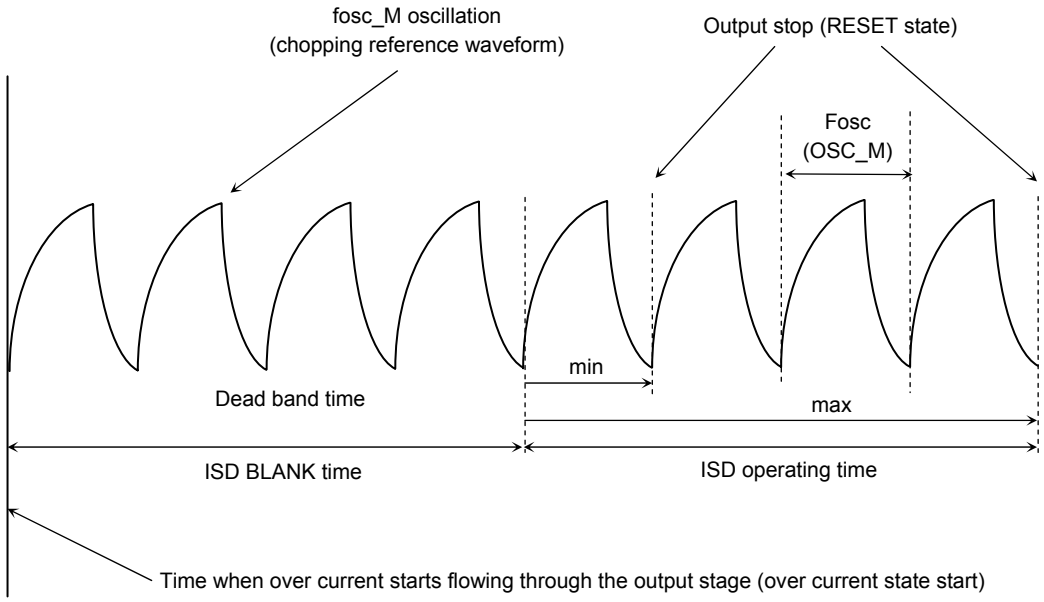
Transient thermal resistance of THQFP64 stand-alone and on a PC board
(for reference only)



THQFP64-P-1010-0.50

Note: The board assumed in simulation is Toshiba's ideal board (for reference only).

Operating Time of The Motor Over Current Protection Circuit
(ISD dead band time and ISD operating time)



Reference diagram: Timing chart showing over current flowing through a motor

The over current protection circuit has the dead band time to avoid detecting over current accidentally from current spikes in switching. The dead band time is in synchronization with the frequency of the OSC for setting up the chopping frequency (OSC_M).

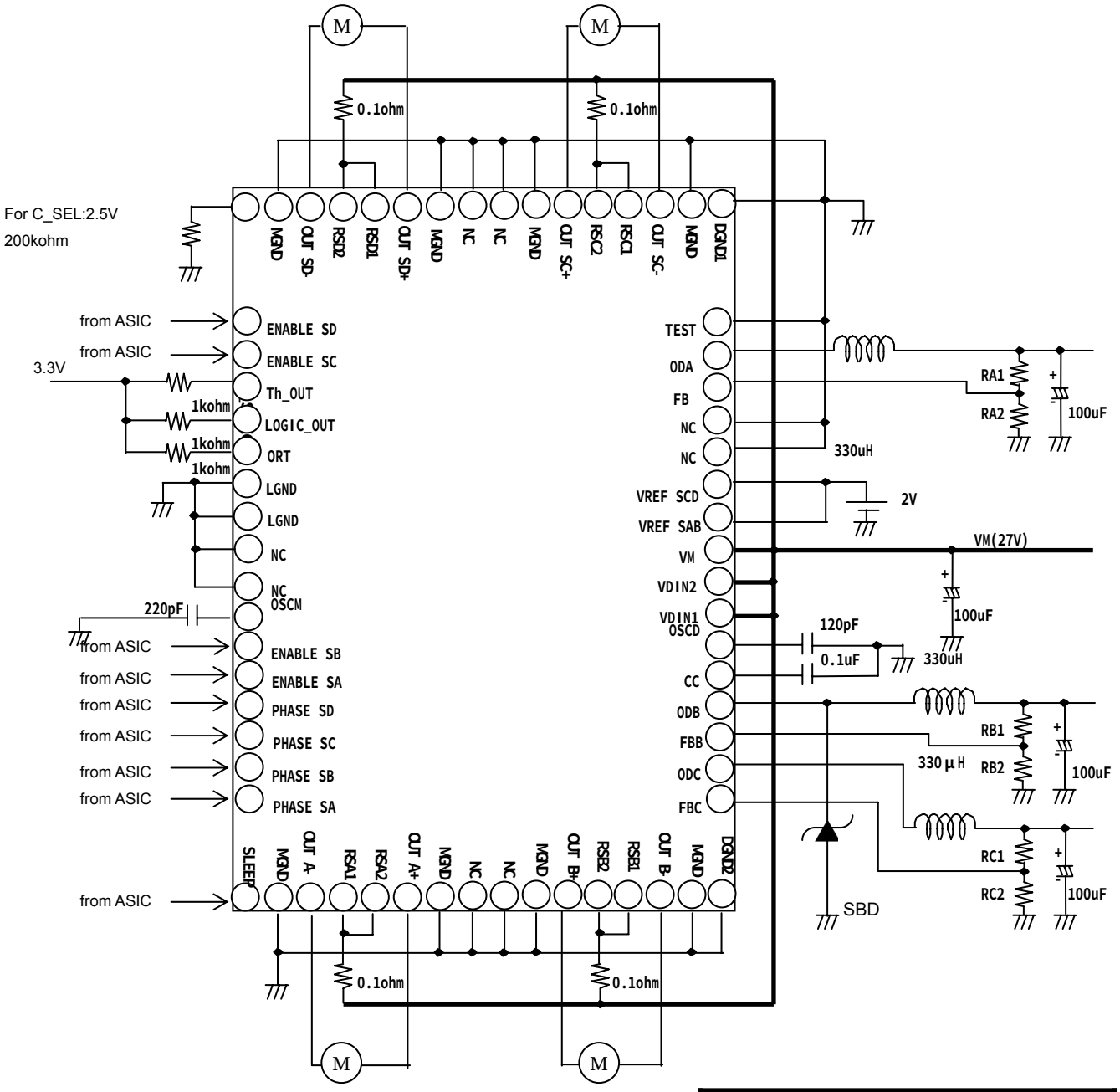
The time between the instant when over current starts flowing through the output stage and the instant when the output stops is as follows:

When dead band time = 4 × fosc_M period

Minimum: 4 × fosc_M period
Maximum: 8 × fosc_M period (+ synchronization time + 1 fosc_M time)

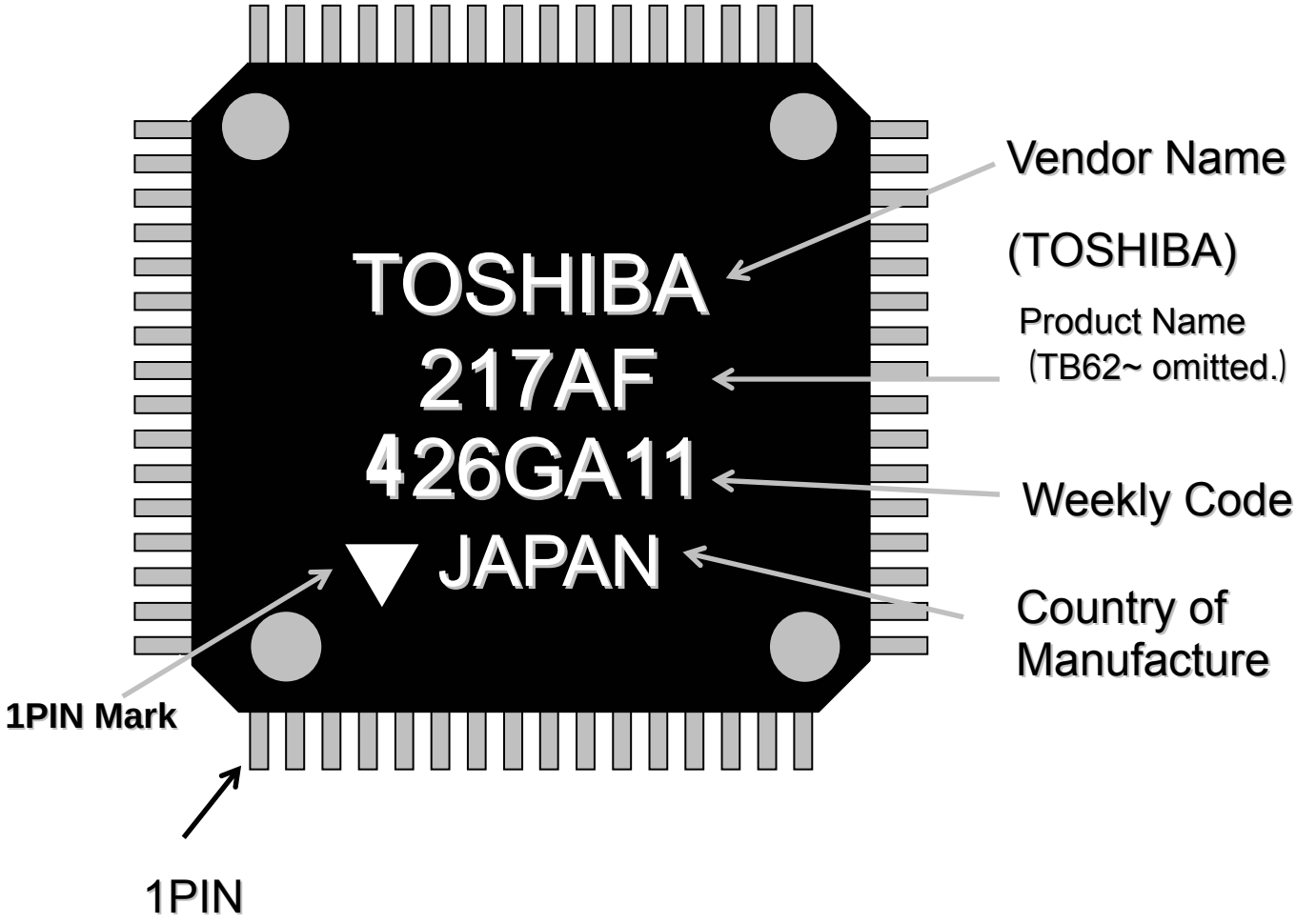
However, the operating time stated above applies when the over current flows ideally. The over current circuit may not work depending on the output control mode and timing.
Therefore, a protection fuse needs to be inserted in the VM power supply.
(The required rating of the fuse varies depending on the conditions under which the IC is used. Therefore, select a rating that will not cause the maximum power dissipation of the IC to be exceeded and that will not pose any problem.)

Application Circuit Example



Output Voltage	RA1/RB1/RC1	RA2/RB2/RC2
1.5V	0ohm	nothing
3.3V	1.2kohm	1.0kohm
5.0V	5.6kohm	2.4kohm

Marking



Lot traceability correspondence

lot code 4 2 6 G A 1 1

Weekly

Manufacture year

1 figure

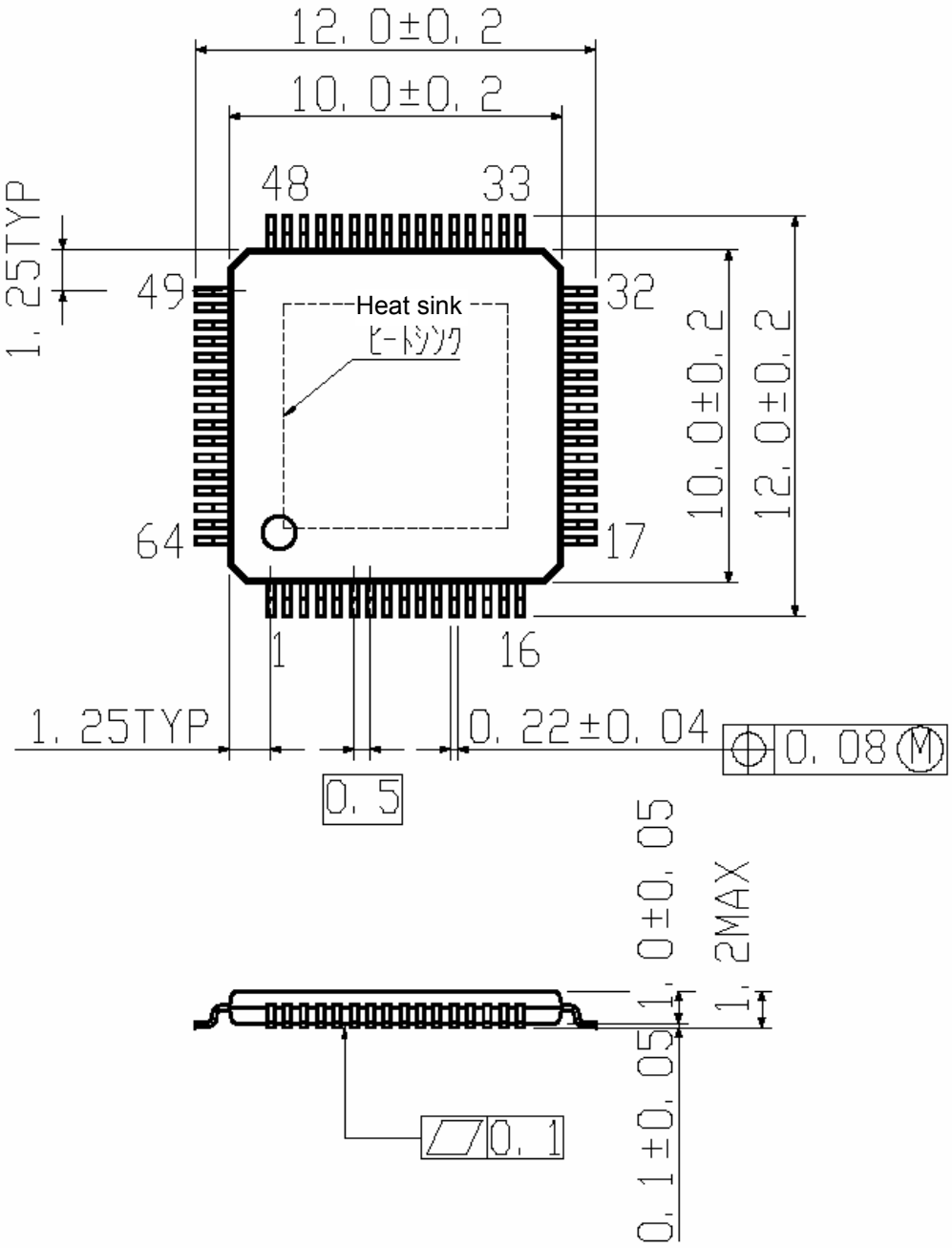
Wafer / Assembly

traceability code

Production factory

G : Toshiba Oita factory

Package Dimensions (THQFP64-P-1010-0.50)



Weight: 0.45 g (typ.)

Note: The heat sink provided on the bottom surface of the package is 5.5 mm × 5.5 mm (tentative).