SONY

CXD2403AR

Timing Generator for Color Liquid Crystal Panel

Description

The CXD2403AR is a timing signal generator for color liquid crystal panel drivers.

Features
- Generates the LCX003, LCX004 and LCX005 drive pulses
- Supports line inversion and field inversion
- AC drive for liquid crystal panel during no signal (NTSC/PAL)
- Generates timing signal of external sample-and-hold circuit
- AFC circuit supporting static and dynamic fluctuations
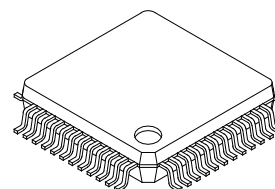- Pulse driver for liquid crystal panel driver (12.0V)

Applications

Color liquid crystal viewfinders

Structure

Silicon gate CMOS IC

48 pin LQFP (Plastic)

Absolute Maximum Ratings (5V system)

$(Ta = +25°C, V_{SS1} = 0V)$
- Supply voltage — V_{CC} — -0.3 to $+7.0$ — V
- Input voltage — V_I — -0.3 to $V_{DD} +0.3$ — V
- Output voltage — V_O — -0.3 to $V_{DD} +0.3$ — V
- Operating temperature — Topr — -20 to $+75$ — °C
- Storage temperature — Tstg — -55 to $+125$ — °C

Absolute Maximum Ratings (12V system)

$(Ta = +25°C, V_{SS3} = 0V)$
- Supply voltage — V_{EE} — -0.3 to $+20.0$ — V
- Output voltage — V_O — -0.3 to $V_{EE} +0.3$ — V
- Operating temperature — Topr — -20 to $+75$ — °C
- Storage temperature — Tstg — -55 to $+125$ — °C
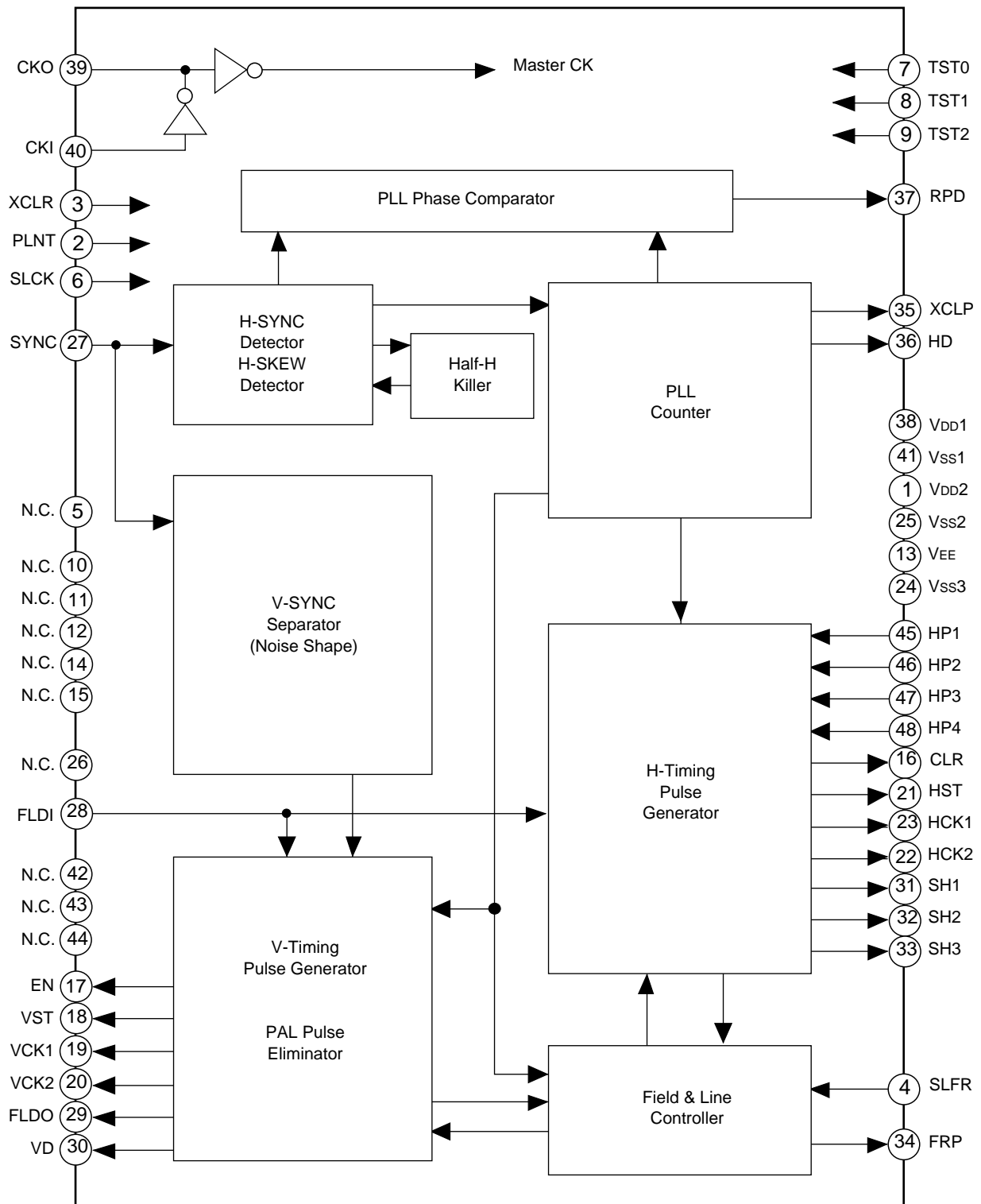
Recommended Operating Conditions (5V system)
- Supply voltage — V_{DD} — 2.7 to 5.5 — V
- Operating temperature — Topr — -20 to $+75$ — °C

Recommended Operating Conditions (12V system)
- Supply voltage — V_{EE} — 11.5 to 12.5 — V
- Operating temperature — Topr — -20 to $+75$ — °C

E94421-TE

Block Diagram

Pin Description   (H: Pull Up, L: Pull Down)

Pin No.	Symbol	I/O	Description	Input Pin for Open Status
1	V$_{DD}$2	I	5V system power supply	
2	PLNT	I	Switches between PAL (High) and NTSC (Low)	L
3	XCLR	I	Reset at 0V	H
4	SLFR	I	Switches between field inversion (High) and line inversion (Low)	L
5	N.C.	—	No connected	—
6	SLCK	I	Switches between LCX003/004 (Low) and LCX005 (High)	L
7	TST0	I	Test	L
8	TST1	I	Test	L
9	TST2	I	Test	L
10	N.C.	—	No connected	—
11	N.C.	—	No connected	—
12	N.C.	—	No connected	—
13	V$_{EE}$	I	12V system power supply	—
14	N.C.	—	No connected	—
15	N.C.	—	No connected	—
16	CLR	O	CLR pulse output (positive polarity)	—
17	EN	O	EN pulse output (negative polarity)	—
18	VST	O	V start pulse output (positive polarity)	—
19	VCK1	O	V clock pulse 1 output (positive polarity)	—
20	VCK2	O	V clock pulse 2 output (positive polarity)	—
21	HST	O	H start pulse output (positive polarity)	—
22	HCK2	O	H clock pulse 2 output (positive polarity)	—
23	HCK1	O	H clock pulse 1 output (positive polarity)	—
24	V$_{SS}$3	I	12V system GND	—
25	V$_{SS}$2	I	5V system GND	—
26	N.C.	—	No connected	—
27	SYNC	I	Composite sync input (positive polarity)	—
28	FLDI	I	Field identification signal input ODD (High)/EVEN (Low)	—
29	FLDO	O	Field identification signal output	—
30	VD	O	VD pulse output (positive polarity)	—
31	SH1	O	Sample-and-hold pulse output (positive polarity)	—
32	SH2	O	Sample-and-hold pulse output (positive polarity)	—
33	SH3	O	Sample-and-hold pulse output (positive polarity)	—
34	FRP	O	AC drive timing pulse output	—
35	XCLP	O	Burst position clamp pulse output (negative polarity)	—
36	HD	O	HD pulse output (positive polarity)	—
37	RPD	O	Phase comparator output	—
38	V$_{DD}$1	I	5V system power supply	—
39	CKO	O	Oscillation cell (output)	—
40	CKI	I	Oscillation cell (input)	—

Pin No.	Symbol	I/O	Description	Input Pin for Open Status
41	VSS1	I	5V system GND	
42	N.C.	—	No connected	—
43	N.C.	—	No connected	—
44	N.C.	—	No connected	—
45	HP1	I	Switches for the horizontal display start position	H
46	HP2	I	Switches for the horizontal display start position	L
47	HP3	I	Switches for the horizontal display start position	L
48	HP4	I	Switches for the horizontal display start position	H

Electrical Characteristics 1

DC Characteristics (VDD = 5.0V ± 10%)

Item	Applicable Pins	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Input voltage	SYNC	VIH		0.7*VDD		5.5	V
		VIL		VSS		0.3*VDD	
Output current	Other than CKO and RPD	IOH	VOH = VDD–0.8V			–2.0	mA
		IOL	VOL = 0.4V	4			
	RPD	IOH	VOH = VDD–0.8V			–2	
		IOL	VOL = 0.4V	2			
	CKO	IOH	VOH = VDD/2	–18		–3.0	
		IOL	VOL = VDD/2	3.0		18	
Input leak current	Normal input pins	II	VIN = VSS or VDD	–2		2	µA
	Pull-up resistor connected	IIL	VIN = VSS	–240		–10	
	Pull-down resistor connected	IIH	VIN = VDD	10		240	
Output leak current	RPD (at high imedance state)	IO2	VIN = VSS or VDD	–40		40	

Item	Applicable Pins	Symbol	Measurement Conditions		Min.	Typ.	Max.	Unit
Output voltage	12V system output pins	VOH	IOUT = –20µA		11.9	12.0	—	V
		VOL	IOUT = 20µA		—	0.0	0.1	
Output current	12V system output pins	IOH	VOH = 11.5V	(VEE= 12V)			–1.0	mA

Item		Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Current consumption	5V system	IDD	Note 1)			25.0	mA
	12V system	IEE	Note 1)			2.0	

Note:
1. Master clock frequency FCKI = 12MHz, input conditions VIH = VDD, VIL = VSS, no output load.

AC Characteristics (VDD = 5.0V ± 10%)

5V System

Item	Applicable Pins	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Clock input cycle	CKI Note 4)	tck		83			ns
High level pulse width		tw (H)		30			
Low level pulse width		tw (L)		30			
Clock rise time		tr (ck)				10	
Clock fall time		tf (ck)				10	
Output rise time	SH1, SH2 SH3	tr	CL = 10pF			20	
Output fall time		tf	CL = 10pF			20	
Output rise delay time	5V system output pins	tpr	CL = 20pF			70	
Output fall delay time		tpf	CL = 20pF			70	

12V System

Item	Applicable Pins	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Output rise time	12V system all Output pins Note 3)	tr	CL = 10pF			50	ns
			CL = 40pF			80	
Output fall time		tf	CL = 10pF			50	
			CL = 40pF			80	
Cross point time difference Note 2)	VCK1, 2 HCK1, 2	Δt	CL = 10pF			15	
		Δt	CL = 40pF			15	
Output rise delay time	12V system all ouput pins Note 3)	tpLH	CL = 10pF			160	
			CL = 40pF			180	
Output fall delay time		tpHL	CL = 10pF			160	
			CL = 40pF			180	
HCK1, SH1 delay time difference	HCK1 SH1	dt1	CL = 40pF (HCK1, HCK2)	80		125	
HCK2, SH2 delay time difference	HCK2 SH1	dt2	CL = 20pF (SH1) Note 5)	90		130	
HCK delay time difference	HCK1 HCK2	tH–tL	CL = 40pF	−30		40	

Notes:
2. Applicable to the relationships between HCK1 and HCK2, and VCK1 and VCK2.
3. 12V system output pins : HST, HCK1, HCK2, VST, VCK1, VCK2, EN, CLR.
4. CKI input voltage conditions : The input signal must have the full swing amplitude.
5. Master clock frequency fCKI=8MHz.

Electrical Characteristics 2

DC Characteristics (V_{DD} = 2.7V to 3.6V)

| Item	Applicable Pins	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Input voltage Note) 4	SYNC	V_{IH}		$0.7*V_{DD}$		5.5	V
		V_{IL}		V_{SS}		$0.3*V_{DD}$	
Output current	Other than CKO	I_{OH}	$V_{OH} = V_{DD}-0.8V$			−1.1	mA
		I_{OL}	$V_{OL} = 0.4V$	1.0			
	CKO	I_{OH}	$V_{OH} = V_{DD}/2$	−8.0		−0.7	
		I_{OL}	$V_{OL} = V_{DD}/2$	0.75		8.0	
Input leak current	Normal input pins	I_I	$V_{IN} = V_{SS}$ or V_{DD}	−2		2	µA
	Pull-up resistor connected	I_{IL}	$V_{IN} = V_{SS}$	−240		−3	
	Pull-down resistor connected	I_{IH}	$V_{IN} = V_{DD}$	5		240	
Output leak current	RPD (at high imedance state)	I_{O2}	$V_{IN} = V_{SS}$ or V_{DD}	−40		40	

Item	Applicable Pins	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Output voltage	12V system output pins	V_{OH}	$I_{OUT} = -20µA$	11.9	12.0	—	V
		V_{OL}	$I_{OUT} = 20µA$	—	0.0	0.1	
Output current	12V system output pins	I_{OH}	$V_{OH} = 11.5V$ ($V_{EE}=$			−1.0	mA
		I_{OL}	$V_{OL} = 0.5V$ 12V)	1.0			

Item		Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Current consumption	5V system	I_{DD}	Note 1)			25.0	mA
	12V system	I_{EE}	Note 1)			2.0	

Notes:
1. Master clock frequency F_{CKI} = 12MHz, input conditions $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$, no output load.
4. CKI input voltage conditions : The input signal must have the full swing amplitude.

AC Characteristics (V$_{DD}$ = 2.7V to 3.6V)

5V System

Item	Applicable Pins	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Clock input cycle	CKI Note 4)	tck		83			ns
High level pulse width		tw (H)		30			
Low level pulse width		tw (L)		30			
Clock rise time		tr (ck)				10	
Clock fall time		tf (ck)				10	
Output rise time	SH1, SH2 SH3	tr	CL = 10pF			30	
Output fall time		tf	CL = 10pF			30	
Output rise delay time	5V system output pins	tpr	CL = 20pF			200	
Output fall delay time		tpf	CL = 20pF			200	

12V System

Item	Applicable Pins	Symbol	Measurement Conditions	Min.	Typ.	Max.	Unit
Output rise time	12V system all Output pins Note 3)	tr	CL = 10pF			50	ns
			CL = 40pF			80	
Output fall time		tf	CL = 10pF			50	
			CL = 40pF			80	
Cross point time difference Note 2)	VCK1, 2 HCK1, 2	Δt	CL = 10pF			15	
		Δt	CL = 40pF			15	
Output rise delay time	12V system all ouput pins Note 3)	tpLH	CL = 10pF			200	
			CL = 40pF			250	
Output fall delay time		tpHL	CL = 10pF			200	
			CL = 40pF			250	
HCK1, SH1 delay time difference	HCK1 SH1	dt1	CL = 40pF (HCK1, HCK2)	80		145	
HCK2, SH2 delay time difference	HCK2 SH1	dt2	CL = 20pF (SH1) Note 5)	90		145	
HCK delay time difference	HCK1 HCK2	tH–tL	CL = 40pF	–30		40	

Notes:
2. Applicable to the relationships between HCK1 and HCK2, and VCK1 and VCK2.
3. 12V system output pins : HST, HCK1, HCK2, VST, VCK1, VCK2, EN, CLR.
4. CKI input voltage conditions : The input signal must have the full swing amplitude.
5. Master clock frequency f$_{CKI}$ = 8MHz.

Timing Definition for 5V System Pins
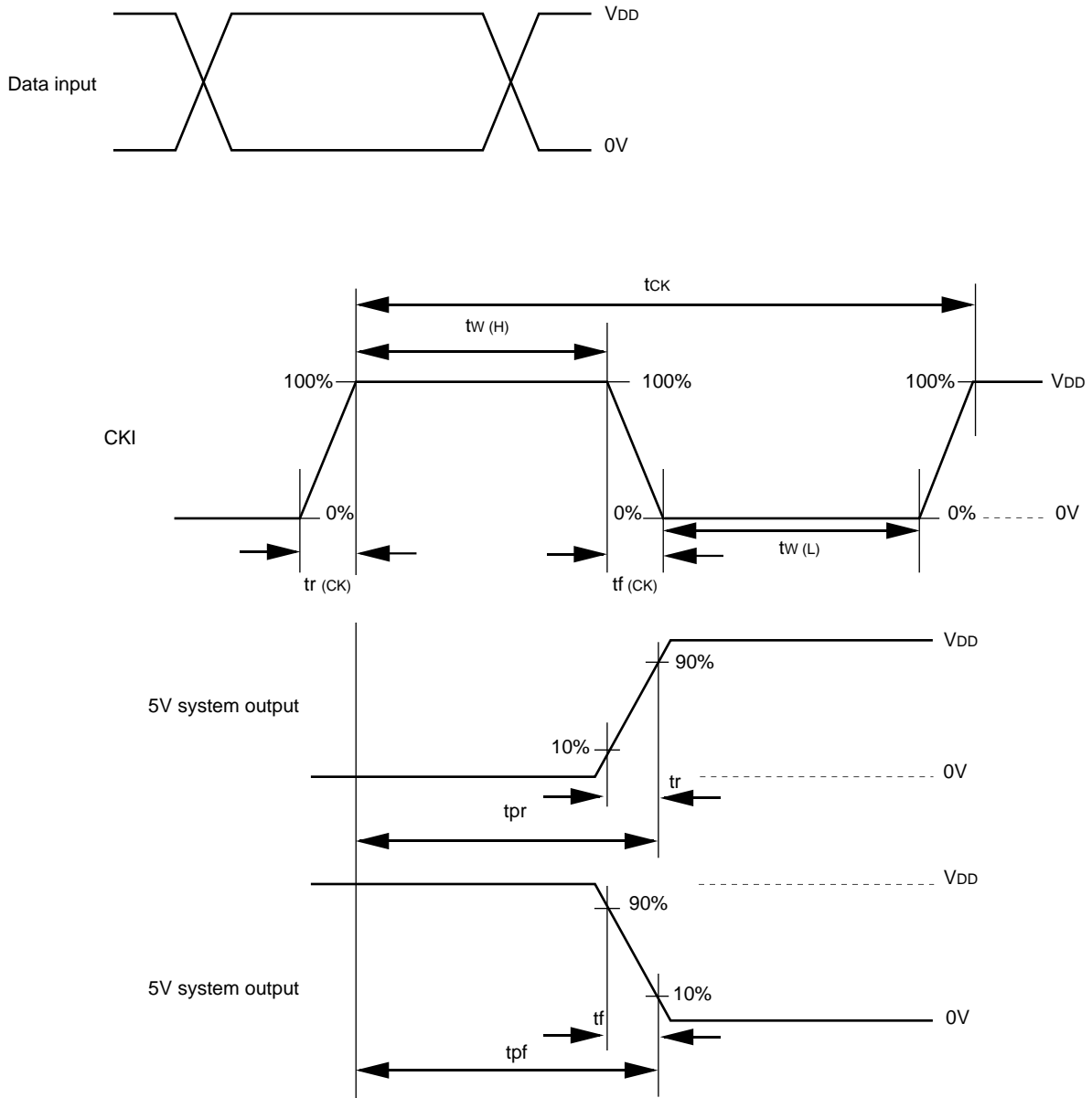
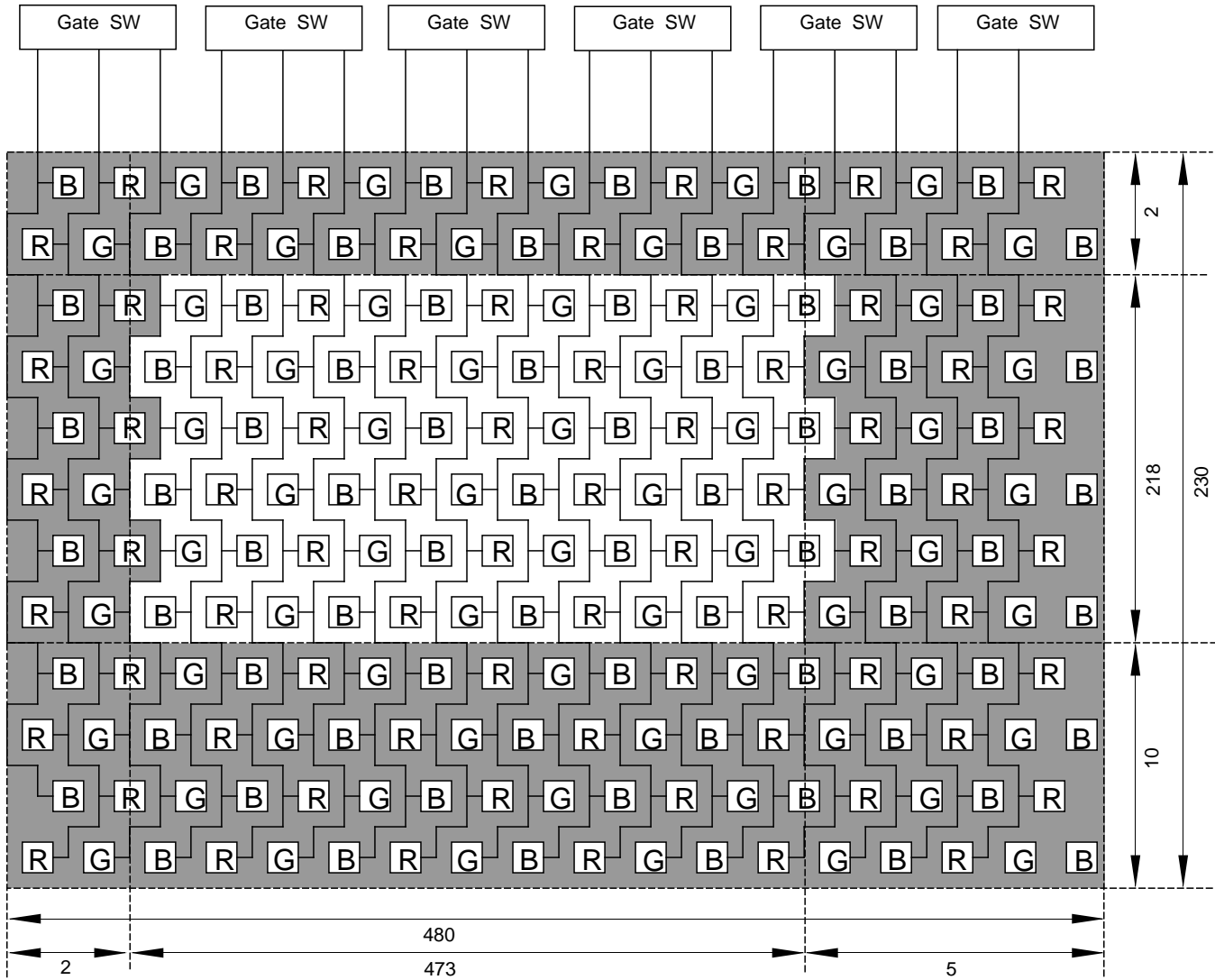## Timing Definition for 12V System Pins
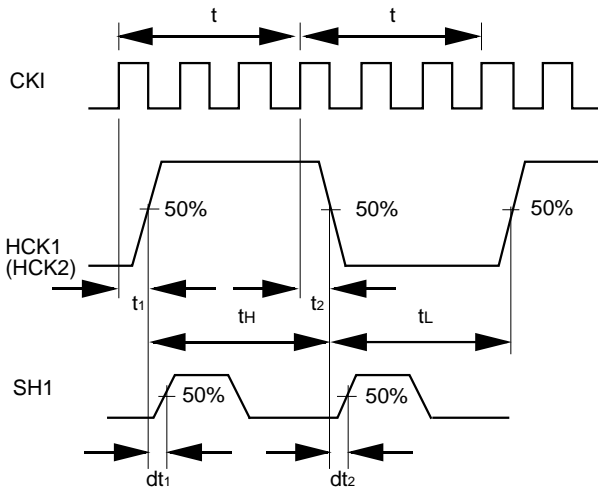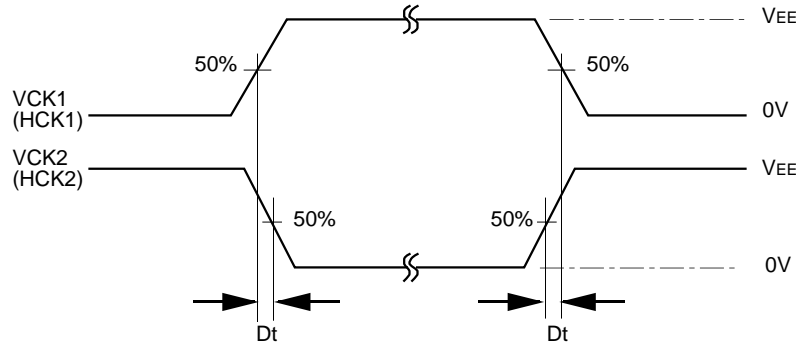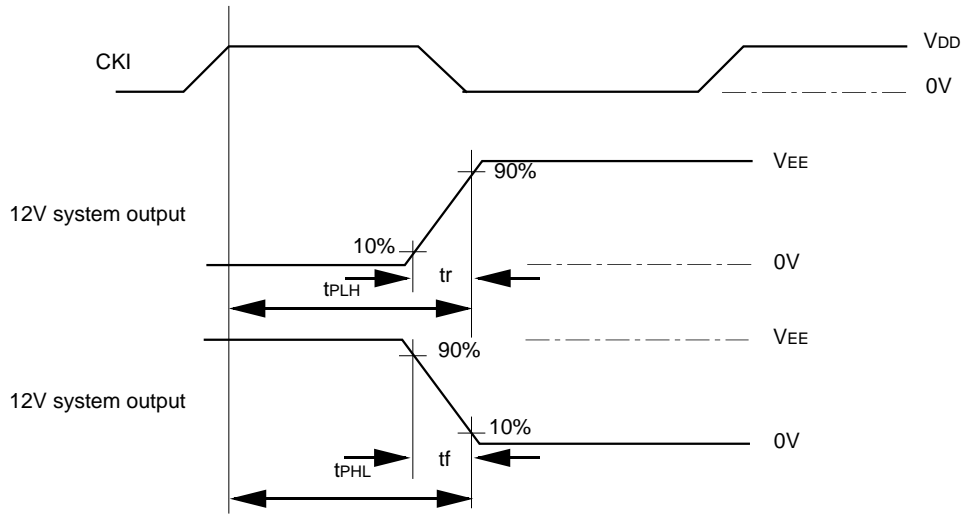
$$t - t_L = 2(t - t_1)$$

$$\left(\begin{array}{l} t_H = t - t_1 + t_2 \\ t_L = t - t_2 + t_1 \\ t_H - t_L = 2(t_2 - t_1) \end{array} \right)$$

Description of Functions

The structure of liquid crystal panel driven by this IC is shown below.

Liquid Crystal Panel Structure

| Gate SW | Gate SW | Gate SW | Gate SW | Gate SW | Gate SW |

LCX003

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┌─────────────────────────────────────────────┐
│                Basic Specifications           │
│                                               │
│  Total number of horizontal pixels  (A line) :   479H   │
│                                     (B line) :   480H   │
│  Number of horizontal display pixels (A line) :   473H   │
│                                     (B line) :   473H   │
│  Total number of vertical pixels             :   230H   │
│  Number of vertical display pixels           :   218H   │
│                                               │
│  Total number of pixels              :  110285 │
│  Number of display pixels            :  103114 │
└─────────────────────────────────────────────┘
```

Liquid Crystal Panel Structure

| Gate SW | Gate SW | Gate SW | Gate SW | Gate SW | Gate SW |
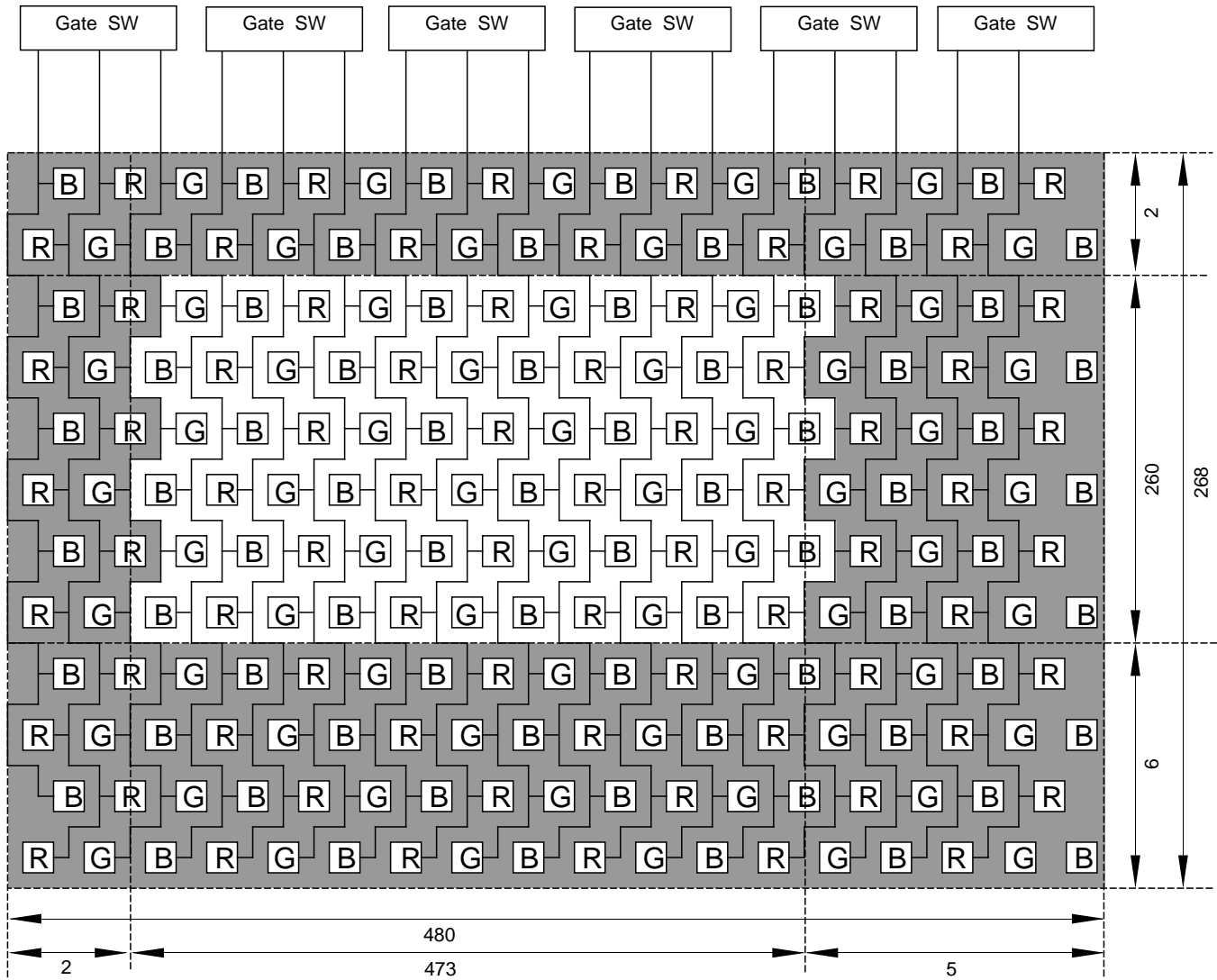
LCX004

```
Basic Specifications

Total number of horizontal pixels        (A line)  :    479H
                                          (B line)  :    480H
Number of horizontal display pixels       (A line)  :    473H
                                          (B line)  :    473H
Total number of vertical pixels                     :    268H
Number of vertical display pixels                   :    260H

Total number of pixels                              :    128506
Number of display pixels                            :    122980
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Liquid Crystal Panel Structure
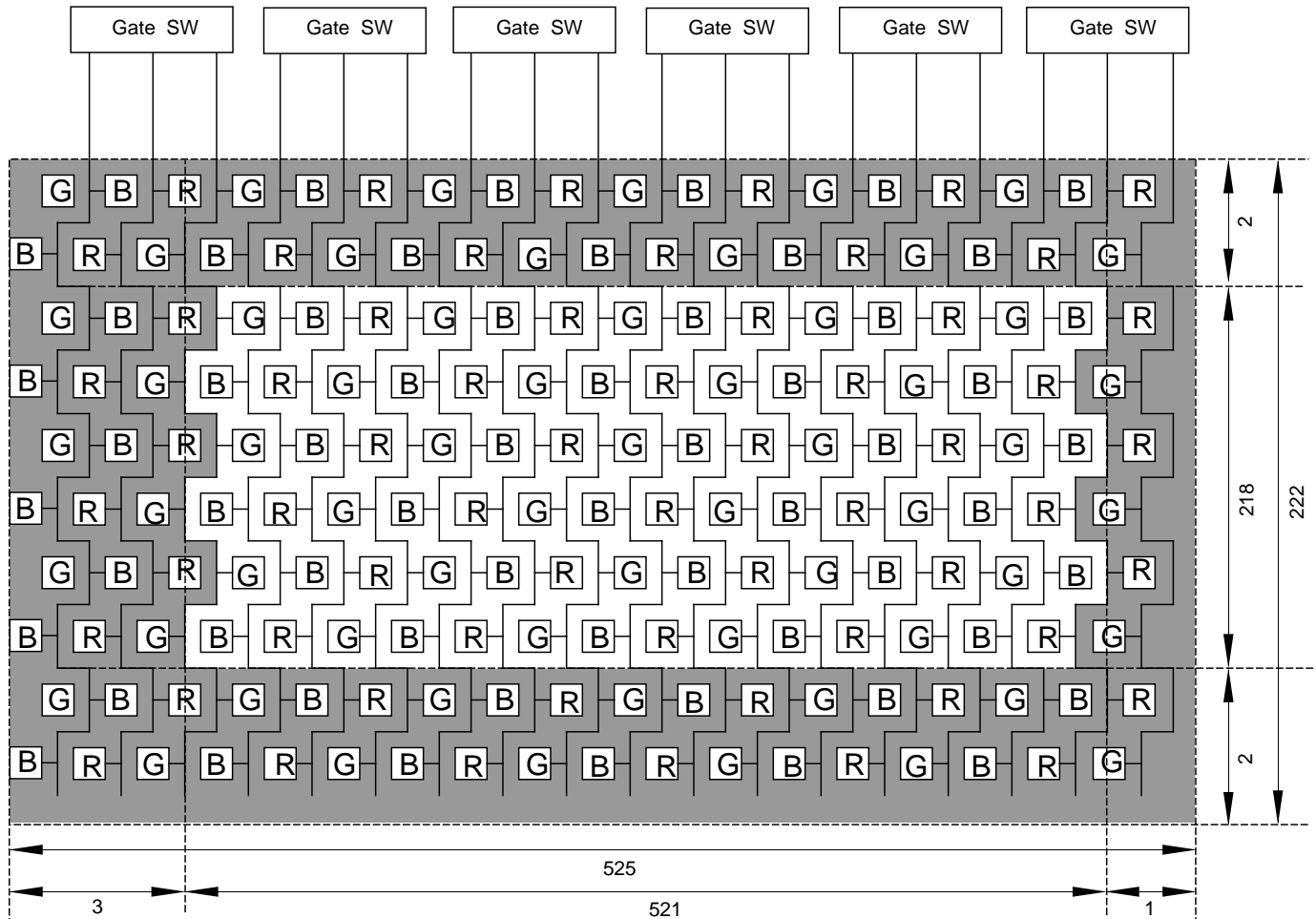
LCX005

```
                      Basic Specifications

Total number of horizontal pixels    :       525H
Number of horizontal display pixels :       521H


Total number of vertical pixels      :       222H
Number of vertical display pixels    :       218H


Total number of pixels               :       116550
Number of display pixels             :       113578
```

Horizontal Direction Output Pulse

The picture display timing of horizontal direction is as follows.

The horizontal start position is offset by two clocks in 16 different ways with the HP1 to 4 pins.

Effective Pixel Display Timing (for the LCX003)
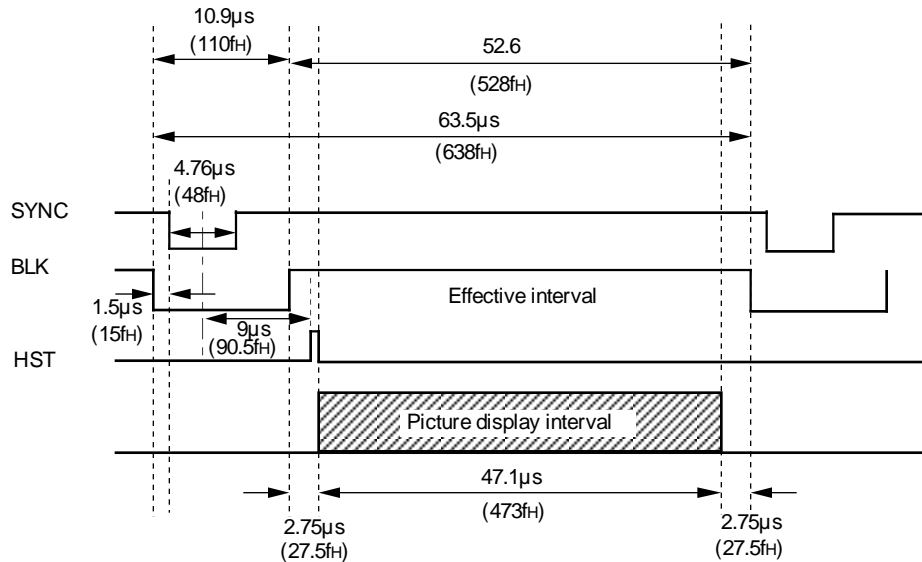
Horizontal Start Position Concept

Horizontal scan interval
$$63.5\mu s = 638f_H$$

Blanking and SYNC
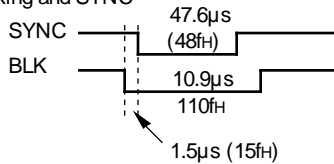
Picture display interval
$$47.1\mu s = 473f_H$$
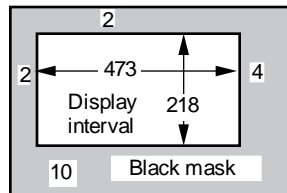
Interval from sync signal to picture display

Picture display starts $(528–473)/2 = 27.5f_H$ later from the end of BLK. Therefore, picture display starts $11 – 15 + 27.5 = 122.5f_H$ later.
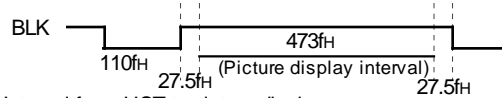
Interval from HST to picture display
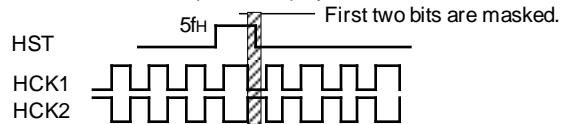
Therefore, the interval between HST and display start is 6 clocks.

Interval from the center of sync signal to HST.

Add time delayed four bits of sync separation circuit.
$110-15-26+27.5-6-4=90.5f_H$ $(9.0\mu s)\mu s$

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Variable Range from the Center of Sync Signal to Hst Rise Timing

HP4	HP3	HP2	HP1	
0	0	0	0	108CLK (10.7μs)
0	0	0	1	106CLK
0	0	1	0	104CLK
0	0	1	1	102CLK
0	1	0	0	100CLK
0	1	0	1	98CLK
0	1	1	0	96CLK
0	1	1	1	94CLK (9.4μs)
1	0	0	0	92CLK
1	0	0	1	90CLK
1	0	1	0	88CLK
1	0	1	1	86CLK
1	1	0	0	84CLK
1	1	0	1	82CLK
1	1	1	0	80CLK
1	1	1	1	78CLK (7.8μs)

HP1 to HP4 pins can be used to vary the interval from the center of sync signal to HST rise as shown in the left table.

Internal preset: 1001 (90CLK)
NTSC (typ.):   1001 (90CLK)
PAL (typ.):   1000 (92CLK)

Liquid Crystal Panel Driving Pulse Generation

HST, HCK1, HCK2, VST, VCK1, and VCK2 (EN, CLR in LCX005 mode only) are generated for the liquid crystal panel driver.

External Sample-and-Hold Pulse Generation

Timing pulses of external sample-and-hold circuit SH1, SH2, and SH3 are generated.

AC Driving Pulse Generation

FRP is output for liquid crystal AC driving. Field inverts when F/H input pin is High and line inverts when

Low. Polarity is not specified for each field. The point is changed from VCK1 and VCK2 pulse change points after 1 clock.

HD-Clamp Pulse Generation

HD pulse is output during horizontal BLK in order to drive the backlight (fluorescent tube). Even during no signal, raster screen with no screen noise can be created synchronizing to the free running frequency. XCLP is output for BF timing clamp pulse.
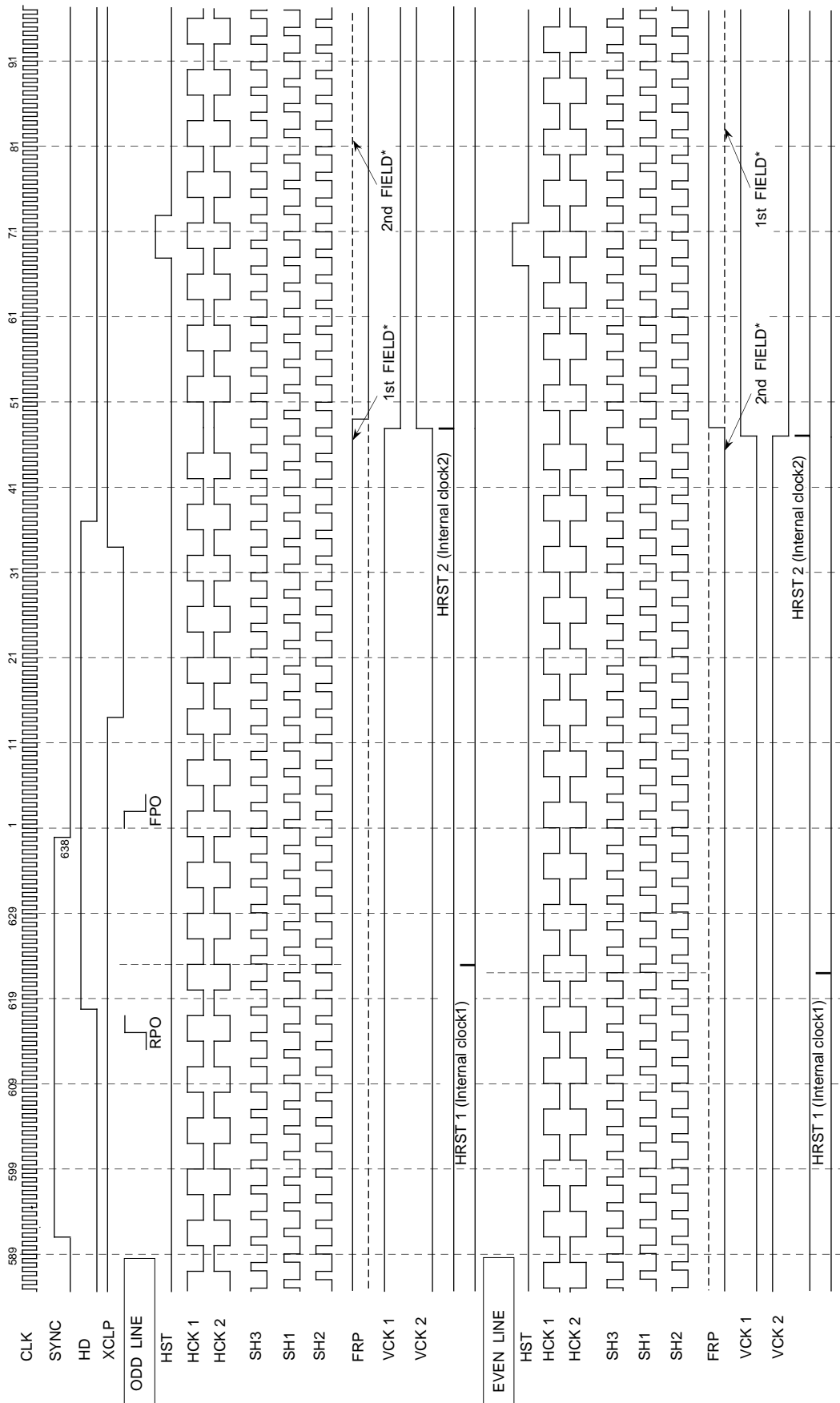
Pulse Timing Chart (for the LCX003)
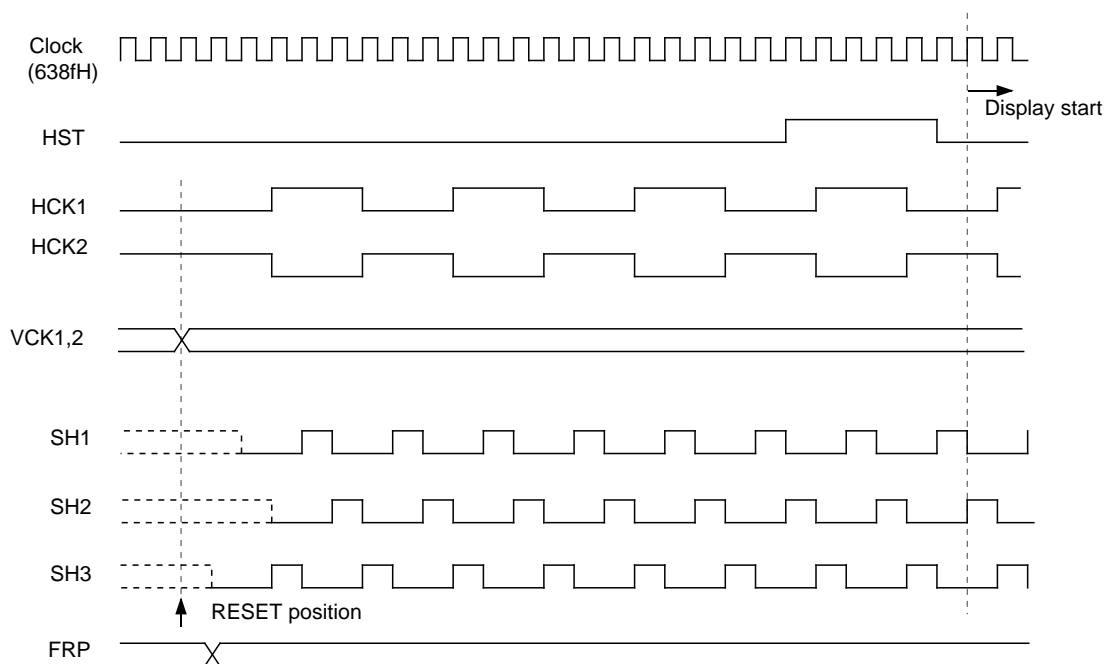
* In accordance with the layout of picture elements on LCD panel, timings between the adjacent lines and fields are offset accordingly.

      1.5 bit offset pulse   → HST, HCK1, HCK2, SH1, SH2, SH3, CLR

      1 bit offset pulse   → VCK1,VCK2, FRP, EN

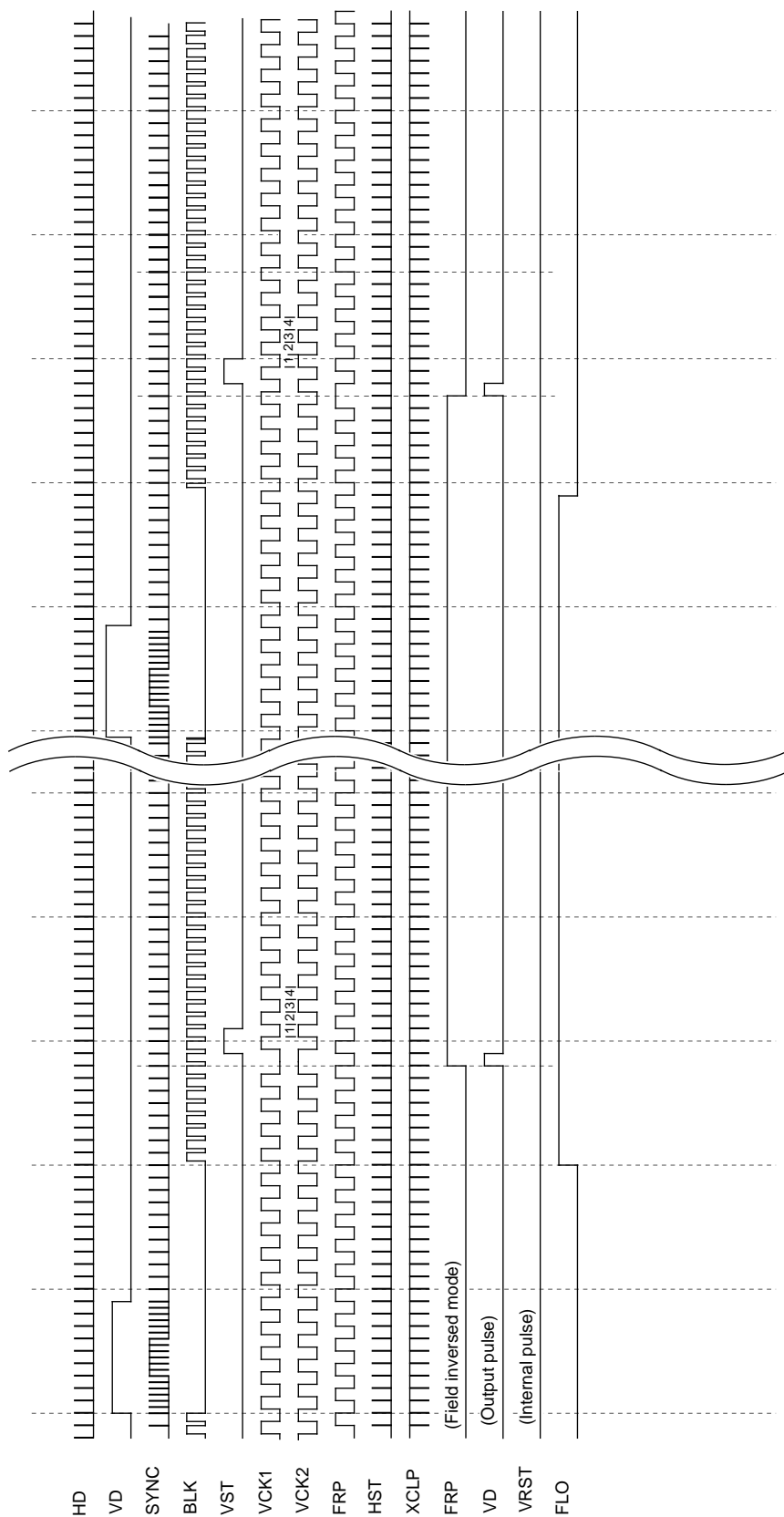**LCX003/004 Horizontal Direction Timing Chart — NTSC, PAL (HPOS-1001)**

Notes) Signals for the timing interval from input SYNC changes with HST according to horizontal start position settings (HP1 to HP4) :
HCK1, HCK2, SH1, SH2, SH3, FRP, VCK1, VCK2
Constant signals regardless of the horizontal start position settings (HP1 to HP4) : SYNC, HD, XCLP

*FRP polarity is not specified for each field.

LCX003 Vertical Direction Timing Chart — NTSC

The signals shown (top to bottom): HD, VD, SYNC, BLK, VST, VCK1, VCK2, FRP, HST, XCLP, FRP (Field inversed mode), VD (Output pulse), VRST (Internal pulse), FLO

Note) The second row of the timing chart 'VD' is a pulse indicated as a reference and is not a pulse output from pins.

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LCX004 Vertical Direction Timing Chart — PAL
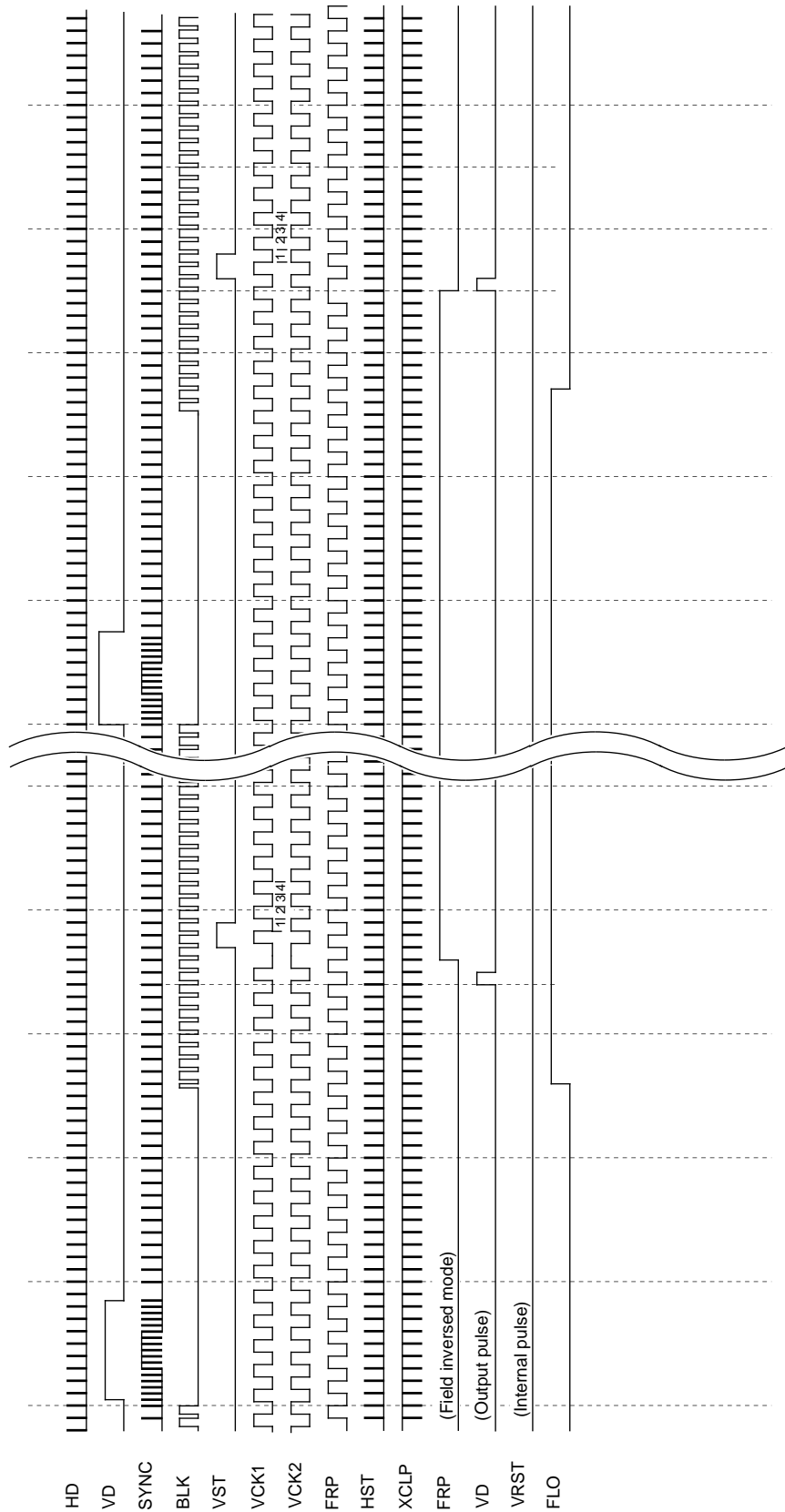
HD, VD, SYNC, BLK, VST, VCK1, VCK2, FRP, HST, XCLP, FRP (Field inversed mode), VD (Output pulse), VRST (Internal pulse), FLO

Note) The second row of the timing chart 'VD' is a pulse indicated as a reference and is not a pulse output from pins.

LCX005 Holizontal Direction Timing Chart — NTSC, PAL (HP=1001)
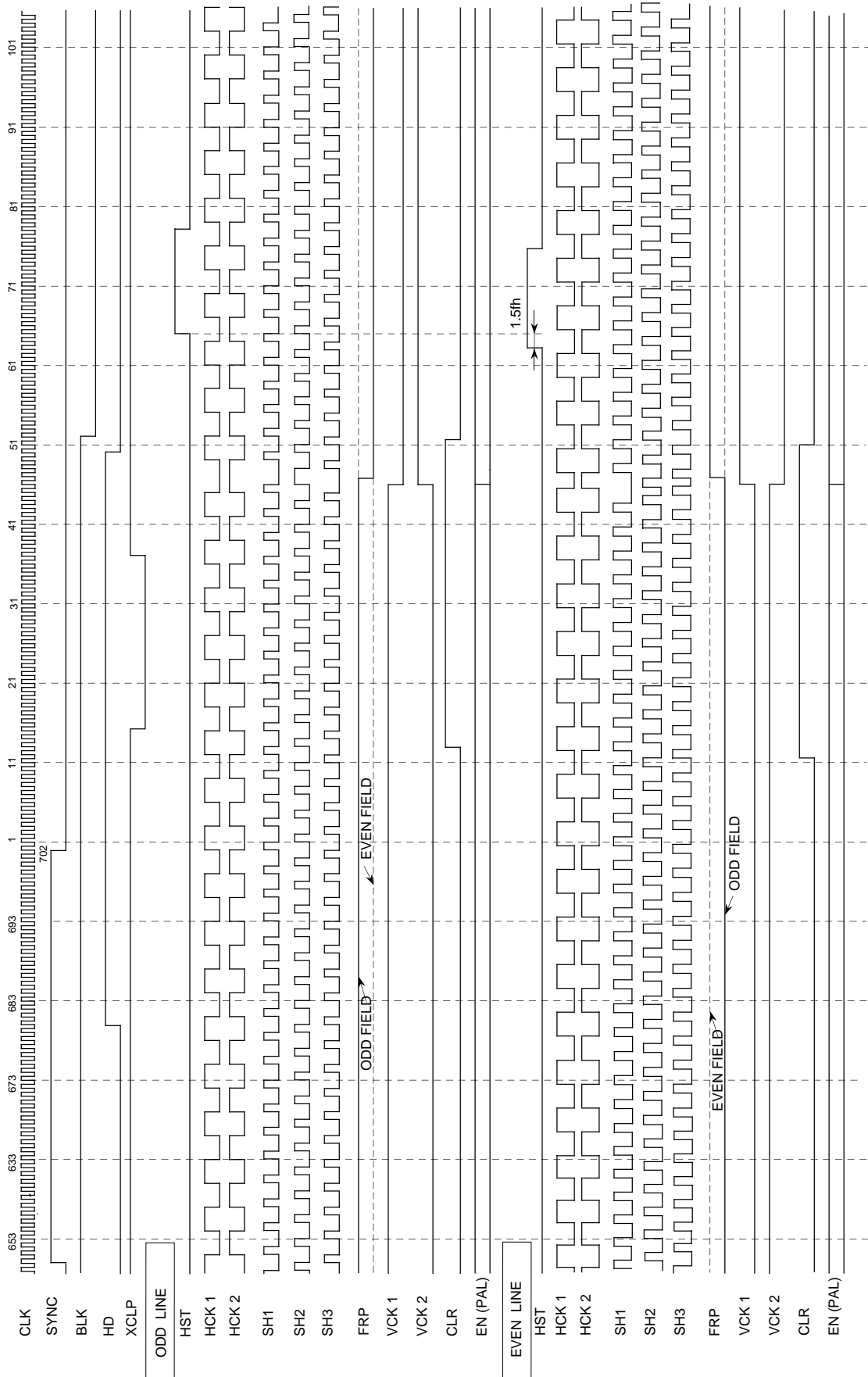
LCX005 Vertical Direction Timing Chart — NTSC
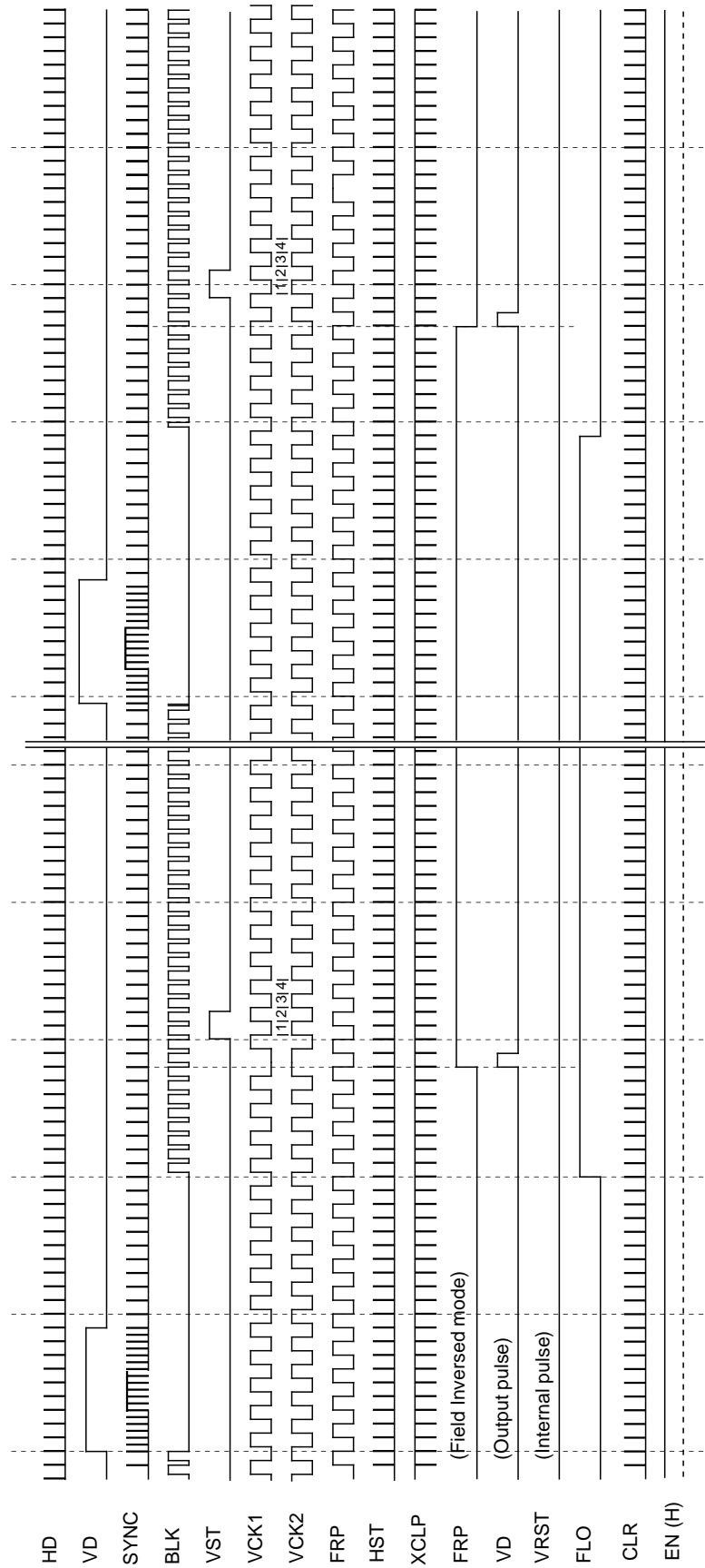
Note) The second row of the timing chart 'VD' is a pulse indicated as a reference and is not a pulse output from pins.

LCX005 Vertical Direction Timing Chart — PAL
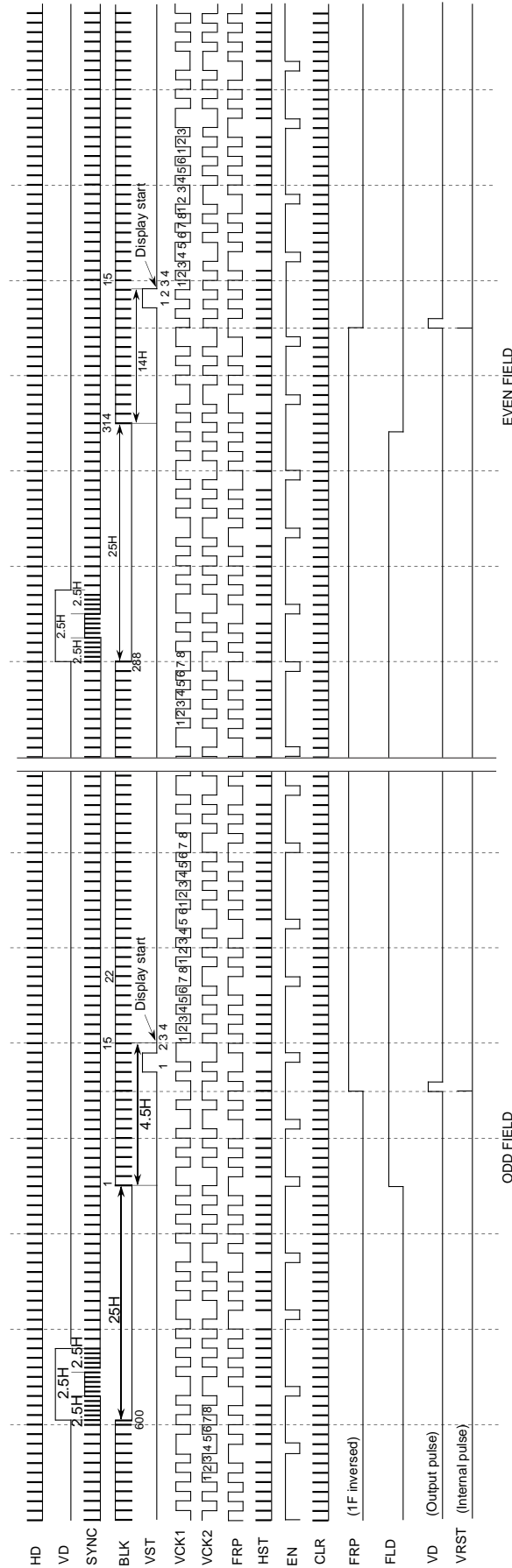
ODD FIELD

EVEN FIELD

Note) The second row of the timing chart 'VD' is a pulse indicated as a reference and is not a pulse output from pins.

Driving for No Signal

HST, HCK1, HCK2, FRP, VCK1, VCK2, XCLP, HD, VD, and VST are made to run free so that the liquid crystal panel is AC driven even when there is no composite sync from the SYNC pin.

The PLL counter is made to run free because the HSYNC separation circuit stops. In addition, the auxiliary V counter is used to create the reference pulse for generating VD and VST because the VSYNC separation circuit is also stopped.

The period of the V counter is 269H for NTSC and 321H for PAL, and if there is no VSYNC during 269H/321H, it is assumed to be a no signal state.

The RPD pin is kept at high impedance so that the AFC circuit does not cause phase errors by phase comparison.

AFC Circuit (638/702 fh clock generation)

A fully synchronized AFC circuit is built in. PLL error detection signal is generated at the following timing.
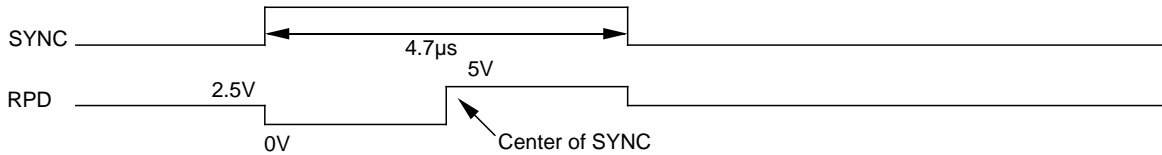
The phase comparison output of the entire bottom of SYNC and the internal H counter becomes RPD. RPD output is converted to DC error with the lag-lead filter. Then the outputs change the vari-cap capacitance and the oscillating frequency is stabilized at 638 fh in LCX003/1004 or 702 fh in LCX005.

Example of PLL Related Peripheral Circuit
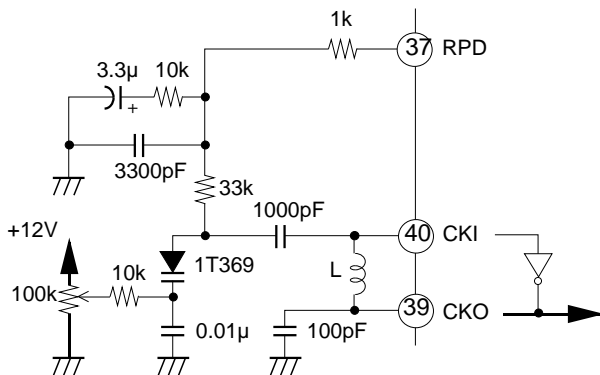
L value
  LCX003/004 → 8.2μ
  LCX005   → 6.8μ

*The parameters of the elements are reference.

Parts : Vari-cap
1T369 (Sony), MA365 (Matsushita)

Adjustment Method

1. Adjust the voltage for vari-cap with the variable resistor connected to 12V power supply while checking HSYNC and RPD waveforms with an oscilloscope.

Concretely, adjust so that the RPD rise is at the center of HSYNC.

2. When PLL is still not locked, change the L of the LC oscillations.

HSYNC Separation

HSYNC is separated from the composite sync input. Noise is eliminated with the counter and equivalent pulse is eliminated with the half H killer.

HSYNC jumping detection and address management when jumping occurs frequently (matching the number of H in a field) are also performed.
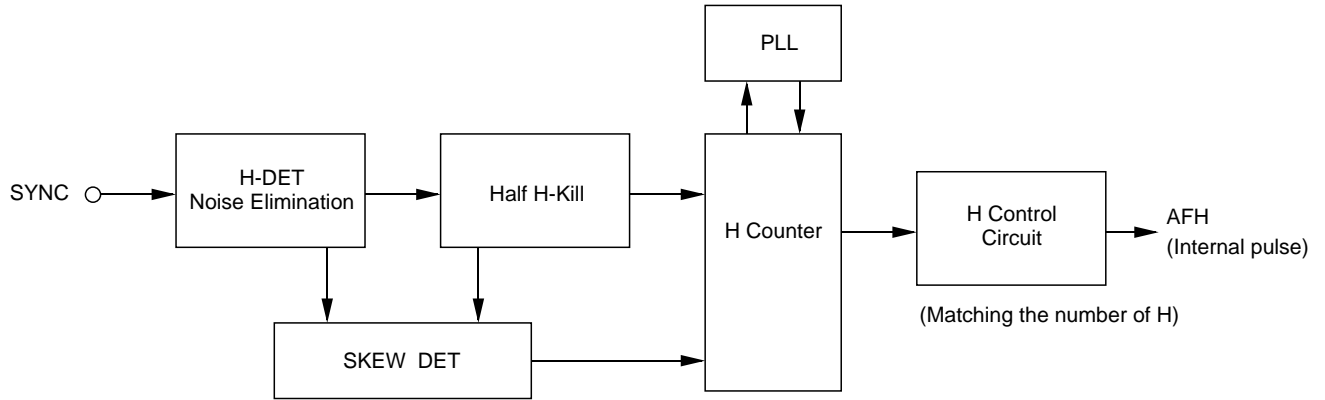

V. SYNC Separation
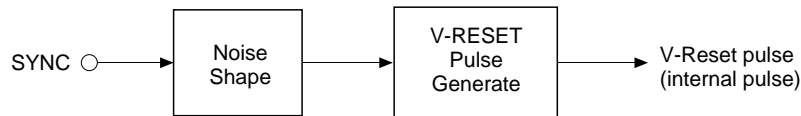
V-SYNC Separation Circuit

V. sync is separated from the composite sync input connected to SYNC connector. The serration pulses are removed as noise. When considerable pulse width is detected, the V reset pulse is output to notify V sync input and to synchronize timing of output signals. When a V sync having different pulse width from normal one is input, it can be separated when the width of serration pulse is narrower than 2~3 µsec or less which is positioned right after the V sync having 0.5H width during A~F period.
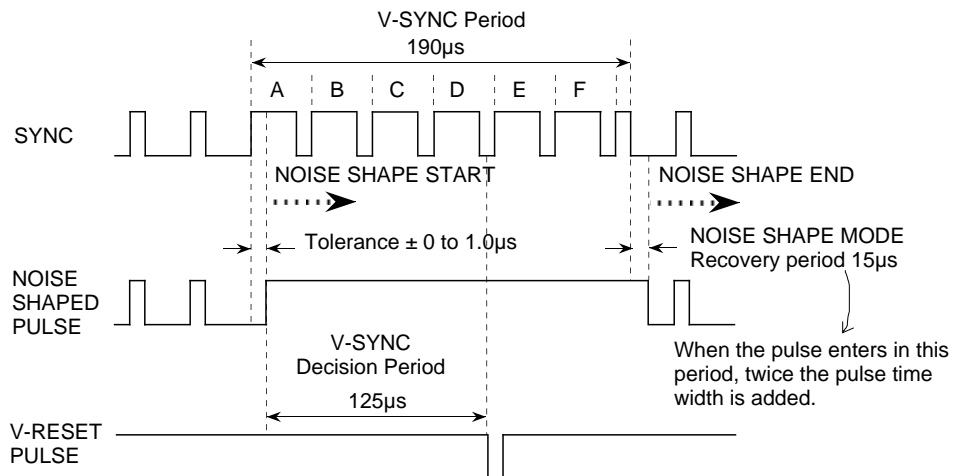
V-SYNC Input Time Axis Specification

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Application Circuit
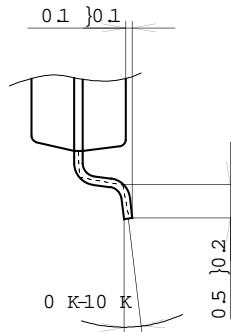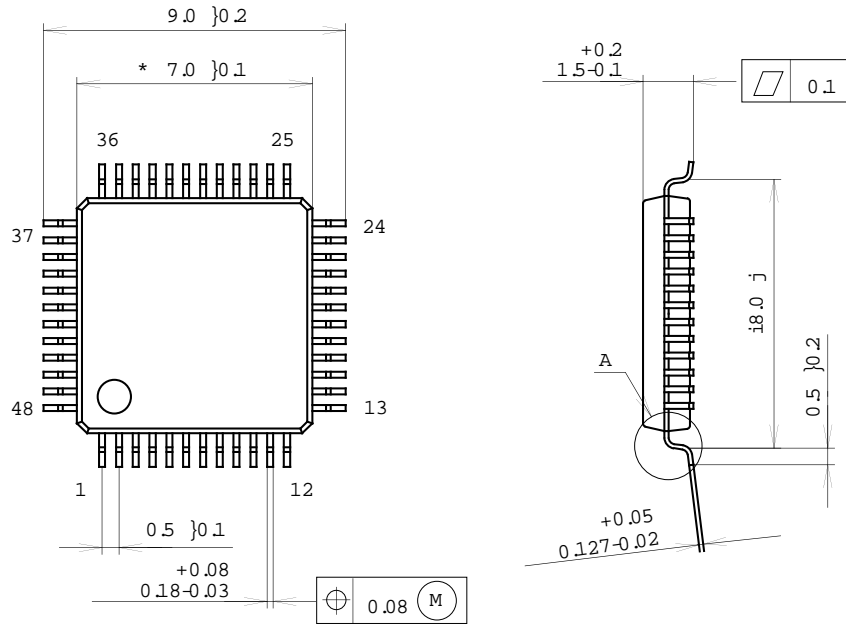
(for driving the liquid crystal panel LCX003)
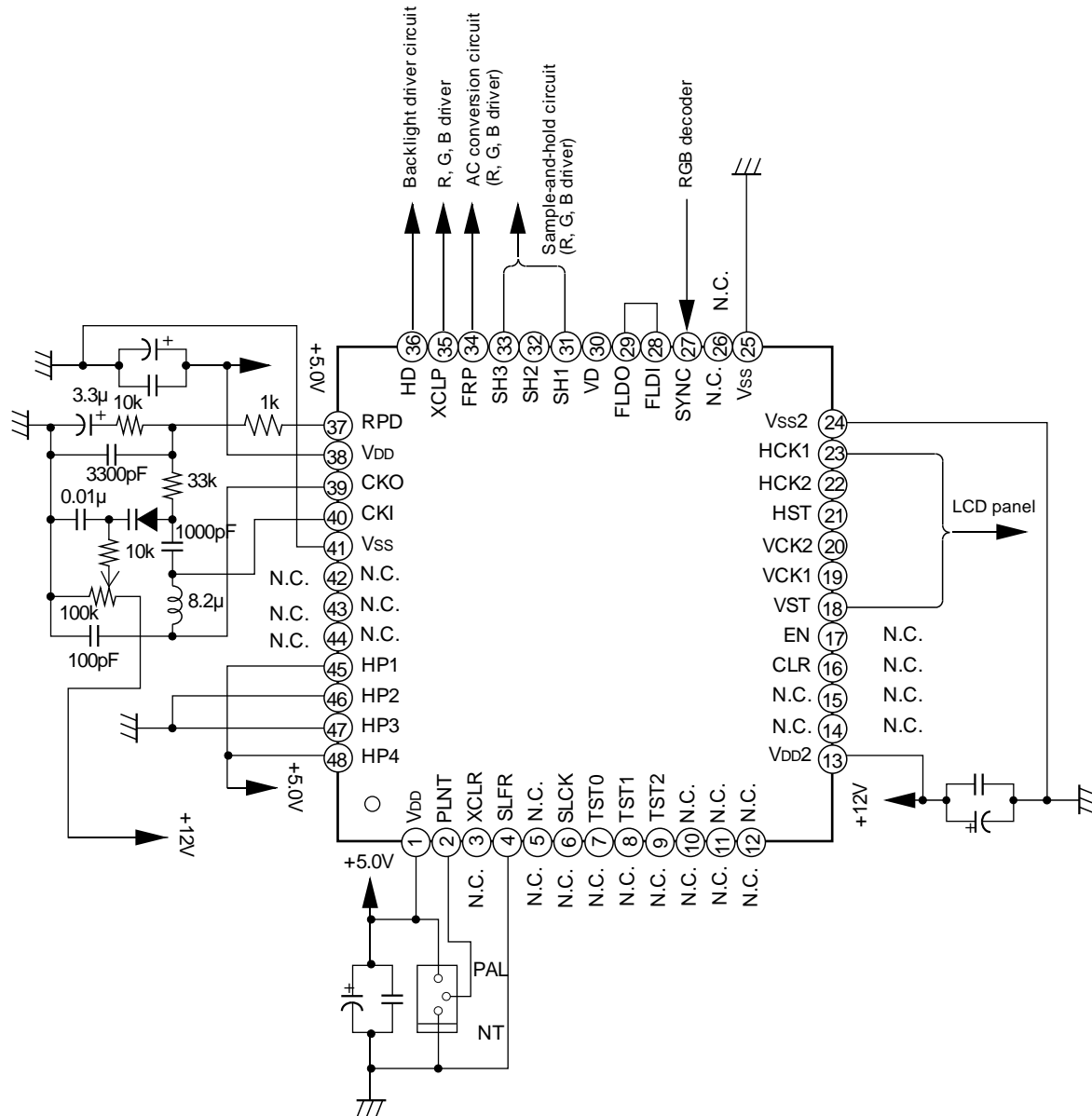
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party and other right due to same.

Package Outline   Unit : mm

48PIN LQFP (PLASTIC)

NOTE Dimension "g" does not include mold protrusion.

DETAIL A

SONY CODE	LQFP-48P-L121
EIAJ CODE	LQFP048-P-0707-AX
JEDEC CODE	—

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.2