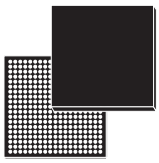
STA2062

Cartesio™
Infotainment application processor with embedded GPS

Data Brief

Features

- High performance ARM926 MCU (up to 333MHz)
- MCU memory organization
  - Cache: 16KByte instruction, 16KByte data
  - 8KByte instruction TCM (tightly coupled memory)
  - 8KByte data TCM
  - 32KByte embedded ROM for boot
  - Two banks of 64KByte embedded SRAM
  - 512Byte embedded SRAM for back-up
  - 4GByte total linear address space
  - Memory extension through:
    Flexible static memory controller-FSMC (NOR/NAND Flash, CF/CF+, ROM, SRAM support)
    Mobile DDR/SDRAM controller:
    16bit data @166MHz, 2 Chip Select, 512Kbit each
- Interrupt
  - 64-channel interrupt controller (VIC)
  - 16-vectorized interrupts with 16 programmable priority Level
- DMA
  - Two 8-channel double port system DMA controllers
  - 32 DMA request for each controller
  - Two external DMA requests are supported
- 32 channel high performance GPS correlation embedded subsystem
- Eight 32-bit free running timers/counters
- Four 16-bit extended function timer (EFT) with input capture/output compare and PWM
- Real time clock (RTC)
- Pulse width light modulator (PWL)
- 32-bit watchdog timer
- Four autobaud UART with 64X8 transmit and 64x12 receive FIFO with DMA and hardware flow control
- One IrDA(SIR/MIR/FIR) interface
- Three I^2C multi-master/slave interfaces
- Two synchronous serial port (SSP) with 32x32 separate transmit and receive FIFO with Motorola-SPI, National-MicroWire and Texas-SSI support modes



LFBGA361 (16x16x1.4mm)

- Four multichannel serial ports (MSP) with 32x8 separate transmit and receive FIFO
- Color LCD controller for STN,TFT or HR-TFT panels
- USB 2.0 OTG high speed dual role controller (ULPI interface)
- USB full speed dual role controller with integrated 1.1 physical layer transceiver
- Two secure-digital multimedia memory card Interface (SD/SDIO/MMC) up to 8 bit data
- SPDIF input interface
- C3 hardware Reed-Solomon decoder
- Hardware sample rate converter (SaRaC)
- Two controller area network (CAN)
- Four 32-bit GPIO ports
- JTAG based in-circuit emulator (ICE) with embedded medium trace module
- Typical working condition: V_{dd}: 1.2 ±10%V, V_{IO}: 1.8V
- Overdrive: V_{dd}: 1.4 ±5%V, V_{IO}: 1.8 ±10%V, 2.5 ±10%V
- Bus frequency: 166 MHz (overdrive)
- Bus/DDR frequency: 166 MHz
- HCMOS 0.90µm process
- Package:
  - LFBGA16x16x1.4mm (19x19balls)
  - 0.8mm ball pitch, (0.4mm ball)
  - Full array
- Ambient temperature range: -40 / +85°C

Table 1. Device summary

Order code	Package	Packing
STA2062	LFBGA361	Tray

For further information contact your local STMicroelectronics sales office. www.st.com

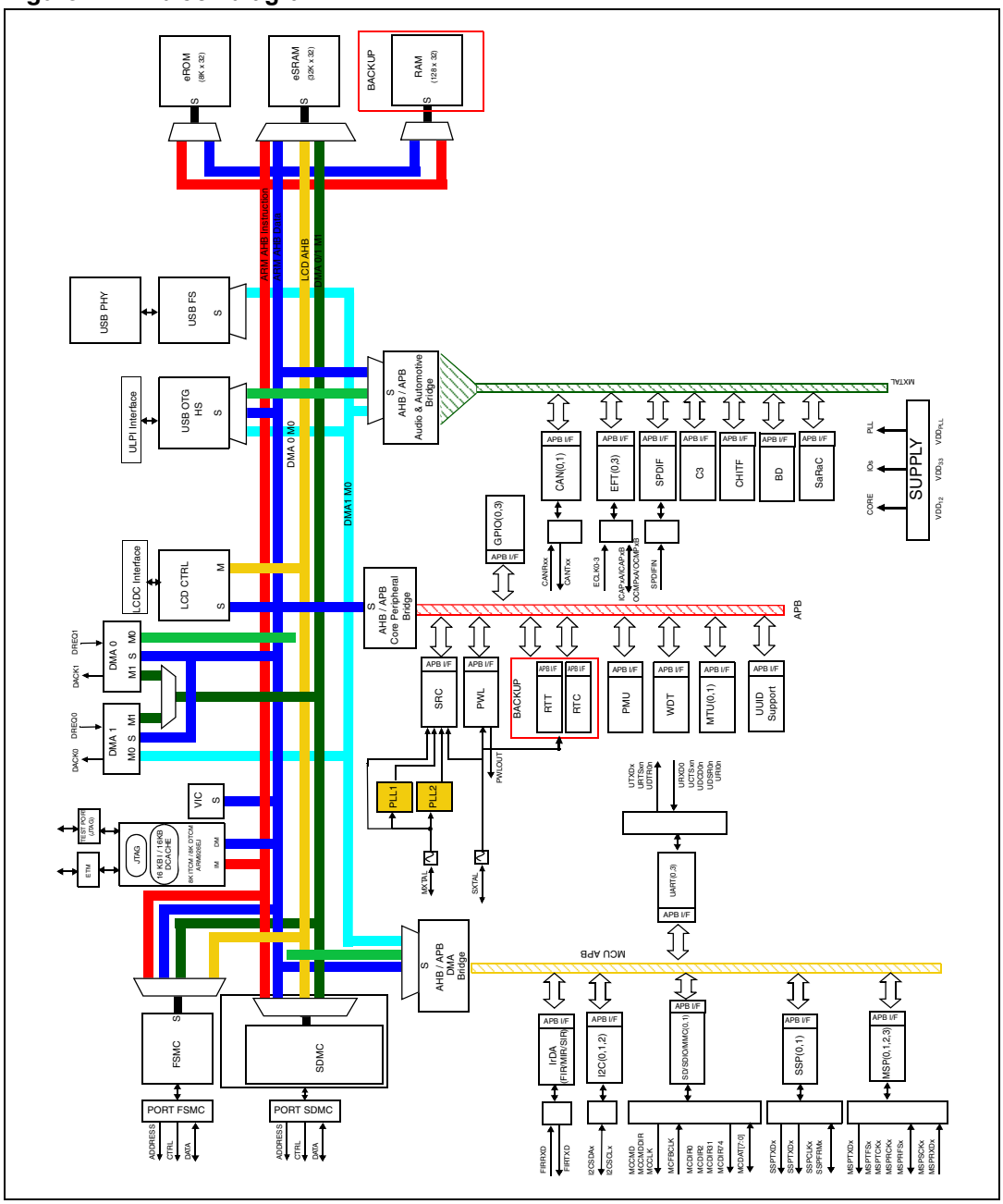
1 Description

The STA2062 is an highly integrated SOC application processor combining host capability with embedded GPS.

STA2062 targets in vehicle and mobile navigation (PND), telematics, advance audio and connectivity systems.

Figure 1: block diagram gives an overview of the complete processor, showing how the ARM926 microcontroller and its peripherals are interfaced.

Figure 1. block diagram



2 Package information

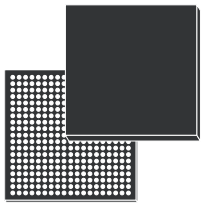
In order to meet environmental requirements, ST offers this device in ECOPACK® packages. This package has a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 2. LFBGA361 (16x16x1.4mm) mechanical data & package dimensions

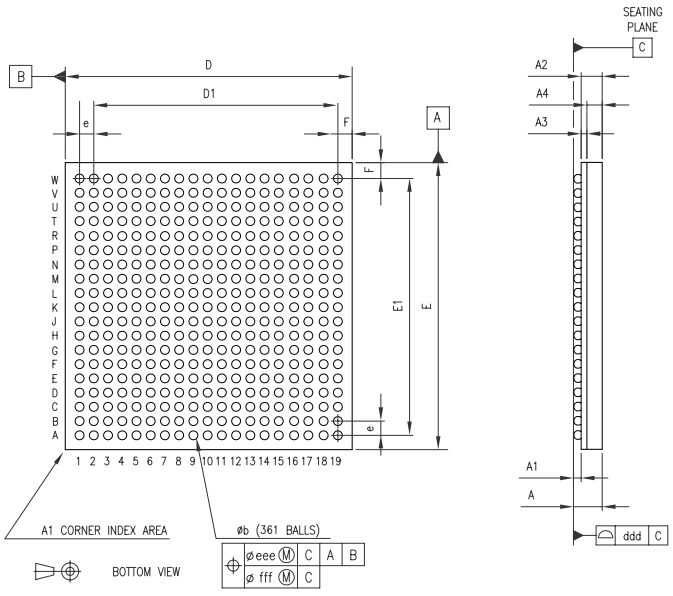
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.400			0.0551
A1	0.210			0.0082		
A2		0.985			0.0387	
A3		0.200			0.0079	
A4			0.800			0.0315
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	15.850	16.000	16.150	0.6240	0.6299	0.6358
D1		14.400			0.5669	
E	15.850	16.000	16.150	0.6240	0.6299	0.6358
E1		14.400			0.5669	
e		0.800			0.0315	
F		0.800			0.0315	
ddd			0.100			0.0039
eee			0.150			0.0059
fff			0.080			0.0031

OUTLINE AND MECHANICAL DATA



Body: 16 x 16 x 1.4mm

LFBGA361
Low profile **F**ine Pitch **B**all **G**rid **A**rray



3 Revision history

Table 2. Document revision history

Date	Revision	Changes
3-Oct-2007	1	Initial release.
12-Oct-2007	2	Minor changes.

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