CompactFlash Card Controller
SST55LC100M

FEATURES:

- **CompactFlash Association Specification Revision 2.0 standard**
- **Interface for standard NAND Flash Media**
  - Flash Media Interface: 8-bit or 16-bit access
    - Supports up to 8 flash media devices directly
  - Supports Multi-Level Cell (MLC) and high density Single-Level Cell (SLC) flash media
    - 2KByte program page size only
- **Low power, 3.3V core operation**
- **5.0V or 3.3V host interface through V_{DDQ} pins**
- **Low current operation:**
  - Active mode: 25 mA/35 mA (3.3V/5.0V) (typical)
  - Sleep mode: 40 µA/50 µA (3.3V/5.0V) (typical)
- **20-byte Unique ID for Enhanced Security**
  - Factory Pre-programmed 10-byte Unique ID
  - User-Programmable 10-byte ID
- **Power Management Unit**
  - Immediate disabling of unused circuitry
- **Integrated Voltage Detector**
  - Industrial Controller requires external POR# signal
- **Start Up Time**
  - Sleep to Read: 200 ns
  - Sleep to Write: 200 ns

- **Pre-programmed Embedded Firmware**
  - Performs self-initialization on first system Power-on
  - Executes industry standard CF commands
  - Implements dynamic wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
  - Built-in ECC corrects up to 3 random 12-bit symbols of error per 512-byte sector
- **Multi-tasking Technology enables Fast Sustained Read and Write Performance**
  - Up to 10 MB/sec
- **Automatic Recognition and Initialization of Flash Media Devices**
  - Seamless integration into a standard SMT manufacturing process
  - 3 sec (typical) for flash drive recognition and setup
- **Commercial and Industrial Temperature Ranges**
  - 0°C to 70°C for Commercial operation
  - -40°C to +85°C for Industrial operation
- **Packages Available**
  - 84-ball TFBGA – 9mm x 9mm
  - 100-lead TQFP– 16mm x 16mm
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST55LC100M CompactFlash Card Controller is the heart of a high-performance, flash media-based Compact-Flash card solution. The SST55LC100M recognizes the control, address, and data signals on the CompactFlash bus and translates them into memory accesses to the standard NAND-type flash media. The SST55LC100M device supports Multi-Level Cell (MLC) and high density Single Level Cell (SLC) Flash media only. This technology suits solid state mass storage applications offering new, expanded functionality while enabling smaller, lighter designs with lower power consumption.

The CompactFlash interface is widely used in products such as portable and desktop computers, digital cameras, music players, handheld data collection scanners, PDAs, handy terminals, personal communicators, audio recorders, monitoring devices, and set-top boxes. The SST55LC100M supports CFA Specification Revision 2.0 commands standard with up to PIO Mode-4.

Utilizing SST's proprietary SuperFlash embedded memory technology, the CompactFlash card controller is pre-programmed with an embedded flash file system which, upon

initial power-up, recognizes the flash media devices, sets up a bad block table, executes all the necessary handshaking routines for flash media support, and, finally, performs the low-level format.

This technology enables a very fast and completely seamless integration of flash drives into an embedded design. For added manufacturing flexibility, system debug, re-initialization, and user customization can be accomplished through the CompactFlash interface.

The SST55LC100M CompactFlash Card Controller offers sustained read and write performance up to 10.0 MB/sec. The device can support up to 8 flash media devices directly for up to 8 GByte of maximum CompactFlash Card capacity.

The CompactFlash card controller comes packaged in an industry standard 100-lead TQFP package or 84-ball BGA package for easy integration into an SMT manufacturing process.

Advance Information

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Advance Information

1.0 GENERAL DESCRIPTION

The CompactFlash card controller contains a microcontroller and embedded flash file system integrated in TQFP or TFBGA packages. Refer to Figure 2-1 for the Compact-Flash card controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

1.1 Performance-optimized CompactFlash Card Controller

The heart of the CompactFlash card is the CompactFlash card controller which translates standard CF signals into flash media data and control signals. The following components contribute to the CompactFlash card controller's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates CF commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

The CompactFlash card controller uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The power management unit controls the power consumption of the CompactFlash card controller. The PMU dramatically reduces the power consumption of the CompactFlash card controller by putting the part of the circuitry that is not in operation into sleep mode.

1.1.4 SRAM Buffer

A key contributor to the CompactFlash card controller performance is an SRAM buffer. The buffer optimizes the host's data transfer to and from the flash media.

1.1.5 Embedded Flash File System

The embedded flash file system is an integral part of the CompactFlash card controller. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads.

2. Provides dynamic flash media wear leveling to spread the flash writes across all unused memory address space to increase the longevity of flash media.

3. Keeps track of data file structures.

1.1.6 Error Correction Code (ECC)

The CompactFlash card controller utilizes 72-bit Reed-Solomon Error Detection Code (EDC) and Error Correction Code (ECC), which provides the following error immunity for each 512-byte block of data:

1. Corrects up to three random 12-bit symbol errors.

2. Corrects single bursts up to 25 bits.

3. Detects single bursts up to 61 bits and double bursts up to 15 bits.

4. Detects up to six random 12-bit symbol errors.

1.1.7 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed to report initialization errors and allow manufacturers to debug system failures.

1.1.8 Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program, and Erase operations to multiple flash media devices. This interface optimizes the performance of Multi-Level Cell (MLC) and high density Single-Level Cell (SLC) flash media.

Advance Information

2.0 FUNCTIONAL BLOCKS
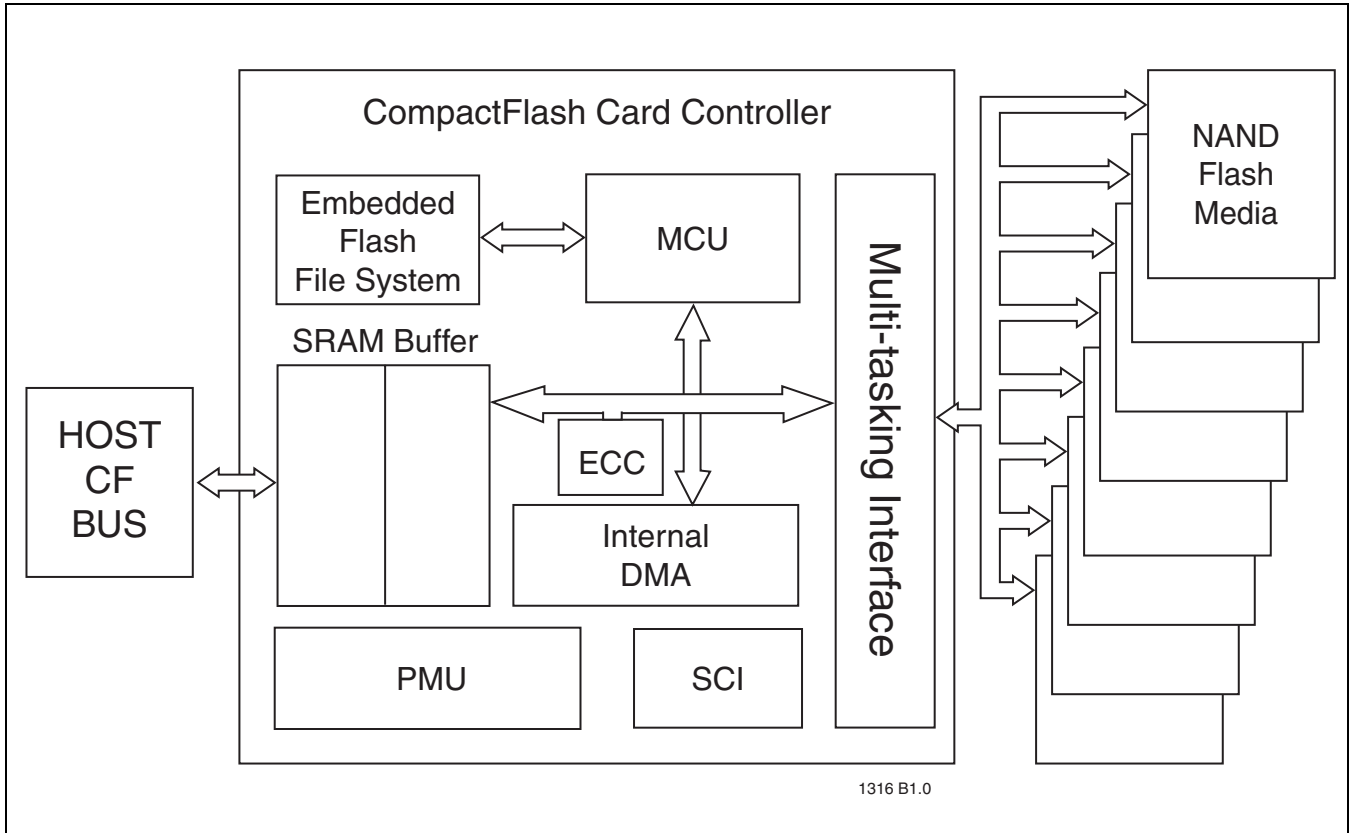
FIGURE   2-1: CompactFlash Card Controller Block Diagram

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the host are designated as inputs while signals that the CompactFlash card controller sources are outputs.

TOP VIEW (balls facing down)

	A	B	C	D	E	F	G	H	J	K
10		DASP#	D9	D11	D14	WE#	A9	A7	CSEL#	
9	SCIDOUT	V_{DD}(Core)	SCICLK	D10	D13	WAIT#	A8	IOWR#	PDIAG#	CE2#
8	V_{REG}	FCE1#	SCIDIN	D8	D12	D15	A10	WP/IOCS16#	A2	FAD15
7	FCE0#	FRE#	FCE2#	V_{SS}(IO)			V_{SS}(Core)	POR#	FAD7	FAD14
6	FCE3#	FCE6#	FCLE					FAD13	FAD6	FAD5
5	FCE4#	FALE	FCE5#					FAD11	FAD12	FAD4
4	FWE#	FWP#	D6	D4			V_{SS}(IO)	FAD2	FAD3	V_{DD}(IO)
3	EXTCLK$_{OUT}$	EXTCLK$_{IN}$	D7	D2	INPACK#	A5	A1	FAD0	FAD9	FAD10
2	RESET	D5	D3	D0	A3	A6	REG#	CE1#	FAD8	FAD1
1		V_{DDQ}(IO)	D1	OE#	A4	IORD#	INTRQ	A0	FCE7#/INTCLKEN	

1316 84-tfbga P1.0

FIGURE   3-1: Pin Assignments for 84-ball TFBGA
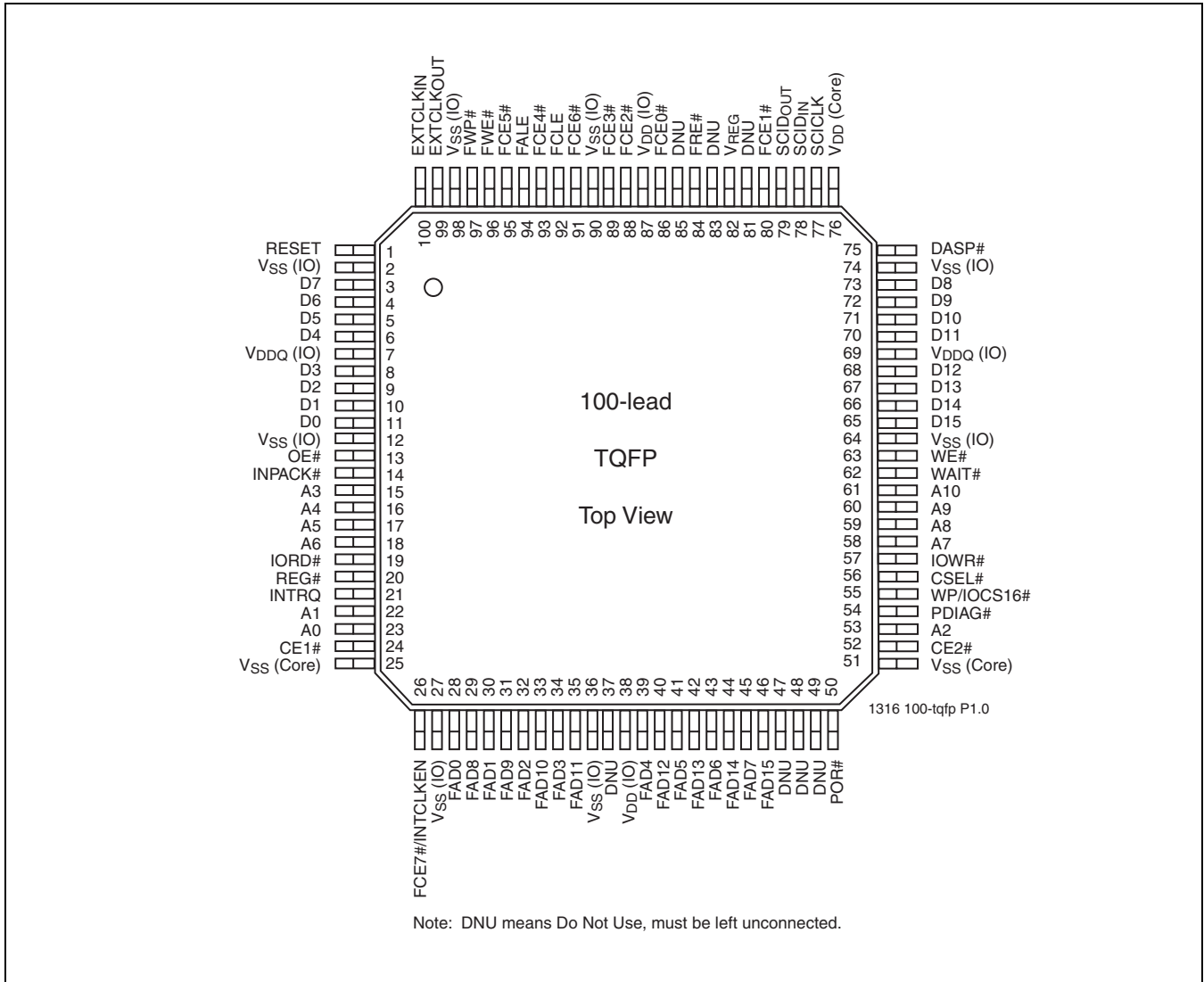
FIGURE   3-2: Pin Assignments for 100-lead TQFP

TABLE   3-1:Pin Assignments (1 of 6)

Signal Name	100-lead	84-ball	Pin Type	I/O Type[1]	Name and Functions
Host Side Interface					
A_{10}-A_0 (Memory Card mode)	61 60 59 58 18 17	G8 G10 G9 H10 F2 F3	I	I2D	These address lines, along with the REG# signal, are used to select the following: The I/O port address registers within the CompactFlash card, the memory mapped port address registers within the CompactFlash card, a byte in the card's information structure and its configuration control and status registers.
A_{10}-A_0 (PC Card I/O mode)	16 15 53 22 23	E1 E2 J8 G3 H1			This signal is the same as the PC Card Memory mode signal.
A_2-A_0 (True IDE mode)	53 22 23	J8 G3 H1			In True IDE mode only A[2:0] are used to select the one of eight registers in the Task File.
A_{10}-A_3	61 60 59 58 18 17 16 15	G8 G10 G9 H10 F2 F3 E1 E2			The remaining address lines should be grounded by the host.
BVD1 (Memory Card mode)	54	J9	O	I2U, O1	This signal is asserted high as BVD1 is not supported.
STSCHG# (PC Card I/O mode)					This signal is asserted low to alert the host to changes in the Ready and Write Protect states, while the I/O interface is configured. Its use is controlled by the Card Config and Status register.
PDIAG# (True IDE mode)					In the True IDE mode, this input/output is the Pass Diagnostic signal in the master/slave handshake protocol.
BVD2 (Memory Card mode)	75	B10	O	I2U, O1	This signal is asserted high as BVD2 is not supported.
SPKR# (PC Card I/O mode)					This output line is always driven to a high state in I/O mode since the CompactFlash card controller does not support the audio function.
DASP# (True IDE mode)					In the True IDE mode, this input/output is the Disk Active/Slave Present signal in the master/slave handshake protocol.

Advance Information

TABLE   3-1:Pin Assignments (Continued) (2 of 6)

Signal Name	100-lead	84-ball	Pin Type	I/O Type[1]	Name and Functions
CE1#, CE2# (Memory Card mode)	24 52	H2 K9	I	I3U	**Card Enable:** These input signals are used both to select the card and to indicate to the card whether a byte or a word operation is being performed. CE2# always accesses the Odd Byte of the word. CE1# accesses the Even Byte or the Odd Byte of the word depending on A_0 and CE2#. A multiplexing scheme based on A_0, CE1#, CE2# allows 8-bit hosts to access all data on D_0-D_7. See Tables 8-1, 8-3, 8-7, 8-8, and 8-9.
CE1#, CE2# (PC Card I/O mode)					**Card Enable:** This signal is the same as the PC Card Memory mode signal.
CS0#, CS1# (True IDE mode)					In the True IDE mode CS0# is the chip select for the task file registers while CS1# is used to select the Alternate Status register and the Device Control register.
CSEL# (Memory Card mode)	56	J10	I	I2U	This signal is not used for this mode.
CSEL# (PC Card I/O mode)					This signal is not used for this mode.
CSEL# (True IDE mode)					This internally pulled up signal is used to configure this device as a master or a slave when configured in the True IDE mode. When this pin is grounded, this device is configured as a master. When the pin is open, this device is configured as a slave.
D_{15}-D_0 (Memory Card mode)	65 66 67	F8 E10 E9			These lines carry the Data, Commands and Status information between the host and the controller. D_0 is the LSB of the Even Byte of the Word. D_8 is the LSB of the Odd Byte of the Word.
D_{15}-D_0 (PC Card I/O mode)	68 70	E8 D10			This signal is the same as the PC Card Memory mode signal.
D_{15}-D_0 (True IDE mode)	71 72 73 3 4 5 6 8 9 10 11	D9 C10 D8 C3 C4 B2 D4 C2 D3 C1 D2	I/O	I2D, O2	In True IDE mode, all Task File operations occur in Byte-Mode on the low order bus D_7-D_0 while all data transfers are 16 bit using D_{15}-D_0.
INPACK# (Memory Card mode)					This signal is not used in this mode.
INPACK# (PC Card I/O mode)	14	E3	O	O1	The Input Acknowledge signal is asserted by the CompactFlash card when the card is selected and responding to an I/O read cycle at the address that is on the address bus. This signal is used by the host to control the enable of any input data buffers between the CompactFlash card and the CPU.
Reserved (True IDE mode)					In True IDE mode this output signal is not used and should not be connected at the host.

TABLE 3-1:Pin Assignments (Continued) (3 of 6)

Signal Name	100-lead	84-ball	Pin Type	I/O Type[1]	Name and Functions
IORD# (Memory Card mode)	19	F1	I	I3U	This signal is not used in this mode.
IORD# (PC Card I/O mode)					This is an I/O Read strobe generated by the host. This signal gates I/O data onto the bus from the CompactFlash card when the card is configured to use the I/O interface.
IORD# (True IDE mode)					In True IDE mode, this signal has the same function as in PC card I/O mode.
IOWR# (Memory Card mode)	57	H9	I	I3U	This signal is not used in this mode.
IOWR# (PC Card I/O mode)					The I/O Write strobe pulse is used to clock I/O data on the card data bus into the CompactFlash card controller registers when the CompactFlash card is configured to use the I/O interface.
IOWR# (True IDE mode)					In True IDE mode, this signal has the same function as in PC Card I/O mode.
OE# (Memory Card mode)	13	D1	I	I3U	This is an Output Enable strobe generated by the host interface. It is used to read data from the CompactFlash card in Memory mode and to read the CIS and configuration registers.
OE# (PC Card I/O mode)					In PC Card I/O mode, this signal is used to read the CIS and configuration registers.
ATASEL# (True IDE mode)					To enable True IDE mode this input should be grounded by the host.
Ready (Memory Card mode)	21	G1	O	O1	In Memory mode this signal is set high when the CompactFlash card is ready to accept a new data transfer operation and held low when the card is busy. At power up and at Reset, the Ready signal is held low (busy) until the CompactFlash card has completed its power up or reset function. No access of any type should be made to the CompactFlash card during this time.
IREQ# (PC Card I/O mode)					I/O Operation - After the CompactFlash card has been configured for I/O operation, this signal is used as Interrupt Request. This line is strobed low to generate a pulse mode interrupt or held low for a level mode interrupt.
INTRQ (True IDE mode)					In True IDE mode signal is the active high Interrupt Request to the host.
REG# (Memory Card mode)	20	G2	I	I3U	This signal is used during Memory cycles to distinguish between Common Memory and Register (Attribute) Memory Attribute Memory Select accesses. High for Common Memory, Low for Attribute Memory.
REG# (PC Card I/O mode)					The signal must also be active (low) during I/O Cycles when the I/O address is on the Bus.
Reserved (True IDE mode)					In True IDE mode this input signal is not used and should be connected to V_{DD} by the host.

S71316-00-000   3/06

Advance Information

TABLE   3-1:Pin Assignments (Continued) (4 of 6)

Signal Name	100-lead	84-ball	Pin Type	I/O Type[1]	Name and Functions
RESET (Memory Card mode)	1	A2	I	I4U	When the pin is high, this signal Resets the CompactFlash card. The CompactFlash card is Reset only at power up if this pin is left high or open from power-up. The CompactFlash card is also Reset when the Soft-Reset bit in the Card Configuration Option register is set.
RESET (PC Card I/O mode)					This signal is the same as the PC Card Memory mode signal.
RESET# (True IDE mode)					In the True IDE mode this input pin is the active low hardware reset from the host.
WAIT# (Memory Card mode)	62	F9	O	O1	The WAIT# signal is driven low by the CompactFlash Card to signal the host to delay completion of a memory or I/O cycle that is in progress.
WAIT# (PC Card I/O mode)					This signal is the same as the PC Card Memory mode signal.
IORDY# (True IDE mode)					In True IDE mode this output signal may be used as IORDY.
WE# (Memory Card mode)	63	F10	I	I3U	This is a signal driven by the host and used for strobing memory write data to the registers of the CompactFlash card when the card is configured in the memory interface mode. It is also used for writing the configuration registers.
WE# (PC Card I/O mode)					In PC Card I/O mode, this signal is used for writing the configuration registers.
WE# (True IDE mode)					In True IDE mode this input signal is not used and should be connected to V_{DD} by the host.
WP (Memory Card mode)	55	H8	O	O2	The CompactFlash card does not have a write protect switch. This signal is held low after the completion of the reset initialization sequence.
IOIS16# (PC Card I/O mode)					When the CompactFlash card is configured for I/O Operation Pin 55 is used for the I/O# Selected is 16-bit Port (IOIS16#) function. A Low signal indicates that a 16 bit or Odd Byte only operation can be performed at the addressed port.
IOCS16# (True IDE mode)					In True IDE mode this output signal is asserted low when this device is expecting a word data transfer cycle.

S71316-00-000   3/06

TABLE   3-1:Pin Assignments (Continued) (5 of 6)

Signal Name	100-lead	84-ball	Pin Type	I/O Type[1]	Name and Functions
Flash Media Interface					
FWP#	97	B4	O	O5	Active Low Flash Media Chip Write Protect Connect this pin to the NAND flash media Write Protect pin
FRE#	84	B7	O	O5	Active Low Flash Media Chip Read
FWE#	96	A4	O	O5	Active Low Flash Media Chip Write
FCLE	92	C6	O	O5	Active High Flash Media Chip Command Latch Enable
FALE	94	B5	O	O5	Active High Flash Media Chip Address Latch Enable
FAD15	46	K8	I/O	I3U/O5	Flash Media Chip High Byte Address/Data Bus pins
FAD14	44	K7			
FAD13	42	H6			
FAD12	40	J5			
FAD11	35	H5			
FAD10	33	K3			
FAD9	31	J3			
FAD8	29	J2			
FAD7	45	J7	I/O	I3U/O5	Flash Media Chip Low Byte Address/Data Bus pins
FAD6	43	J6			
FAD5	41	K6			
FAD4	39	K5			
FAD3	34	J4			
FAD2	32	H4			
FAD1	30	K2			
FAD0	28	H3			
FCE6#	91	B6	O	O4	Active Low Flash Media Chip Enable pin
FCE5#	95	C5			
FCE4#	93	A5			
FCE3#	89	A6			
FCE2#	88	C7			
FCE1#	80	B8			
FCE0#	86	A7			
FCE7#/INTCLKEN	26	J1	I/O	I3D/O4	Active Low Flash Media Chip Enable pin This pin is sensed during the Power-on Reset (POR) to select an Internal Clock mode. If this pin is pulled up during the Power-on Reset then the Internal Clock is selected.
Serial Communication Interface (SCI)					
SCICLK	77	C9	I	I3U	SCI interface clock
SCID$_{IN}$	78	C8	I	I3U	SCI interface data input
SCID$_{OUT}$	79	A9	O	O4	SCI interface data output

Advance Information

TABLE   3-1:Pin Assignments (Continued) (6 of 6)

Signal Name	100-lead	84-ball	Pin Type	I/O Type[1]	Name and Functions
External Clock Option					
FCE7#/INTCLKEN	26	J1	I/O	I3D/O4	Active Low Flash Media Chip Enable pin This pin is sensed during the Power-on Reset (POR) to select an Internal Clock mode. If this pin is pulled up during the Power-on Reset then the Internal Clock is selected.
EXTCLK$_{IN}$	100	B3	I	I4Z	External Clock source input pin
EXTCLK$_{OUT}$	99	A3	O	O4	External Clock source output pin
Miscellaneous					
V$_{DD}$ (core)	76	B9	PWR		V$_{DD}$ (3.3V)
V$_{DD}$ (IO)	38 87	K4	PWR		V$_{DD}$ (3.3V)
V$_{DDQ}$ (IO)	7 69	B1	PWR		V$_{DDQ}$ (5V/3.3V) for Host interface
V$_{REG}$	82	A8	O	O5	Voltage Regulator Output
V$_{SS}$ (core)	25 51	G7	PWR		Ground for core
V$_{SS}$ (IO)	2 12 27 36 64 74 90 98	D7 G4	PWR		Ground for I/O
POR#	50	H7	I	Analog Input[2]	**Power-on Reset (POR):** Active Low
DNU	37 47 48 49 81 83 85				Do Not Use, must be left unconnected.

T3-1.0 1316

1. Please refer to Section 10.1 for details.
   I = Input
   0 = Output
2. Analog input for supply voltage detection

4.0 CAPACITY SPECIFICATION

Table 4-1 shows the default capacity and specific settings for heads, sectors, and cylinders. Users can reduce the default settings in the drive ID table (see Table 9-8) for customization. If the total number of bytes is less than the default, the remaining space could be used as spares to increase the flash drive endurance.

TABLE   4-1: Default CompactFlash Card Settings

Capacity	Total Bytes	Cylinders	Heads	Sectors
128 MB	128,450,560	980	8	32
256 MB	256,901,120	980	16	32
512 MB	512,483,328	993	16	63
1 GB	1,024,966,656	1986	16	63
2 GB	2,048,901,120	3970	16	63
4 GB	4,110,188,544	7964	16	63
6 GB	6,146,703,360	11910	16	63
8 GB	8,195,604,480	15880	16	63

T4-1.0 1316

4.1 Functional Specifications

Table 4-2 shows the performance and the maximum capacity supported by each controller.

TABLE   4-2: Functional Specification

Functions	SST55LC100M
CompactFlash Card Supported Capacity	up to 8 GB
CompactFlash Card Performance-Sustained Write speed	Up to 10.0 MB/sec
CompactFlash Card Performance-Sustained Read speed	Up to 10.0 MB/sec

T4-2.0 1316

Advance Information

5.0 MANUFACTURING SUPPORT

The CompactFlash card controller firmware contains a list of supported standard NAND flash media devices. Upon initial Power-on, the controller scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices in the CompactFlash card controller, the controller performs drive recognition based on the algorithm provided by the flash media suppliers. This includes setting up the bad block table, executing all the necessary handshaking routines for flash media support, and, finally, performing the low-level format. For Power-up timing specifications, please refer to Table 10-2.

Please contact SST for the most current list of supported NAND Flash media devices.

In the event that the NAND flash media device ID is not recognized by the CompactFlash card controller, the user has an option of adding this device to the controller device table through the manufacturing interface provided by SST. Please contact SST for the CompactFlash card controller manufacturing interface software. If the drive initialization fails, and a visual inspection is unable to determine the problem, the SST55LC100M CompactFlash card controller provides a comprehensive interface for manufacturing flow debug. This interface not only allows debug of the failure and manual reset of the initialization process, but also allows customization of user definable options.

5.1 CF Interface

The CompactFlash interface can be used for manufacturing support. SST provides an example of a DOS-based solution (an executable routine downloadable from SST's web site) for manufacturing debug and rework.

5.2 Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for manufacturing error reporting. The SCI consists of 3 active signals: $SCID_{OUT}$, $SCID_{IN}$, and SCICLK.

6.0 EXTERNAL CLOCK INTERFACE

The external clock interface allows CompactFlash card controller operation from an external clock source generated by an RC circuit. Do not use a free running clock as input to the EXTCLKIN pin; an RC circuit must be used. Contact SST for reference circuit and recommended external clock settings.

While the controller has an internal clock source, the external clock source allows slowing of the system clock operation to limit the peak current and overcome additional bus loading.

The external clock interface consists of three signals: INTCLKEN, EXTCLKIN, and EXTCLKOUT. The INTCLKEN pin selects between external and internal clock sources for the CompactFlash card controller. If this pin is pulled high before device Power-on, then the internal clock source is selected; otherwise, the external clock source is selected. The EXTCLKIN and EXTCLKOUT signals are the input and output clock signals, respectively.

7.0 POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

Please contact SST to obtain CompactFlash reference design schematics including the POR# circuit for commercial and industrial CompactFlash offerings.
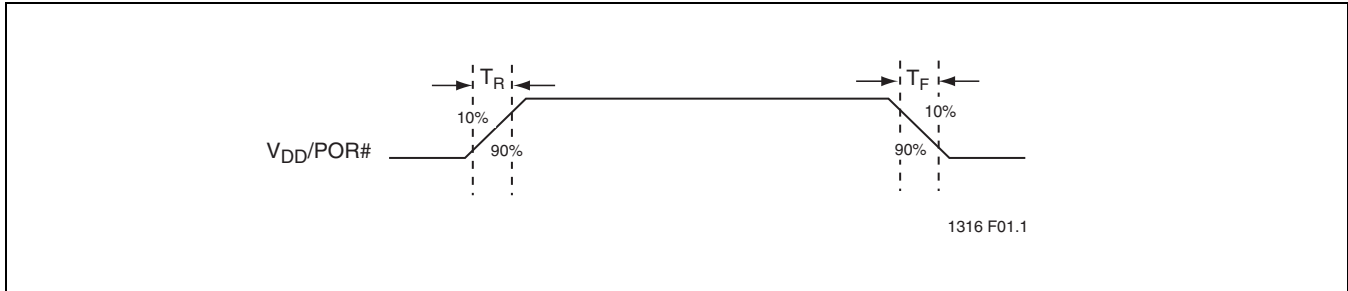
FIGURE 7-1: Power-on and Brown-out Reset Timing (Commercial Temperature)

TABLE 7-1: Power-on and Brown-out Reset Timing (Commercial Temperature)

Item	Symbol	Min	Max	Units
V_{DD}/POR# Rise Time[1]	T_R		200	ms
V_{DD}/POR# Fall Time[2]	T_F		200	ms

T7-1.0 1316

1. V_{DD} Rise Time should be greater than or equal to POR# Rise Time.
2. V_{DD} Fall Time should be slower than or equal to POR# Fall Time.
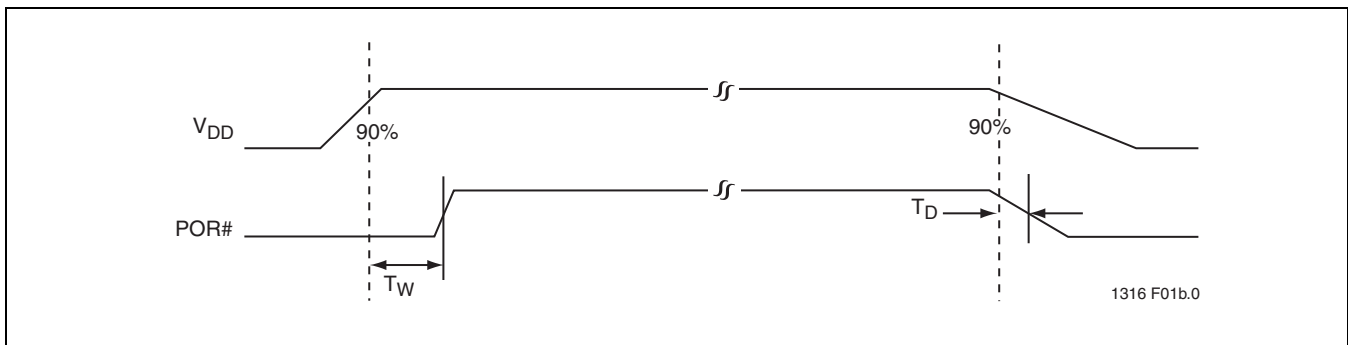
FIGURE 7-2: Power-on and Brown-out Reset Timing (Industrial Temperature)

TABLE 7-2: Power-on and Brown-out Reset Timing (Industrial Temperature)

Item	Symbol	Min	Max	Units
POR Wait Time	T_W	0.1		ms
Brown-out Delay Time	T_D		30	µs

T7-2.0 1316

Advance Information

8.0 CARD CONFIGURATION

The CompactFlash cards are identified by appropriate information in the Card Information Structure (CIS). The following configuration registers are used to coordinate the I/O spaces and the Interrupt level of cards that are located in the system. In addition, these registers provide a method for accessing status information about the Compact-Flash card that may be used to arbitrate between multiple interrupt sources on the same interrupt level or to replace status information that appears on dedicated pins in memory cards that have alternate use in I/O cards.

TABLE   8-1: Registers and Memory Space Decoding

CE2#	CE1#	REG#	OE#	WE#	A_{10}	A_9	A_8-A_4	A_3	A_2	A_1	A_0	Selected Space
1	1	X	X	X	X	X	XX	X	X	X	X	Standby
X	0	0	0	1	0	1	XX	X	X	X	0	Configuration Registers Read
1	0	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit D_7-D_0)
0	1	1	0	1	X	X	XX	X	X	X	X	Common Memory Read (8 bit D_{15}-D_8)
0	0	1	0	1	X	X	XX	X	X	X	0	Common Memory Read (16 bit D_{15}-D_0)
X	0	0	1	0	0	1	XX	X	X	X	0	Configuration Registers Write
1	0	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit D_7-D_0)
0	1	1	1	0	X	X	XX	X	X	X	X	Common Memory Write (8 bit D_{15}-D_8)
0	0	1	1	0	X	X	XX	X	X	X	0	Common Memory Write (16 bit D_{15}-D_0)
X	0	0	0	1	0	0	XX	X	X	X	0	Card Information Structure Read
1	0	0	1	0	0	0	XX	X	X	X	0	Invalid Access (CIS Write)
1	0	0	0	1	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Read)
1	0	0	1	0	X	X	XX	X	X	X	1	Invalid Access (Odd Attribute Write)
0	1	0	0	1	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Read)
0	1	0	1	0	X	X	XX	X	X	X	X	Invalid Access (Odd Attribute Write)

T8-1.0 1316

TABLE   8-2: Configuration Registers Decoding

CE2#	CE1#	REG#	OE#	WE#	A_{10}	A_9	A_8-A_4	A_3	A_2	A_1	A_0	Selected Register
X	0	0	0	1	0	1	00	0	0	0	0	Configuration Option Reg Read
X	0	0	1	0	0	1	00	0	0	0	0	Configuration Option Reg Write
X	0	0	0	1	0	1	00	0	0	1	0	Card Status Register Read
X	0	0	1	0	0	1	00	0	0	1	0	Card Status Register Write
X	0	0	0	1	0	1	00	0	1	0	0	Pin Replacement Register Read
X	0	0	1	0	0	1	00	0	1	0	0	Pin Replacement Register Write
X	0	0	0	1	0	1	00	0	1	1	0	Socket and Copy Register Read
X	0	0	1	0	0	1	00	0	1	1	0	Socket and Copy Register Write

T8-2.0 1316

Note: The location of the card configuration registers should always be read from the CIS locations 0000H to 0198H.
No writes should be performed to the CompactFlash card attribute memory except to the card configuration register addresses.
All other attribute memory locations are reserved.

Advance Information

8.1 Attribute Memory Function

Attribute memory is a space where CompactFlash card identification and configuration information are stored. This memory is limited to 8-bit wide accesses, only at even addresses. The card configuration registers are also located in this space.

For the Attribute Memory Read function, signals REG# and OE# must be active and WE# inactive during the cycle. As in the Main Memory Read functions, the signals CE1# and CE2# control the Even Byte and Odd Byte address, but only the Even Byte data is valid during the Attribute Memory access. Refer to Table 8-3 below for signal states and bus validity for the Attribute Memory function.

TABLE   8-3:Attribute Memory Function

Function Mode	REG#	CE2#	CE1#	A_{10}	A_9	A_0	OE#	WE#	D_{15}-D_8	D_7-D_0
Standby mode	X	V_{IH}	V_{IH}	X	X	X	X	X	High Z	High Z
Read Byte Access CIS ROM (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
Write Byte Access CIS (8 bits) (Invalid)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Byte Access Configuration (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
Write Byte Access Configuration (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Word Access CIS (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Not Valid	Even Byte
Write Word Access CIS (16 bits) (Invalid)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Don't Care	Even Byte
Read Word Access Configuration (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Not Valid	Even Byte
Write Word Access Configuration (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Don't Care	Even Byte

T8-3.0 1316

Note: The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations.

8.2 Configuration Option Register (Address 200H in Attribute Memory)

The Configuration Option register is used to configure the cards interface, address decoding and interrupt and to issue a soft reset to the CompactFlash card.

Operation	D7	D6	D5	D4	D3	D2	D1	D0
R/W	SRESET	LevIREQ	Conf5	Conf4	Conf3	Conf2	Conf1	Conf0

SRESET — Soft Reset - Setting this bit to one (1), waiting the minimum reset width time and returning to zero (0) places the CompactFlash card in the Reset state. Setting this bit to one (1) is equivalent to assertion of the RESET signal except that the SRESET bit is not cleared. Returning this bit to zero (0) leaves the CompactFlash card in the same un-configured Reset state as following power-up and hardware reset. This bit is set to zero (0) by power-up and hardware reset. Using the PCMCIA Soft Reset is considered a hard Reset by the ATA Commands. Contrast with Soft Reset in the Device Control register.

LevIREQ — This bit is set to one (1) when Level Mode Interrupt is selected, and zero (0) when Pulse mode is selected. Set to zero (0) by Reset.

Conf5-Conf0 — Configuration Index. Set to zero (0) by reset. It's used to select operation mode of the CompactFlash card as shown below.
Note: Conf5 and Conf4 are reserved and must be written as (0).

Advance Information

TABLE   8-4: Card Configurations

Conf5	Conf4	Conf3	Conf2	Conf1	Conf0	Disk Card Mode
0	0	0	0	0	0	Memory Mapped
0	0	0	0	0	1	I/O Mapped, any 16 Byte system decoded boundary
0	0	0	0	1	0	I/O Mapped, 1F0H-1F7H/3F6H-3F7H
0	0	0	0	1	1	I/O Mapped, 170H-177H/376H-377H

T8-4.0 1316

TABLE   8-5: Card Configuration and Status Register Organization

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Changed	SigChg	IOis8	XE#	Audio	PwrDwn	Int	0
Write	0	SigChg	IOis8	XE#	Audio	PwrDwn	0	0

Changed   Indicates that one or both of the Pin Replacement register CRdy or CWProt bits are set to one (1). When the Changed bit is set, Pin 46 (STSCHG#) is held low if the SigChg bit is a One (1) and the CompactFlash card is configured for the I/O interface.

SigChg   This bit is set and reset by the host to enable and disable a state-change "signal" from the Status register, the Changed bit control pin 46 the Changed Status signal. If no state change signal is desired, this bit should be set to zero (0) and pin 46 (STSCHG#) signal will be held high while the CompactFlash card is configured for I/O.

IOis8   The host sets this bit to a one (1) if the CompactFlash card is to be configured in an 8-bit I/O mode. The CompactFlash card is always configured for both 8- and 16-bit I/O, so this bit is ignored.

XE#:   This bit has value 0 and is not writable.

Audio: This bit should always be zero for CompactFlash cards.

PwrDwn   This bit indicates whether the host requests the CompactFlash card to be in the power saving or active mode. When the bit is one (1), the CompactFlash card enters a power down mode. When zero (0), the host is requesting the CompactFlash card to enter the active mode. The PCMCIA Ready value becomes BUSY when this bit is changed. Ready will not become ready until the power state requested has been entered. The CompactFlash card automatically powers down when it is idle and powers back up when it receives a command.

Int   This bit represents the internal state of the interrupt request. This value is available whether or not I/O interface has been configured. This signal remains true until the condition which caused the interrupt request has been serviced. If interrupts are disabled by the -IEn bit in the Device Control register, this bit is a zero (0).

8.3 Pin Replacement Register (Address 204H in Attribute Memory)

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	0	0	CRDY/BSY#	CWProt	1	1	RDY/BSY#	WProt
Write	0	0	CRDY/BSY#	CWProt	0	0	MRDY/BSY#	MWProt

CRDY/BSY#   This bit is set to one (1) when the bit RDY/BSY# changes state. This bit can also be written by the host.

CWProt   This bit is set to one (1) when the RWprot changes state. This bit may also be written by the host.

RDY/BSY#   This bit is used to determine the internal state of the RDY/BSY# signal. This bit may be used to determine the state of the Ready/-Busy as this pin has been reallocated for use as Interrupt Request on an I/O card. When written, this bit acts as a mask for writing the corresponding bit CRDY/BSY#.

WProt: This bit is always zero (0).
When written, this bit acts as a mask for writing the corresponding bit CWProt.

MRDY/BSY#   This bit acts as a mask for writing the corresponding bit CRDY/BSY#.

MWProt: This bit when written acts as a mask for writing the corresponding bit CWProt.

TABLE   8-6:   Pin Replacement Changed Bit/Mask Bit Values

	Written by Host			
Initial Value of (C) Status	**"C" Bit**	**"M" Bit**	**Final "C" Bit**	**Comments**
0	X	0	0	Unchanged
1	X	0	1	Unchanged
X	0	1	0	Cleared by host
X	1	1	1	Set by host

T8-6.0 1316

8.4 Socket and Copy Register (Address 206H in Attribute Memory)

This register contains additional configuration information. This register is always written by the system before writing the card's Configuration Index register.

Socket and Copy Register Organization:

Operation	D7	D6	D5	D4	D3	D2	D1	D0
Read	Reserved	0	0	Drive #	0	0	0	0
Write	0	0	0	Drive #	X	X	X	X

Reserved   This bit is reserved for future standardization. This bit must be set to zero (0) by the software when the register is written.

Drive #   This bit indicates the drive number of the card for twin card configuration.
Twin card configuration is currently not supported

X   The socket number is ignored by the CompactFlash card.

Advance Information

8.5 I/O Transfer Function

8.5.1 I/O Function

The I/O transfer to or from the CompactFlash card can be either 8 or 16 bits. When a 16-bit accessible port is addressed, the signal IOIS16# is asserted by the CompactFlash card. Otherwise, the IOIS16# signal is de-asserted. When a 16 bit transfer is attempted, and the IOIS16# signal is not asserted by the CompactFlash card, the system must generate a pair of 8-bit references to access the word's Even Byte and Odd Byte. The Compact-Flash card permits both 8 and 16 bit accesses to all of its I/O addresses, so IOIS16# is asserted for all addresses to which the CompactFlash card responds.

TABLE   8-7:I/O Function

Function Code	REG#	CE2#	CE1#	A_0	IORD#	IOWR#	D_{15}-D_8	D_7-D_0
Standby mode	X	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Byte Input Access (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	High Z	Odd Byte
Byte Output Access (8 bits)	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	Odd Byte
Word Input Access (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Odd Byte	Even Byte
Word Output Access (16 bits)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Odd Byte	Even Byte
I/O Read Inhibit	V_{IH}	X	X	X	V_{IL}	V_{IH}	Don't Care	Don't Care
I/O Write Inhibit	V_{IH}	X	X	X	V_{IH}	V_{IL}	High Z	High Z
High Byte Input Only (8 bits)	V_{IL}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Odd Byte	High Z
High Byte Output Only (8 bits)	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Odd Byte	Don't Care

T8-7.0 1316

8.6 Common Memory Transfer Function

8.6.1 Common Memory Function

The Common Memory Transfer to or from the CompactFlash card can be either 8 or 16 bits.
The CompactFlash card permits both 8 and 16 bit accesses to all of its Common Memory addresses.

TABLE   8-8:Common Memory Function

Function Code	REG#	CE2#	CE1#	A_0	OE#	WE#	D_{15}-D_8	D_7-D_0
Standby mode	X	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Byte Read Access (8 bits)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	High Z	Even Byte
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	High Z	Odd Byte
Byte-Write Access (8 bits)	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Don't Care	Even Byte
	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Don't Care	Odd Byte
Word Read Access (16 bits)	V_{IH}	V_{IL}	V_{IL}	X	V_{IL}	V_{IH}	Odd Byte	Even Byte
Word-Write Access (16 bits)	V_{IH}	V_{IL}	V_{IL}	X	V_{IH}	V_{IL}	Odd Byte	Even Byte
Odd Byte Read Only (8 bits)	V_{IH}	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	Odd Byte	High Z
Odd Byte-Write Only (8 bits)	V_{IH}	V_{IL}	V_{IH}	X	V_{IH}	V_{IL}	Odd Byte	Don't Care

T8-8.0 1316

S71316-00-000   3/06

8.7 True IDE Mode I/O Transfer Function

8.7.1 True IDE Mode I/O Function

The CompactFlash card can be configured in a True IDE mode of operation. The CompactFlash card is configured in this mode only when the OE# input signal is grounded by the host during the power off to power on cycle. In this True IDE mode the PCMCIA protocol and configuration are disabled and only I/O operations to the Task File and Data register are allowed. In this mode no Memory or Attribute registers are accessible to the host. CompactFlash cards permit 8 bit data accesses if the user issues a Set Feature Command to put the device in 8-bit mode.

Note: Removing and reinserting the CompactFlash card while the host computer's power is on will reconfigure the CompactFlash to PC Card ATA mode from the original True IDE mode. To configure the CompactFlash card in True IDE mode, the 50-pin socket must be power cycled with the CompactFlash card inserted and OE# (output enable) asserted.

Table 8-9 defines the function of the operations for the True IDE mode.

TABLE 8-9:True IDE Mode I/O Function

Function Code	CE2#	CE1#	A_0-A_2	IORD#	IOWR#	D_{15}-D_8	D_7-D_0
Invalid mode	V_{IL}	V_{IL}	X	X	X	High Z	High Z
Standby mode	V_{IH}	V_{IH}	X	X	X	High Z	High Z
Task File Write	V_{IH}	V_{IL}	1-7H	V_{IH}	V_{IL}	Don't Care	Data In
Task File Read	V_{IH}	V_{IL}	1-7H	V_{IL}	V_{IH}	High Z	Data Out
Data Register Write	V_{IH}	V_{IL}	0	V_{IH}	V_{IL}	Odd Byte In	Even Byte In
Data Register Read	V_{IH}	V_{IL}	0	V_{IL}	V_{IH}	Odd Byte Out	Even Byte Out
Control Register Write	V_{IL}	V_{IH}	6H	V_{IH}	V_{IL}	Don't Care	Control In
Alt Status Read	V_{IL}	V_{IH}	6H	V_{IL}	V_{IH}	High Z	Status Out
Drive Address	V_{IL}	V_{IH}	7H	V_{IL}	V_{IH}	High Z	Data Out

T8-9.0 1316

Advance Information

9.0 SOFTWARE INTERFACE

9.1 CF-ATA Drive Register Set Definition and Protocol

The CompactFlash card can be configured as a high performance I/O device through:

1. Standard PC-AT disk I/O address spaces 1F0H-1F7H, 3F6H-3F7H (primary);
   170H-177H, 376H-377H (secondary) with IRQ 14 (or other available IRQ)

2. Any system decoded 16 Byte I/O block using any available IRQ

3. Memory space

The communication to or from the CompactFlash card is done using the Task File registers which provide all the necessary registers for control and status information. The CompactFlash interface connects peripherals to the host using four register mapping methods. The following is a detailed description of these methods.

TABLE   9-1:I/O Configurations

Standard Configurations			
Config Index	**I/O or Memory**	**Address**	**Description**
0	Memory	0H-FH, 400H-7FFH	Memory Mapped
1	I/O	XX0H-XXFH	I/O Mapped 16 Contiguous registers
2	I/O	1F0H-1F7H, 3F6H-3F7H	Primary I/O Mapped
3	I/O	170H-177H, 376H-377H	Secondary I/O Mapped

T9-1.0 1316

9.1.1 I/O Primary and Secondary Address Configurations

TABLE   9-2:Primary and Secondary I/O Decoding

REG#	A_9-A_4	A_3	A_2	A_1	A_0	IORD#=0	IOWR#=0	Note
0	1F(17)H	0	0	0	0	Even RD Data	Even WR Data	1,2
0	1F(17)H	0	0	0	1	Error register	Features	1,2
0	1F(17)H	0	0	1	0	Sector Count	Sector Count	
0	1F(17)H	0	0	1	1	Sector No.	Sector No.	
0	1F(17)H	0	1	0	0	Cylinder Low	Cylinder Low	
0	1F(17)H	0	1	0	1	Cylinder High	Cylinder High	
0	1F(17)H	0	1	1	0	Select Card/Head	Select Card/Head	
0	1F(17)H	0	1	1	1	Status	Command	
0	3F(37)H	0	1	1	0	Alt Status	Device Control	
0	3F(37)H	0	1	1	1	Drive Address	Reserved	

T9-2.0 1316

1. Register 0 is accessed with CE1# low and CE2# low (and A_0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D_{15}-D_0). This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers which lie at offset 1. When accessed twice as byte register with CE1# low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access.

2. A byte access to register 0 with CE1# high and CE2# low accesses the error (read) or feature (write) register.

Note: Address lines which are not indicated are ignored by the CompactFlash card for accessing all the registers in this table.

9.1.2 Contiguous I/O Mapped Addressing

When the system decodes a contiguous block of I/O registers to select the CompactFlash card, the registers are accessed in the block of I/O space decoded by the system as follows:

TABLE   9-3:Contiguous I/O Decoding

REG#	A_3	A_2	A_1	A_0	Offset	IORD#=0	IOWR#=0	Notes
0	0	0	0	0	0	Even RD Data	Even WR Data	1
0	0	0	0	1	1	Error	Features	2
0	0	0	1	0	2	Sector Count	Sector Count	
0	0	0	1	1	3	Sector No.	Sector No.	
0	0	1	0	0	4	Cylinder Low	Cylinder Low	
0	0	1	0	1	5	Cylinder High	Cylinder High	
0	0	1	1	0	6	Select Card/Head	Select Card/Head	
0	0	1	1	1	7	Status	Command	
0	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
0	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
0	1	1	0	1	D	Dup. Error	Dup. Features	2
0	1	1	1	0	E	Alt Status	Device Ctl	
0	1	1	1	1	F	Drive Address	Reserved	

T9-3.0 1316

1. Register 0 is accessed with CE1# low and CE2# low (and A_0 = Don't Care) as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with CE1# low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access. A byte access to register 0 with CE1# high and CE2# low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9, and D are non-overlapping duplicates of the registers at offset 0 and 1.
   Register 8 is equivalent to register 0, while register 9 accesses the Odd Byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred Odd Byte then Even Byte.

   Repeated byte accesses to register 8 or 0 will access consecutive (Even then Odd) Bytes from the data buffer. Repeated word accesses to register 8, 9, or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (Even then Odd) Bytes from the data buffer. Byte accesses to register 9 access only the Odd Byte of the data.

Note: Address lines which are not indicated are ignored by the CompactFlash card for accessing all the registers in this table.

Advance Information

9.1.3 Memory Mapped Addressing

When the CompactFlash card registers are accessed via memory references, the registers appear in the common memory space window: 0-2 KByte as follows:

TABLE 9-4:Memory Mapped Decoding

REG#	A_{10}	A_9-A_4	A_3	A_2	A_1	A_0	Offset	OE#=0	WE#=0	Notes
1	0	X	0	0	0	0	0	Even RD Data	Even WR Data	1,2
1	0	X	0	0	0	1	1	Error	Features	1,2
1	0	X	0	0	1	0	2	Sector Count	Sector Count	
1	0	X	0	0	1	1	3	Sector No.	Sector No.	
1	0	X	0	1	0	0	4	Cylinder Low	Cylinder Low	
1	0	X	0	1	0	1	5	Cylinder High	Cylinder High	
1	0	X	0	1	1	0	6	Select Card/Head	Select Card/Head	
1	0	X	0	1	1	1	7	Status	Command	
1	0	X	1	0	0	0	8	Dup. Even RD Data	Dup. Even WR Data	2
1	0	X	1	0	0	1	9	Dup. Odd RD Data	Dup. Odd WR Data	2
1	0	X	1	1	0	1	D	Dup. Error	Dup. Features	2
1	0	X	1	1	1	0	E	Alt Status	Device Ctl	
1	0	X	1	1	1	1	F	Drive Address	Reserved	
1	1	X	X	X	X	0	8	Even RD Data	Even WR Data	3
1	1	X	X	X	X	1	9	Odd RD Data	Odd WR Data	3

T9-4.0 1316

1. Register 0 is accessed with CE1# low and CE2# low as a word register on the combined Odd Data Bus and Even Data Bus (D15-D0). This register may also be accessed by a pair of byte accesses to the offset 0 with CE1# low and CE2# high. Note that the address space of this word register overlaps the address space of the Error and Feature byte-wide registers that lie at offset 1. When accessed twice as byte register with CE1# low, the first byte to be accessed is the Even Byte of the word and the second byte accessed is the Odd Byte of the equivalent word access.
A byte access to address 0 with CE1# high and CE2# low accesses the error (read) or feature (write) register.

2. Registers at offset 8, 9 and D are non-overlapping duplicates of the registers at offset 0 and 1.
Register 8 is equivalent to register 0, while register 9 accesses the Odd Byte. Therefore, if the registers are byte accessed in the order 9 then 8 the data will be transferred Odd Byte then Even Byte.

   Repeated byte accesses to register 8 or 0 will access consecutive (Even then Odd) Bytes from the data buffer. Repeated word accesses to register 8, 9 or 0 will access consecutive words from the data buffer. Repeated byte accesses to register 9 are not supported. However, repeated alternating byte accesses to registers 8 then 9 will access consecutive (Even then Odd) Bytes from the data buffer. Byte accesses to register 9 access only the Odd Byte of the data.

3. Accesses to even addresses between 400H and 7FFH access register 8. Accesses to odd addresses between 400H and 7FFH access register 9. This 1 KByte memory window to the data register is provided so that hosts can perform memory to memory block moves to the data register when the register lies in memory space.

   Some hosts, such as the X86 processors, must increment both the source and destination addresses when executing the memory to memory block move instruction. Some PCMCIA socket adapters also have auto incrementing address logic embedded within them. This address window allows these hosts and adapters to function efficiently.

   Note that this entire window accesses the Data register FIFO and does not allow random access to the data buffer within the CompactFlash card. A word access to address at offset 8 will provide even data on the low-order byte of the data bus, along with odd data at offset 9 on the high-order byte of the data bus.

9.1.4 True IDE Mode Addressing

When the CompactFlash card is configured in the True IDE mode, the I/O decoding is as follows:

TABLE   9-5:True IDE Mode I/O Decoding

CE2#	CE1#	A_2	A_1	A_0	IORD#=0	IOWR#=0
1	0	0	0	0	RD Data	WR Data
1	0	0	0	1	Error register	Features
1	0	0	1	0	Sector Count	Sector Count
1	0	0	1	1	Sector No.	Sector No.
1	0	1	0	0	Cylinder Low	Cylinder Low
1	0	1	0	1	Cylinder High	Cylinder High
1	0	1	1	0	Select Card/Head	Select Card/Head
1	0	1	1	1	Status	Command
0	1	1	1	0	Alt Status	Device Control

T9-5.0 1316

9.1.5 CF-ATA Registers

The following section describes the hardware registers used by the host software to issue commands to the CompactFlash device. These registers are often collectively referred to as the "task file."

Note: In accordance with the PCMCIA specification: each of the registers below which is located at an odd offset address may be accessed at its normal address and also the corresponding even address (normal address -1) using data bus lines (D15-D8) when CE1# is high and CE2# is low unless IOIS16# is high (not asserted) and an I/O cycle is being performed.

9.1.5.1 Data Register (Address - 1F0H[170H];Offset 0,8,9)

The Data register is a 16 bit register, and it is used to transfer data blocks between the CompactFlash card data buffer and the Host. This register overlaps the Error register. The table below describes the combinations of data register access and is provided to assist in understanding the overlapped Data register and Error/Feature register rather than to attempt to define general PCMCIA word and byte access modes and operations. See the PCMCIA PC Card Standard Release 2.0 for definitions of the Card Accessing Modes for I/O and Memory cycles.

Note: Because of the overlapped registers, access to the 1F1H, 171H or offset 1 are not defined for word (CE2#=0 and CE1#=0) operations. These accesses are treated as accesses to the Word Data register. The duplicated registers at offsets 8, 9 and DH have no restrictions on the operations that can be performed by the socket.

Data Register	CE2#	CE1#	A_0	Offset	Data Bus
Word Data Register	0	0	X	0,8,9	$D_{15}-D_0$
Even Data Register	1	0	0	0,8	D_7-D_0
Odd Data Register	1	0	1	9	D_7-D_0
Odd Data Register	0	1	X	8,9	$D_{15}-D_8$
Error / Feature Register	1	0	1	1, DH	D_7-D_0
Error / Feature Register	0	1	X	1	$D_{15}-D_8$
Error / Feature Register	0	0	X	DH	$D_{15}-D_8$

Advance Information

9.1.5.2 Error Register (Address - 1F1H[171H]; Offset 1, 0DH Read Only)
This register contains additional information about the source of an error when an error is indicated in bit 0 of the Status register. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BBK	UNC	0	IDNF	0	ABRT	0	AMNF	**0000 0000b**

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with CE2# low and CE1# high.

Symbol	Function
Bit 7 (BBK)	This bit is set when a Bad Block is detected.
Bit 6 (UNC)	This bit is set when an Uncorrectable Error is encountered.
Bit 5	This bit is 0.
Bit 4 (IDNF)	The requested sector ID is in error or cannot be found.
Bit 3	This bit is 0.
Bit 2 (Abort)	This bit is set if the command has been aborted because of a CompactFlash card status condition: (Not Ready, Write Fault, etc.) or when an invalid command has been issued. It is required that the host retry any media access command (such as Read-Sectors and Write-Sectors) that ends with an error condition.
Bit 1	This bit is 0.
Bit 0 (AMNF)	This bit is set in case of a general error. It is required that the host retry any media access command (such as Read-Sectors and Write-Sectors) that ends with an error condition.

9.1.5.3 Feature Register (Address - 1F1H[171H]; Offset 1, 0DH Write Only)
This register provides information regarding features of the CompactFlash card that the host can utilize. This register is also accessed on data bits D15-D8 during a write operation to Offset 0 with CE2# low and CE1# high.

9.1.5.4 Sector Count Register (Address - 1F2H[172H]; Offset 2)
This register contains the numbers of sectors of data requested to be transferred on a read or write operation between the host and the CompactFlash card. If the value in this register is zero, a count of 256 sectors is specified. If the command was successful, this register is zero at command completion. If not successfully completed, the register contains the number of sectors that need to be transferred in order to complete the request.

9.1.5.5 Sector Number (LBA 7-0) Register (Address - 1F3H[173H]; Offset 3)
This register contains the starting sector number or bits 7-0 of the Logical Block Address (LBA) for any CompactFlash card data access for the subsequent command.

9.1.5.6 Cylinder Low (LBA 15-8) Register (Address - 1F4H[174H]; Offset 4)
This register contains the low order 8 bits of the starting cylinder address or bits 15-8 of then Logical Block Address.

9.1.5.7 Cylinder High (LBA 23-16) Register (Address - 1F5H[175H]; Offset 5)
This register contains the high order bits of the starting cylinder address or bits 23-16 of the Logical Block Address.

This register is also accessed on data bits D15-D8 during a write operation to offset 0 with CE2# low and CE1# high.

9.1.5.8 Drive/Head (LBA 27-24) Register (Address 1F6H[176H]; Offset 6)

The Drive/Head register is used to select the drive and head. It is also used to select LBA addressing instead of cylinder/head/sector addressing. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
1	LBA	1	DRV	HS3	HS2	HS1	HS0	**1010 0000b**

Symbol	Function
Bit 7	This bit is set to 1.
Bit 6	LBA is a flag to select either Cylinder/Head/Sector (CHS) or Logical Block Address mode (LBA). When LBA=0, Cylinder/Head/Sector mode is selected. When LBA=1, Logical Block Address is selected. In Logical Block mode, the Logical Block Address is interpreted as follows:

LBA7-LBA0: Sector Number register D7-D0.

LBA15-LBA8: Cylinder Low register D7-D0.

LBA23-LBA16: Cylinder High register D7-D0.

LBA27-LBA24: Drive/Head register bits HS3-HS0.

Symbol	Function
Bit 5	This bit is set to 1.
Bit 4 (DRV)	DRV is the drive number. When DRV=0, drive (card) 0 is selected. When DRV=1, drive (card) 1 is selected. The CompactFlash card is set to be Card 0 or 1 using the copy field (Drive #) of the PCMCIA Socket & Copy configuration register.
Bit 3 (HS3)	When operating in the Cylinder, Head, Sector mode, this is bit 3 of the head number. It is Bit 27 in the Logical Block Address mode.
Bit 2 (HS2)	When operating in the Cylinder, Head, Sector mode, this is bit 2 of the head number. It is Bit 26 in the Logical Block Address mode.
Bit 1 (HS1)	When operating in the Cylinder, Head, Sector mode, this is bit 1 of the head number. It is Bit 25 in the Logical Block Address mode.
Bit 0 (HS0)	When operating in the Cylinder, Head, Sector mode, this is bit 0 of the head number. It is Bit 24 in the Logical Block Address mode.

9.1.5.9 Status & Alternate Status Registers (Address 1F7H[177H]&3F6H[376H]; Offsets 7 & E)

These registers return the CompactFlash card status when read by the host. Reading the Status register does clear a pending interrupt while reading the Auxiliary Status register does not. The meaning of the status bits are described as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
BUSY	RDY	DWF	DSC	DRQ	CORR	0	ERR	**1000 0000b**

Symbol	Function
Bit 7 (BUSY)	The busy bit is set when the CompactFlash card has access to the command buffer and registers and the host is locked out from accessing the command register and buffer. No other bits in this register are valid when this bit is set to a 1.
Bit 6 (RDY)	RDY indicates whether the device is capable of performing CompactFlash card operations. This bit is cleared at power up and remains cleared until the CompactFlash card is ready to accept a command.
Bit 5 (DWF)	This bit, if set, indicates a write fault has occurred.
Bit 4 (DSC)	This bit is set when the CompactFlash card is ready.
Bit 3 (DRQ)	The Data Request is set when the CompactFlash card requires that information be transferred either to or from the host through the Data register.
Bit 2 (CORR)	This bit is set when a Correctable data error has been encountered and the data has been corrected. This condition does not terminate a multi-sector read operation.
Bit 1 (IDX)	This bit is always set to 0.
Bit 0 (ERR)	This bit is set when the previous command has ended in some type of error. The bits in the Error register contain additional information describing the error. It is required that the host retry any media access command (such as Read Sectors and Write Sectors) that ends with an error condition.

9.1.5.10 Device Control Register (Address - 3F6H[376H]; Offset E)

This register is used to control the CompactFlash card interrupt request and to issue an ATA soft reset to the card. This register can be written even if the device is BUSY. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
X	X	X	X	X	SW Rst	-IEn	0	**0000 1000b**

Symbol	Function
Bits 7-3	These bits are ignored by the CompactFlash card.
Bit 2 (SW Rst)	This bit is set to 1 in order to force the CompactFlash card to perform an ATA Disk controller Soft Reset operation. This does not change the PCMCIA Card Configuration registers (Sections 8.2 to 8.4) as a hardware reset does. The card remains in Reset until this bit is reset to '0.'
Bit1(-IEn)	The Interrupt Enable bit enables interrupts when the bit is 0. When the bit is 1, interrupts from the CompactFlash card are disabled. This bit also controls the Int bit in the Configuration and Status register. This bit is set to 0 at Power-on and Reset.
Bit0	This bit is ignored by the CompactFlash card.

9.1.5.11 Card (Drive) Address Register (Address3F7H[377H]; Offset F)
This register is provided for compatibility with the AT disk drive interface. It is recommended that this register not be mapped into the host's I/O space because of potential conflicts on Bit 7. The bits are defined as follows:

D7	D6	D5	D4	D3	D2	D1	D0	**Reset Value**
X	-WTG	-HS3	-HS2	-HS1	-HS0	-nDS1	-nDS0	**x111 1110b**

Symbol	Function
Bit 7	X = don't care

Implementation Note:

Conflicts may occur on the host data bus when this bit is provided by a Floppy Disk Controller operating at the same addresses as the CompactFlash card. Following are some possible solutions to this problem for the PCMCIA implementation:

1. Locate the CompactFlash card at a non-conflicting address, i.e. Secondary address (377) or in an independently decoded Address Space when a Floppy Disk Controller is located at the Primary addresses.

2. Do not install a Floppy and a CompactFlash card in the system at the same time.

3. Implement a socket adapter which can be programmed to (conditionally) tri-state D7 of I/0 address 3F7H/377H when a CompactFlash card is installed and conversely to tri-state D_6-D_0 of I/O address 3F7H/377H when a floppy controller is installed.

4. Do not use the CompactFlash card's Drive Address register. This may be accomplished by either a) If possible, program the host adapter to enable only I/O addresses 1F0H-1F7H, 3F6H (or 170H-177H, 176H) to the CompactFlash card or b) if provided use an additional Primary/Secondary configuration in the CompactFlash card which does not respond to accesses to I/O locations 3F7H and 377H. With either of these implementations, the host software must not attempt to use information in the Drive Address register.

Bit 6 (-WTG)	This bit is 0 when a write operation is in progress, otherwise, it is 1.
Bit 5 (-HS3)	This bit is the negation of bit 3 in the Drive/Head register.
Bit 4 (-HS2)	This bit is the negation of bit 2 in the Drive/Head register.
Bit 3 (-HS1)	This bit is the negation of bit 1 in the Drive/Head register.
Bit 2 (-HS0)	This bit is the negation of bit 0 in the Drive/Head register.
Bit 1 (-nDS1)	This bit is 0 when drive 1 is active and selected.
Bit 0 (-nDS0)	This bit is 0 when the drive 0 is active and selected.

9.2 CF-ATA Command Description

This section defines the software requirements and the format of the commands the host sends to the Compact-Flash cards. Commands are issued to the CompactFlash card by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register. The manner in which a command is accepted varies. There are three classes (see Table 9-6) of command acceptance, all dependent on the host not issuing commands unless the CompactFlash card is not busy (BSY=0).

Table 9-6 summarizes the CF-ATA command set with the paragraphs that follow describing the individual commands and the task file for each.

Advance Information

TABLE   9-6: CF-ATA Command Set

Class	Command	Code	FR[1]	SC[2]	SN[3]	CY[4]	DH[5]	LBA[6]
1	Check-Power-mode	E5H or 98H	-	-	-	-	D	-
1	Execute-Drive-Diagnostic	90H	-	-	-	-	D	-
1	Erase-Sector(s)	C0H	-	Y[7]	Y	Y	Y[8]	Y
1	Flush-Cache	E7H	-	-	-	-	D	-
2	Format-Track	50H	-	Y	-	Y	Y	Y
1	Identify-Drive	ECH	-	-	-	-	D	-
1	Idle	E3H or 97H	-	Y	-	-	D	-
1	Idle-Immediate	E1H or 95H	-	-	-	-	D	-
1	Initialize-Drive-Parameters	91H	-	Y	-	-	Y	-
1	NOP	00H	-	-	-	-	D	-
1	Read-Buffer	E4H	-	-	-	-	D	-
1	Read-Multiple	C4H	-	Y	Y	Y	Y	Y
1	Read-Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
1	Read-Verify-Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH	-	-	-	-	D	-
1	Request-Sense	03H	-	-	-	-	D	-
1	Seek	7XH	-	-	Y	Y	Y	Y
1	Set-Features	EFH	Y	-	-	-	D	-
1	Set-Multiple-mode	C6H	-	Y	-	-	D	-
1	Set-Sleep-mode	E6H or 99H	-	-	-	-	D	-
1	Stand-By	E2H or 96H	-	-	-	-	D	-
1	Stand-By-Immediate	E0H or 94H	-	-	-	-	D	-
1	Translate-Sector	87H	-	Y	Y	Y	Y	Y
2	Write-Buffer	E8H	-	-	-	-	D	-
3	Write-Multiple	C5H	-	Y	Y	Y	Y	Y
3	Write-Multiple-w/o-Erase	CDH	-	Y	Y	Y	Y	Y
2	Write-Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
2	Write-Sector(s)-w/o-Erase	38H	-	Y	Y	Y	Y	Y
3	Write-Verify	3CH	-	Y	Y	Y	Y	Y

T9-6.0 1316

1. FR = Features register
2. SC = Sector Count register
3. SN = Sector Number register
4. CY = Cylinder registers
5. DH = Card/Drive/Head register
6. LBA = Logical Block Address mode Supported (see command descriptions for use).
7. Y = The register contains a valid parameter for this command.
8. For the Drive/Head register: Y - both the CompactFlash card and head parameters are used;
          D - only the CompactFlash card parameter is valid and not the head parameter.

9.2.1 Check-Power-Mode - 98H or E5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	98H or E5H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command checks the power mode.

Because the CompactFlash card controller can recover from sleep in 200 ns, the device always enters power-saving mode when a command is completed. CompactFlash card controller sets BSY, sets the Sector Count register to 00H, clears BSY, and generates an interrupt.

9.2.2 Execute Drive Diagnostic - 90H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	90H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command performs the internal diagnostic tests implemented by the CompactFlash card.

If in PCMCIA configuration this command runs only on the CompactFlash card which is addressed by the Drive/Head register when the diagnostic command is issued. This is because PCMCIA card interface does not allows for direct inter-drive communication (such as the ATA PDIAG# and DASP# signals). If in True IDE mode the Drive bit is ignored and the diagnostic command is executed by both the master and the slave with the master responding with status for both devices.

The Diagnostic codes shown in Table 9-7 are returned in the Error register at the end of the command.

TABLE 9-7: Diagnostic Codes

Code	Error Type
01H	No Error Detected
02H	Formatter Device Error
03H	Sector Buffer Error
04H	ECC Circuitry Error
05H	Controlling Microprocessor Error
8XH	Slave Error in True IDE mode

T9-7.0 1316

Advance Information

9.2.3 Erase-Sector(s) - C0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C0H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

The use of this command is not recommended. This command is effectively a no operation, but it is supported for backward compatibility.

9.2.4 Flush-Cache - E7H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E7H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card controller to complete writing data from its cache. The CompactFlash card controller then clears BSY and generates an interrupt.

9.2.5 Format-Track - 50H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	50H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is accepted for host backward compatibility. The CompactFlash card controller expects a sector buffer of data from the host to follow the command with the same protocol as the Write-Sector(s) command although the information in the buffer is not used by the CompactFlash card controller. The use of this command is not recommended.

9.2.6 Identify-Drive - ECH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	ECH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Identify-Drive command enables the host to receive parameter information from the CompactFlash card controller. This command has the same protocol as the Read-Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 9-8. All reserved bits or words are zero. Table 9-8 gives the definition for each field in the Identify-Drive information.

TABLE   9-8:   Identify-Drive Information (1 of 2)

Word Address	Default Value	Total Bytes	Data Field Type Information
0	848AH	2	General configuration bit-significant information
1	bbbbH[1]	2	Default number of cylinders
2	0000H	2	Reserved
3	bbbbH[1]	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	0000H	2	Number of unformatted bytes per sector
6	bbbbH[1]	2	Default number of sectors per track
7-8	nnnnH[2]	4	Number of sectors per card (Word 7 = MSW, Word 8 = LSW)
9	xxxxH	2	Vendor Unique
10-14	eeeeH[3]	10	User-programmable serial number in ASCII
15-19	ddddH[4]	10	SST preset, unique ID in ASCII
20	0002H	2	Buffer type
21	nnnnH[2]	2	Buffer size in 512 Byte increments
22	0004H	2	# of ECC bytes passed on Read/Write Long Commands
23-26	aaaaH[5]	8	Firmware revision in ASCII. Big Endian Byte Order in Word
27-46	ccccH[6]	40	Model number in ASCII. Big Endian Byte Order in Word
47	0001H	2	Maximum number of sectors on Read/Write Multiple command
48	0000H	2	Reserved
49	0A00H	2	Capabilities
50	0000H	2	Reserved
51	0200H	2	PIO data transfer cycle timing mode
52	0000H	2	Reserved
53	0003H	2	Translation parameters are valid
54	nnnnH[2]	2	Current numbers of cylinders
55	nnnnH[2]	2	Current numbers of heads
56	nnnnH[2]	2	Current sectors per track
57-58	nnnnH[2]	4	Current capacity in sectors (LBAs) (Word 57 = LSW, Word 58 = MSW)

Advance Information

TABLE 9-8:   Identify-Drive Information (Continued) (2 of 2)

Word Address	Default Value	Total Bytes	Data Field Type Information
59	0100H	2	Multiple sector setting
60-61	nnnnH[2]	4	Total number of sectors addressable in LBA mode
62-63	0000H	4	Reserved (DMA data transfer is not supported in CompactFlash)
64	0003H	2	Advanced PIO Transfer mode supported
65-66	0000H	4	Reserved
67	0078H	2	Minimum PIO transfer cycle time without flow control
68	0078H	2	Minimum PIO transfer cycle time with IORDY flow control
69-79	0000H	22	Reserved
80-81	0000H	4	CF card will not return ATA revision value
82	7068H	2	Features/command sets supported
83	4004H	2	Features/command sets supported
84	4000H	2	Features/command sets supported
85-87	xxxxH	6	Features/command sets enabled
88-128	0000H	82	Reserved
129-159	xxxxH	62	Vendor unique bytes
160-255	0000H	192	Reserved

T9-8.0 1316

1. bbbb - default value set by controller. The selections could be user (manufacturer) programmable.
2. nnnn - calculated data based on product configuration
3. eeee - the default value is 2020H
4. dddd - unique number of each device
5. aaaa - any unique SST firmware revision
6. cccc - default value is "xxxx MB CompactFlash Card"

9.2.6.1 Word 0: General Configuration
This field informs the host that this is a non-magnetic, hard sectored, removable storage device with a transfer rate greater than 10 MByte/sec and is not MFM encoded.

9.2.6.2 Word 1: Default Number of Cylinders
This field contains the number of translated cylinders in the default translation mode. This value will be the same as the number of cylinders.

9.2.6.3 Word 3: Default Number of Heads
This field contains the number of translated heads in the default translation mode.

9.2.6.4 Word 4: Number of Unformatted Bytes per Track
This field contains the number of sectors per track in the default translation mode.

9.2.6.5 Word 5: Number of Unformatted Bytes per Sector
This field contains the number of sectors per CompactFlash card controller. This double word value is also the first invalid address in LBA translation mode. This field is only required by CF feature set support.

9.2.6.6 Word 6: Default Number of Sectors per Track
This field contains the number of sectors per track in the default translation mode.

9.2.6.7 Word 7-8: Number of Sectors per Card
This field contains the number of sectors per CompactFlash card. This double word value is also the first invalid address in LBA translation mode.

9.2.6.8 Word 10-19: Memory Card Serial Number
The contents of this field are right justified and padded with spaces (20H). The right-most ten bytes are an SST preset, unique ID. The left-most ten bytes are a user-programmable value with a default value of spaces

9.2.6.9 Word 20: Buffer Type
This field defines the buffer capability:

0002H: a dual ported multi-sector buffer capable of simultaneous data transfers to or from the host and the CompactFlash card controller.

9.2.6.10 Word 21: Buffer Size
This field defines the buffer capacity in 512 Byte increments. SST's CompactFlash card controller has up to 8 sector data buffer for host interface.

9.2.6.11 Word 22: ECC Count
This field defines the number of ECC bytes used on each sector in the Read and Write Long commands.

9.2.6.12 Word 23-26: Firmware Revision
This field contains the revision of the firmware for this product.

9.2.6.13 Word 27-46: Model Number
This field contains the model number for this product and is left justified and padded with spaces (20H).

9.2.6.14 Word 47: Read/Write Multiple Sector Count
This field contains the maximum number of sectors that can be read or written per interrupt using the Read Multiple or Write Multiple commands. SST's CompactFlash card controller can support up to 2 sectors for Read-Multiple or Write-Multiple commands.

9.2.6.15 Word 49: Capabilities

Bit	Function
13	Standby Timer 0: forces sleep mode when host is inactive.
11	IORDY Support 1: CompactFlash card controller supports PIO Mode-4.
9	LBA support 1: CompactFlash card controller supports LBA mode addressing.
8	DMA Support 0: DMA mode is not supported.

9.2.6.16 Word 51: PIO Data Transfer Cycle Timing Mode
This field defines the mode for PIO data transfer. CompactFlash card controller supports up to PIO Mode-4.

9.2.6.17 Word 53: Translation Parameters Valid

Bit	Function
0	1: words 54-58 are valid and reflect the current number of cylinders, heads and sectors.
1	1: words 64-70 are valid to support PIO Mode-4.

9.2.6.18 Word 54-56: Current Number of Cylinders, Heads, Sectors/Track
These fields contains the current number of user addressable Cylinders, Heads, and Sectors/Track in the current translation mode.

Advance Information

9.2.6.19 Word 57-58: Current Capacity
This field contains the product of the current cylinders times heads times sectors.

9.2.6.20 Word 59: Multiple Sector Setting
This field contains a validity flag in the Odd Byte and the current number of sectors that can be transferred per interrupt for R/W Multiple in the Even Byte. The Odd Byte is always 01H which indicates that the Even Byte is always valid.

The Even Byte value depends on the value set by the Set Multiple command. The Even Byte of this word by default contains a 00H which indicates that R/W Multiple commands are not valid.

9.2.6.21 Word 60-61: Total Sectors Addressable in LBA Mode
This field contains the number of sectors addressable for the CompactFlash card controller in LBA mode only.

9.2.6.22 Word 62-63: Multi-word DMA Transfer Mode
Multi-word DMA Transfer mode is not supported.

9.2.6.23 Word 64: Advanced PIO Data Transfer Mode

Bit	Function
0	1: CompactFlash card controller supports PIO Mode-3.
1	1: CompactFlash card controller supports PIO Mode-4.

9.2.6.24 Word 65-66: Multi-word DMA Transfer Mode
Multi-word DMA Transfer mode is not supported.

9.2.6.25 Word 67: Minimum PIO Transfer Cycle Time Without Flow Control
The CompactFlash card controller minimum cycle time is 120 ns.

9.2.6.26 Word 68: Minimum PIO Transfer Cycle Time With IORDY
The CompactFlash card controller minimum cycle time is 120 ns, e.g., PIO Mode-4.

9.2.6.27 Words 82-84: Features/command sets supported

Words 82, 83, and 84 indicate the features and command sets supported.

Word 82

Bit	Function
15	0: Obsolete
14	1: NOP command is supported
13	1: Read Buffer command is supported
12	1: Write Buffer command is supported
11	0: Obsolete
10	0: Host Protected Area feature set is not supported
9	0: Device Reset command is not supported
8	0: Service interrupt is not supported
7	0: Release interrupt is not supported
6	1: Look-ahead is supported
5	1: Write cache is supported
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	0: Security Mode feature set is not supported
0	0: SMART feature set is not supported

Word 83

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are not valid
14	1: Provides indication that the features/command sets supported words are valid
13-9	0: Reserved
8	0: Set-Max security extension is not supported
7-5	0: Reserved
4	0: Removable Media Status feature set is not supported
3	0: Advanced Power Management feature set is not supported
2	1: CFA feature set is supported
1	0: Read DMA Queued and Write DMA Queued commands are not supported
0	0: Download Microcode command is not supported

Word 84

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

Advance Information

9.2.6.28 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 indicate features/command sets enabled.

The host can enable/disable the features or command set only if they are supported in Words 82-84.

Word 85

Bit	Function
15	0: Obsolete
14	0: NOP command is not enabled 1: NOP command is enabled
13	0: Read Buffer command is not enabled 1: Read Buffer command is enabled
12	0:Write Buffer command is not enabled 1: Write Buffer command is enabled
11	0: Obsolete
10	0: Host Protected Area feature set is not enabled
9	0: Device Reset command is not enabled
8	0: Service interrupt is not enabled
7	0: Release interrupt is not enabled
6	0: Look-ahead is not enabled 1: Look-ahead is enabled
5	0: Write cache is not enabled 1: Write cache is enabled
4	0: Packet Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Removable Media feature set is not supported
1	0: Security Mode feature set is not supported
0	0: SMART feature set is not enabled

Word 86

Bit	Function
15-9	0: Reserved
8	0: Set-Max security extension is not enabled
7-5	0: Reserved
4	0: Removable Media Status feature set is not enabled
3	0: Advanced Power Management feature set is not enabled via the Set Features command
2	1: CFA feature set is enabled
1	0: Read DMA Queued and Write DMA Queued commands are not enabled
0	0: Download Microcode command is not enabled

Word 87

The values in this word should not be depended on by host implementers.

Bit	Function
15	0: Provides indication that the features/command sets supported words are valid
14	1: Provides indication that the features/command sets supported words are valid
13-0	0: Reserved

9.2.6.29 Idle - 97H or E3H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	97H or E3H							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Timer Count (5 msec increments)							
Feature (1)	X							

This command causes the CompactFlash card controller to set BSY, enter the Idle mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic Power-down mode is enabled. If the sector count is zero, the automatic Power-down mode is also enabled, the timer count is set to 1, with each count being 5 ms. Note that this time base (5 msec) is different from the ATA specification.

9.2.6.30 Idle-Immediate - 95H or E1H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	95H or E1H							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card controller to set BSY, enter the Idle mode, clear BSY and generate an interrupt.

Advance Information

9.2.6.31 Initialize-Drive-Parameters - 91H

Bit ->	7	6	5	4	3	2	1	0
Command (7)				91H				
C/D/H (6)	X	0	X	Drive	Max Head (no. of heads-1)			
Cyl High (5)				X				
Cyl Low (4)				X				
Sec Num (3)				X				
Sec Cnt (2)				Number of Sectors				
Feature (1)				X				

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Drive/Head registers are used by this command.

9.2.6.32 NOP - 00H

Bit ->	7	6	5	4	3	2	1	0
Command (7)				00H				
C/D/H (6)		X		Drive		X		
Cyl High (5)				X				
Cyl Low (4)				X				
Sec Num (3)				X				
Sec Cnt (2)				X				
Feature (1)				X				

This command always fails with the CompactFlash card controller returning command aborted.

9.2.6.33 Read-Buffer - E4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)				E4H				
C/D/H (6)		X		Drive		X		
Cyl High (5)				X				
Cyl Low (4)				X				
Sec Num (3)				X				
Sec Cnt (2)				X				
Feature (1)				X				

The Read-Buffer command enables the host to read the current contents of the CompactFlash card controller's sector buffer. This command has the same protocol as the Read-Sector(s) command

9.2.6.34 Read-Multiple - C4H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C4H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the CompactFlash card controller can support up to a block count of 1 as indicated in the Identify-Drive Command information.

The Read-Multiple command is similar to the Read-Sector(s) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a Set Multiple command.

Command execution is identical to the Read-Sectors operation except that the number of sectors defined by a Set Multiple command are transferred without intervening interrupts. DRQ qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple-Mode command, which must be executed prior to the Read-Multiple command. When the Read-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where

n = remainder (sector count/block count).

If the Read-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Read-Multiple commands are disabled, the Read-Multiple operation is rejected with an Aborted Command error. Disk errors encountered during Read-Multiple commands are posted at the beginning of the block or partial block transfer, but DRQ is still set and the data transfer will take place as it normally would, including transfer of corrupted data, if any.

Interrupts are generated when DRQ is set at the beginning of each block or partial block. The error reporting is the same as that on a Read-Sector(s) command. This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read.

If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block which contained the error.

Advance Information

9.2.6.35 Read-Sector(s) - 20H or 21H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	20H or 21H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is issued and after each sector of data (except the last one) has been read by the host, the CompactFlash card controller sets BSY, puts the sector of data in the buffer, sets DRQ, clears BSY, and generates an interrupt. The host then reads the 512 Bytes of data from the buffer.

At command completion, the Command Block registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block registers contain the cylinder, head, and sector number of the sector where the error occurred. The flawed data is pending in the sector buffer.

9.2.6.36 Read-Verify-Sector(s) - 40H or 41H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	40H or 41H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is identical to the Read-Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash card controller sets BSY.

When the requested sectors have been verified, the CompactFlash card controller clears BSY and generates an interrupt. Upon command completion, the Command Block registers contain the cylinder, head, and sector number of the last sector verified.

If an error occurs, the verify terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count register contains the number of sectors not yet verified.

9.2.6.37 Recalibrate - 1XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	1XH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a no operation, and is provided for compatibility purposes.

Advance Information

9.2.6.38 Request-Sense - 03H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	03H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command requests extended error information for the previous command. Table 9-9 defines the valid extended error codes for the CompactFlash card controller. The extended error code is returned to the host in the Error register.

TABLE   9-9:   Extended Error Codes

Extended Error Code	Description
00H	No Error Detected
01H	Self Test OK (No Error)
09H	Miscellaneous Error
20H	Invalid Command
21H	Invalid Address (Requested Head or Sector Invalid)
2FH	Address Overflow (Address Too Large)
35H, 36H	Supply or generated Voltage Out of Tolerance
11H	Uncorrectable ECC Error
18H	Corrected ECC Error
05H, 30-34H, 37H, 3EH	Self Test or Diagnostic Failed
10H, 14H	ID Not Found
3AH	Spare Sectors Exhausted
1FH	Data Transfer Error / Aborted Command
0CH, 38H, 3BH, 3CH, 3FH	Corrupted Media Format
03H	Write / Erase Failed

T9-9.0 1316

9.2.6.39 Seek - 7XH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	7XH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	X (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command is effectively a no operation, although it does perform a range check of cylinder and head or LBA address, and returns an error if the address is out of range.

9.2.6.40 Set-Features - EFH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	EFH							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Config							
Feature (1)	Feature							

This command is used by the host to establish or select certain features. Table 9-10 defines all features that are supported.

TABLE 9-10:   Features Supported

Feature	Operation
01H	Enable 8-bit data transfers.
02H[1]	Enable Write cache
03H	Set transfer mode based on value in Sector Count register. Table 9-11 defines the values.
09H	Enable Extended Power Operations
0AH	NOP - Accepted for backward compatibility.
55H[1]	Disable Read Look Ahead.
66H	Disable Power-on Reset (POR) establishment of defaults at software reset.
69H	NOP - Accepted for backward compatibility.
81H	Disable 8-bit data transfer.
82H[1]	Disable Write Cache
89H	Disable Extended Power operations
8AH	NOP - Accepted for backward compatibility.
96H	NOP - Accepted for backward compatibility.
97H	Accepted for backward compatibility. Use of this Feature is not recommended.
9AH[2]	Set the host current source capability Allows trade-off between current drawn and Read/Write speed
BBH	4 Bytes of data apply on Read/Write-Long-Sector commands.
AAH	Enable Read-Look-Ahead
CCH	Enable Power-on Reset (POR) establishment of defaults at software reset.

T9-10.0 1316

1. SST CompactFlash card controller does not implement cache operations.
   These commands are returned with no error.
2. SST CompactFlash card controller has fixed power consumption.
   The command will be accepted and returned with no error.

Advance Information

Features 01H and 81H are used to enable and clear 8-bit data transfer mode. If the 01H feature command is issued all data transfers will occur on the low order D_7-D_0 data bus and the IOCS16# signal will not be asserted for data register accesses.

Feature 03H allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. One PIO mode is selected at all times. The host may change the selected modes by the Set-Features command.

TABLE9-11:Transfer Mode Values

Mode	Bits [7:3]	Bits [2:0]
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode[1]
Reserved	Other	N/A

T9-11.0 1316

1. Mode = transfer mode number, all other values are not valid

Features 66H and CCH can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

9.2.6.41 Set-Multiple-Mode - C6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C6H							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command enables the CompactFlash card controller to perform Read and Write-Multiple operations and establishes the block count for these commands. The Sector Count register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash card controller sets BSY to 1 and checks the Sector Count register.

If the Sector Count register contains a valid value (see Section 9.2.6.14 for details) and the block count is supported, the value is loaded for all subsequent Read-Multiple and Write-Multiple commands and execution of those commands is enabled. If a block count is not supported, an Aborted Command error is posted, and Read-Multiple and Write-Multiple commands are disabled. If the Sector Count register contains 0 when the command is issued, Read and Write-Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write-Multiple disabled.

9.2.6.42 Set-Sleep-Mode - 99H or E6H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	99H or E6H							
C/D/H (6)		X		Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card controller to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 15 milliseconds.

Advance Information

9.2.6.43 Standby - 96H or E2H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	96H or E2H							
C/D/H (6)		X		Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card controller to set BSY, enter the Sleep mode (which corresponds to the ATA Standby mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

9.2.6.44 Standby-Immediate - 94H or E0H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	94H or E0H							
C/D/H (6)		X		Drive		X		
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

This command causes the CompactFlash card controller to set BSY, enter the Sleep mode (which corresponds to the ATA "Standby" mode), clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

9.2.6.45 Translate-Sector - 87H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	87H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	X							
Feature (1)	X							

This command allows the host a method of determining the exact number of times a user sector has been erased and programmed. The controller responds with a 512 Byte buffer of information containing the desired cylinder, head, and sector, including its logical address, and the Hot Count, if available, for that sector. Table 9-12 represents the information in the buffer. Please note that this command is unique to the CompactFlash card controller.

TABLE 9-12: Translate-Sector Information

Address	Information
00H-01H	Cylinder MSB (00H), Cylinder LSB (01H)
02H	Head
03H	Sector
04H-06H	LBA MSB (04H) - LSB (06H)
07H-12H	Reserved
13H	Erased Flag (FFH) = Erased; 00H = Not Erased
14H-17H	Reserved
18H-1AH	Hot Count MSB (18H) - LSB (1AH)[1]
1BH-1FFH	Reserved

T9-12.0 1316

1. A value of 0 indicates Hot Count is not supported.

9.2.6.46 Write-Buffer - E8H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	E8H							
C/D/H (6)	X			Drive	X			
Cyl High (5)	X							
Cyl Low (4)	X							
Sec Num (3)	X							
Sec Cnt (2)	X							
Feature (1)	X							

The Write-Buffer command enables the host to overwrite contents of the CompactFlash card controller's sector buffer with any data pattern desired. This command has the same protocol as the Write-Sector(s) command and transfers 512 Bytes.

Advance Information

9.2.6.47 Write-Multiple - C5H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	C5H							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Note: The current revision of the CompactFlash card controller can support up to a block count of 1 as indicated in the Identify-Drive Command information.

This command is similar to the Write-Sectors command. The CompactFlash card controller sets BSY within 400 ns of accepting the command. Interrupts are not presented on each sector but on the transfer of a block which contains the number of sectors defined by Set Multiple. Command execution is identical to the Write-Sectors operation except that the number of sectors defined by the Set Multiple command is transferred without intervening interrupts.

DRQ qualification of the transfer is required only at the start of the data block, not on each sector. The block count of sectors to be transferred without intervening interrupts is programmed by the Set-Multiple-Mode command, which must be executed prior to the Write-Multiple command.

When the Write-Multiple command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested. If the number of requested sectors is not evenly divisible by the sector/block, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

$$n = \text{remainder (sector count/block)}.$$

If the Write-Multiple command is attempted before the Set-Multiple-Mode command has been executed or when Write-Multiple commands are disabled, the Write-Multiple operation will be rejected with an aborted command error.

Errors encountered during Write-Multiple commands are posted after the attempted writes of the block or partial block transferred. The Write command ends with the sector in error, even if it is in the middle of a block. Subsequent blocks are not transferred in the event of an error. Interrupts are generated when DRQ is set at the beginning of each block or partial block.

The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred and the Sector Count register contains the residual number of sectors that need to be transferred for successful completion of the command e.g. each block has 4 sectors, a request for 8 sectors is issued and an error occurs on the third sector. The Sector Count register contains 6 and the address is that of the third sector.

9.2.6.48 Write-Multiple-Without-Erase - CDH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	CDH							
C/D/H (6)	1	LBA	1	Drive	Head			
Cyl High (5)	Cylinder High							
Cyl Low (4)	Cylinder Low							
Sec Num (3)	Sector Number							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Use of this command is not recommended, but it is supported as Write-Multiple command for backward compatibility.

9.2.6.49 Write-Sector(s) - 30H or 31H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	30H or 31H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number register. When this command is accepted, the CompactFlash card controller sets BSY, then sets DRQ and clears BSY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY will be set and DRQ will be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It will remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

Advance Information

9.2.6.50 Write-Sector(s)-Without-Erase - 38H

Bit ->	7	6	5	4	3	2	1	0
Command (7)	38H							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

Use of this command is not recommended, but it is supported as the Write-Sector(s) command for backward compatibility.

9.2.6.51 Write-Verify - 3CH

Bit ->	7	6	5	4	3	2	1	0
Command (7)	3CH							
C/D/H (6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cyl High (5)	Cylinder High (LBA 23-16)							
Cyl Low (4)	Cylinder Low (LBA 15-8)							
Sec Num (3)	Sector Number (LBA 7-0)							
Sec Cnt (2)	Sector Count							
Feature (1)	X							

This command is similar to the Write-Sector(s) command, except each sector is verified immediately after being written. This command has the same protocol as the Write-Sector(s) command.

9.2.7 Error Posting

The following table summarizes the valid status and error value for all the CF-ATA Command set.

TABLE 9-13:Error and Status Register

Command	Error Register					Status Register				
	BBK	UNC	IDNF	ABRT	AMNF	DRDY	DWF	DSC	CORR	ERR
Check-Power-mode				V		V	V	V		V
Execute-Drive-Diagnostic[1]						V		V		V
Erase-Sector(s)	V		V	V	V	V	V	V		V
Flush-Cache				V		V	V	V		V
Format-Track			V	V	V	V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
Initialize-Drive-Parameters						V		V		V
NOP				V		V	V			V
Read-Buffer				V		V	V	V		V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sectors	V	V	V	V	V	V	V	V	V	V
Recalibrate				V		V	V	V		V
Request-Sense				V		V		V		V
Seek			V	V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Multiple-mode				V		V	V	V		V
Set-Sleep-mode				V		V	V	V		V
Stand-By				V		V	V	V		V
Stand-By-Immediate				V		V	V	V		V
Translate-Sector	V		V	V	V	V	V	V		V
Write-Buffer				V		V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Multiple -w/o-Erase	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Sector(s)-w/o-Erase	V		V	V	V	V	V	V		V
Write-Verify	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

T9-13.0 1316

1. See Table 9-7
Note: V = valid on this command

Advance Information

10.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Stress Ratings Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Temperature Under Bias . . . . -55°C to +125°C

Storage Temperature . . . . -65°C to +150°C

D.C. Voltage on Pins[1] I3, I4, O4, and O5 to Ground Potential . . . . -0.5V to V_{DD}+0.5V

Transient Voltage (<20 ns) on Pins[1] I3, I4, O4, and O5 to Ground Potential . . . . -2.0V to V_{DD}+2.0V

D.C. Voltage on Pins[1] I1, I2, O1, O2, and O6 to Ground Potential. . . . . -0.5V to V_{DDQ}+0.5V

Transient Voltage (<20 ns) on Pins[1] I1, I2, O1, O2, and O6 to Ground Potential. . . . . -2.0V to V_{DDQ}+2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Through Hole Lead Soldering Temperature (10 Seconds). . . . . 300°C

Surface Mount Solder Reflow Temperature . . . . 260°C for 10 seconds

Output Short Circuit Current[2] . . . . 50 mA

1. Please refer to Table 3-1 for pin assignment information.
2. Outputs shorted for no more than one second. No more than one output shorted at a time.

TABLE 10-1: Absolute Maximum Power Pin Stress Ratings

Parameter	Symbol	Conditions
Input Power	V_{DDQ} V_{DD}	-0.3V min to 6.5V max -0.3V min to 4.0V max
Voltage on any flash media interface pin with respect to V_{SS}		-0.5V min to V_{DD} + 0.5V max
Voltage on all other pins with respect to V_{SS}		-0.5V min to V_{DDQ} + 0.5V max

T10-1.0 1316

Operating Range

Range	Ambient Temperature	V_{DD}	V_{DDQ}
Commercial	0°C to +70°C	3.165-3.465V	4.5-5.5V; 3.165-3.465V
Industrial	-40°C to +85°C	3.165-3.465V	4.75-5.25V; 3.165-3.465V

AC Conditions of Test

Input Rise/Fall Time . . . . 10 ns
Output Load . . . . C_L = 100 pF
See Figure 10-1

Note: All AC specifications are guaranteed by design.

TABLE 10-2: Recommended System Power-on Timing

Symbol	Parameter	Typical	Maximum	Units
$T_{PU-INITIAL}$	Drive Initialization to Ready	3 sec + (0.5 sec/GByte)	50	sec
$T_{PU-READY1}$[1]	Host Power-on/Reset to Ready Operation		1000	ms
$T_{PU-WRITE1}$[1]	Host Power-on/Reset to Write Operation		1000	ms

T10-2.0 1316

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10-3: Capacitance (T$_A$ = 25°C, f=1 MHz, other pins open)

Parameter	Description	Test Condition	Maximum
C$_{I/O}$[1]	I/O Pin Capacitance	V$_{I/O}$ = 0V	15 pF
C$_{IN}$[1]	Input Capacitance	V$_{IN}$ = 0V	9 pF

T10-3.0 1316

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10-4: Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
I$_{LTH}$[1]	Latch Up	100 + I$_{DD}$	mA	JEDEC Standard 78

T10-4.0 1316

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

10.1 DC Characteristics

TABLE 10-5: DC Characteristics for Media Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
V$_{IH3}$	I3	Input Voltage	2.0		V	V$_{DD}$=V$_{DD}$ Max
V$_{IL3}$				0.8		V$_{DD}$=V$_{DD}$ Min
I$_{IL3}$	I3Z	Input Leakage Current	-10	10	uA	V$_{IN}$ = GND to V$_{DD}$, V$_{DD}$ = V$_{DD}$ Max
I$_{U3}$	I3U	Input Pull-Up Current	-8	-50	uA	V$_{IN}$ = GND, V$_{DD}$ = V$_{DD}$ Max
I$_{D3}$	I3D	Input Pull-Down Current	30	200	uA	V$_{IN}$ = V$_{DD}$, V$_{DD}$ = V$_{DD}$ Max
V$_{T+4}$	I4	Input Voltage Schmitt Trigger		2.5	V	V$_{DD}$ = V$_{DD}$ Max
V$_{T-4}$			0.75			V$_{DD}$ = V$_{DD}$ Min
I$_{IL4}$	I4Z	Input Leakage Current	-10	10	uA	V$_{IN}$ = GND to V$_{DD}$, V$_{DD}$ = V$_{DD}$ Max
I$_{U4}$	I4U	Input Pull-Up Current	-8	-50	uA	V$_{IN}$ = GND, V$_{DD}$ = V$_{DD}$ Max
V$_{OH4}$	O4	Output Voltage	2.4		V	I$_{OH4}$=I$_{OH4}$ Min
V$_{OL4}$				0.4		I$_{OL4}$=I$_{OL4}$ Max
I$_{OH4}$		Output Current	-1.5		mA	V$_{DD}$=V$_{DD}$ Min
I$_{OL4}$		Output Current		1.5	mA	V$_{DD}$=V$_{DD}$ Min
V$_{OH5}$	O5	Output Voltage	2.4		V	I$_{OH5}$=I$_{OH5}$ Min
V$_{OL5}$				0.4		I$_{OL5}$=I$_{OL5}$ Max
I$_{OH5}$		Output Current	-3		mA	V$_{DD}$=V$_{DD}$ Min
I$_{OL5}$		Output Current		3	mA	V$_{DD}$=V$_{DD}$ Min

T10-5.0 1316

Advance Information

TABLE   10-6: DC Characteristics for Host Interface

Symbol	Type	Parameter	Min	Max	Units	Conditions
V_{IH1}	I1	Input Voltage	2.0V		V	$V_{DDQ}=V_{DDQ}$ Max
V_{IL1}				0.8V		$V_{DDQ}=V_{DDQ}$ Min
I_{IL1}	I1Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U1}	I1U	Input Pull-Up Current	-110	-1	uA	V_{OUT} = GND, V_{DDQ} = V_{DDQ} Max
V_{T+2}	I2	Input Voltage Schmitt Trigger		2.0	V	$V_{DDQ}=V_{DDQ}$ Max
V_{T-2}				0.8		$V_{DDQ}=V_{DDQ}$ Min
I_{IL2}	I2Z	Input Leakage Current	-10	10	uA	V_{IN} = GND to V_{DDQ}, V_{DDQ} = V_{DDQ} Max
I_{U2}	I2U	Input Pull-Up Current	-110	-1	uA	V_{OUT} = GND, V_{DDQ} = V_{DDQ} Max
V_{OH1}	O1	Output Voltage	2.4		V	$I_{OH1}=I_{OH1}$ Min
V_{OL1}				0.4		$I_{OL1}=I_{OL1}$ Max
I_{OH1}		Output Current	-4		mA	$V_{DDQ}=V_{DDQ}$ Min
I_{OL1}		Output Current		4	mA	$V_{DDQ}=V_{DDQ}$ Min
V_{OH2}	O2	Output Voltage	2.4		V	$I_{OH2}=I_{OH2}$ Min
V_{OL2}				0.4		$I_{OL2}=I_{OL2}$ Max
I_{OH2}		Output Current	-6		mA	V_{DDQ}=3.135V-3.465V
I_{OL2}		Output Current		6	mA	V_{DDQ}=3.135V-3.465V
I_{OH2}		Output Current	-8		mA	V_{DDQ}=4.5V-5.5V
I_{OL2}		Output Current		8	mA	V_{DDQ}=4.5V-5.5V
V_{OH6}	O6	Output Voltage for DASP# pin	2.4		V	$I_{OH6}=I_{OH6}$ Min
V_{OL6}				0.4		$I_{OL6}=I_{OL6}$ Max
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=3.135V-3.465V
I_{OL6}		Output Current for DASP# pin		8	mA	V_{DDQ}=3.135V-3.465V
I_{OH6}		Output Current for DASP# pin	-3		mA	V_{DDQ}=4.5V-5.5V
I_{OL6}		Output Current for DASP# pin		12	mA	V_{DDQ}=4.5V-5.5V
I_{DD}[1,2]	PWR	Power supply current (T_A = 0°C to +70°C)		50	mA	$V_{DD}=V_{DD}$ Max; $V_{DDQ}=V_{DDQ}$ Max
I_{DD}[1,2]	PWR	Power supply current (T_A = -40°C to +85°C)		100	mA	$V_{DD}=V_{DD}$ Max; $V_{DDQ}=V_{DDQ}$ Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_A = 0°C to +70°C)		100	µA	$V_{DD}=V_{DD}$ Max; $V_{DDQ}=V_{DDQ}$ Max
I_{SP}	PWR	Sleep/Standby/Idle current (T_A = -40°C to +85°C)		200	µA	$V_{DD}=V_{DD}$ Max; $V_{DDQ}=V_{DDQ}$ Max

T10-6.0 1316

1. Sequential data transfer for 1 sector read data from host interface and write data to media.
2. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
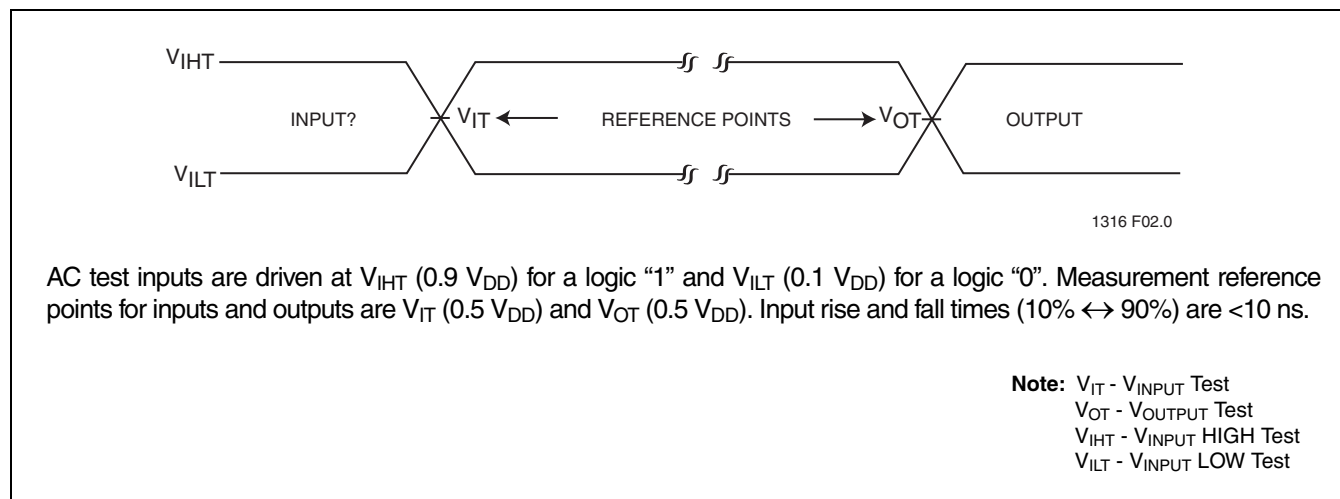
10.2 AC Characteristics

AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <10 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE   10-1: AC Input/Output Reference Waveforms

Advance Information

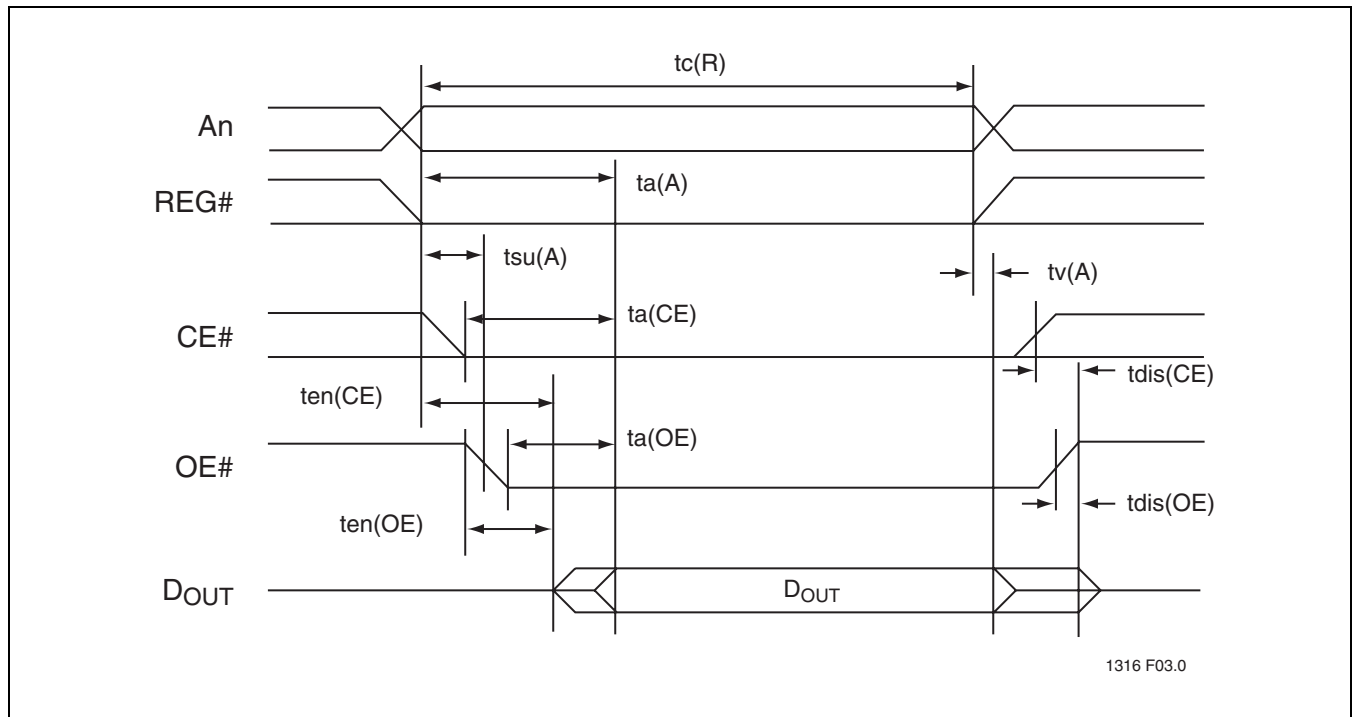## 10.2.1 Attribute Memory Read Timing Specification

The Attribute Memory access time is defined as 100 ns. Detailed timing specifications are shown in Table 10-7.

TABLE 10-7:Attribute Memory Read Timing

Speed Version			100 ns		
Item	Symbol	IEEE Symbol	Min[1]	Max[1]	Units
Read Cycle Time	tc(R)	tAVAV	100		ns
Address Access Time	ta(A)	tAVQV		100	ns
Card Enable Access Time	ta(CE)	tELQV		100	ns
Output Enable Access Time	ta(OE)	tGLQV		50	ns
Output Disable Time from CE#	tdis(CE)	tEHQZ		50	ns
Output Disable Time from OE#	tdis(OE)	tGHQZ		50	ns
Address Setup Time	tsu(A)	tAVGL	10		ns
Output Enable Time from CE#	ten(CE)	tELQNZ	5		ns
Output Enable Time from OE#	ten(OE)	tGLQNZ	5		ns
Data Valid from Address Change	tv(A)	tAXQX	0		ns

T10-7.0 1316

1. D_{OUT} signifies data provided by the CompactFlash card to the system.
   The CE# signal or both the OE# signal and the WE# signal must be de-asserted between consecutive cycle operations.
   All AC specifications are guaranteed by design.

FIGURE 10-2: Attribute Memory Read Timing Diagram

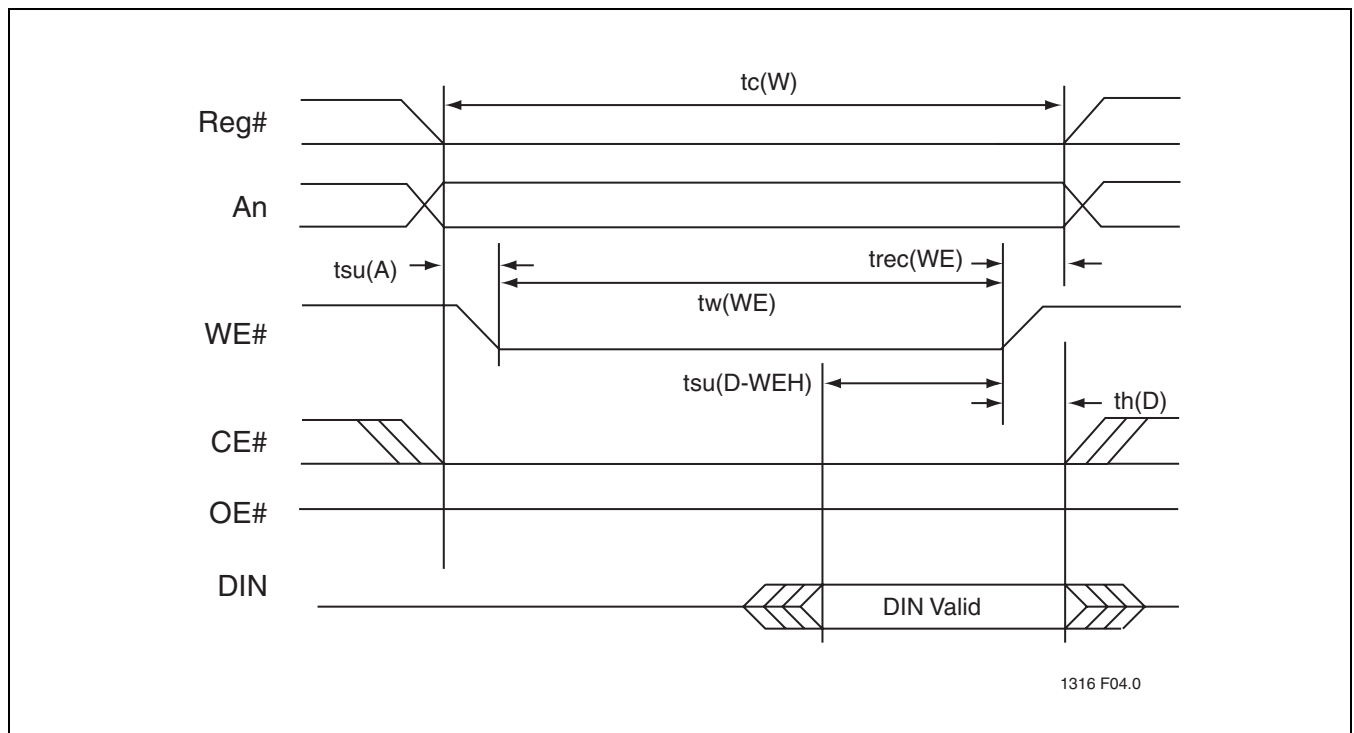### 10.2.2 Configuration Register (Attribute Memory) Write Timing specification

The card configuration write access time is defined as 100 ns. Detailed timing specifications are shown in Table 10-8.

TABLE 10-8:Configuration Register (Attribute Memory) Write Timing

Speed Version			100 ns		
Item	Symbol	IEEE Symbol	Min[1]	Max[1]	Units
Write Cycle Time	tc(W)	tAVAV	100		ns
Write Pulse Width	tw(WE)	tWLWH	60		ns
Address Setup Time	tsu(A)	tAVWL	10		ns
Write Recovery Time	trec(WE)	tWMAX	15		ns
Data Setup Time for WE	tsu(DWE#H)	tDVWH	40		ns
Data Hold Time	th(D)	tWMDX	15		ns

T10-8.0 1316

1. D_{IN} signifies data provided by the system to the CompactFlash card.
   All AC specifications are guaranteed by design.

FIGURE 10-3: Configuration Register (Attribute Memory) Write Timing Diagram

Advance Information

10.2.3 Common Memory Read Timing Specification

TABLE 10-9:Common Memory Read Timing

Item	Symbol	IEEE Symbol	Min[1]	Max[1]	Units
Output Enable Access Time	ta(OE)	tGLQV		50	ns
Output Disable Time from OE	tdis(OE)	tGHQZ		50	ns
Address Setup Time	tsu(A)	tAVGL	10		ns
Address Hold Time	th(A)	tGHAX	15		ns
CE Setup before OE	tsu(CE)	tELGL	0		ns
CE Hold following OE	th(CE)	tGHEH	15		ns

T10-9.0 1316

1. All AC specifications are guaranteed by design.
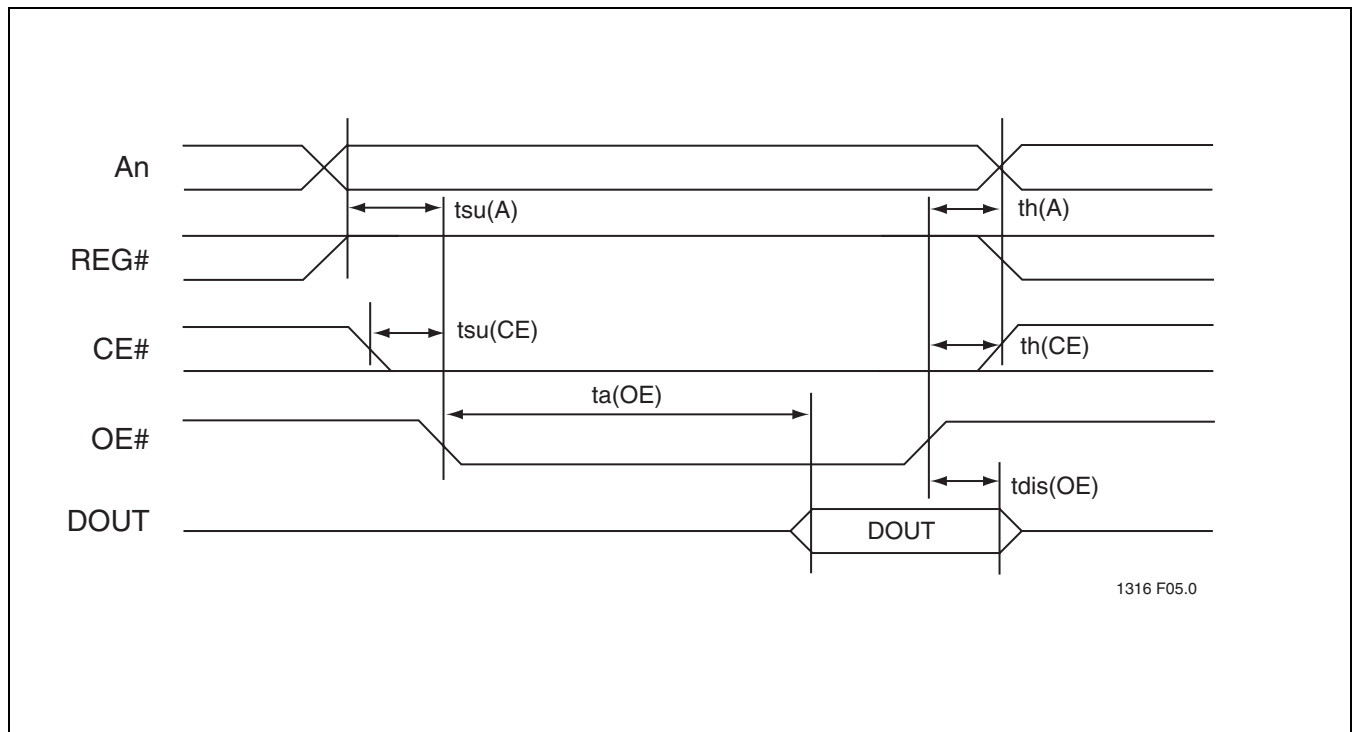
FIGURE 10-4: Common Memory Read Timing Diagram

S71316-00-000   3/06

10.2.4 Common Memory Write Timing Specification

TABLE 10-10:Common Memory Write Timing

Item	Symbol	IEEE Symbol	Min[1]	Max[1]	Units
Data Setup before WE	tsu(DWE#H)	tDVWH	40		ns
Data Hold following WE	th(D)	tWMDX	15		ns
WE Pulse Width	tw(WE)	tWLWH	60		ns
Address Setup Time	tsu(A)	tAVWL	10		ns
CE Setup before WE	tsu(CE)	tELWL	0		ns
Write Recovery Time	trec(WE)	tWMAX	15		ns
Address Hold Time	th(A)	tGHAX	15		ns
CE Hold following WE	th(CE)	tGHEH	15		ns

T10-10.0 1316

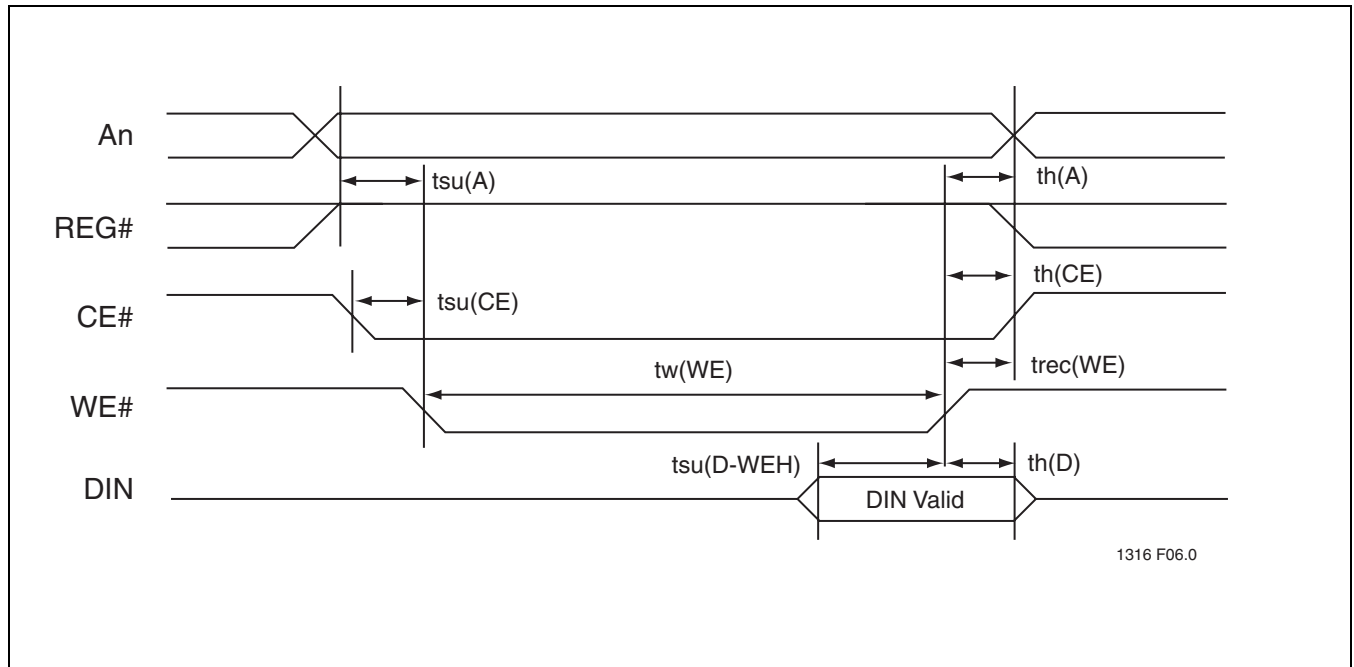1. All AC specifications are guaranteed by design.

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FIGURE 10-5: Common Memory Write Timing Diagram

Advance Information

10.2.5 I/O Input (Read) Timing Specification

TABLE 10-11:I/O Read Timing

Item	Symbol	IEEE Symbol	Min[1]	Max[1]	Units
Data Delay after IORD	td(IORD)	tIGLQV		100	ns
Data Hold following IORD	th(IORD)	tIGHQX	0		ns
IORD Width Time	tw(IORD)	tIGLIGH	165		ns
Address Setup before IORD	tsuA(IORD)	tAVIGL	70		ns
Address Hold following IORD	thA(IORD)	tIGHAX	20		ns
CE Setup before IORD	tsuCE(IORD)	tELIGL	5		ns
CE Hold following IORD	thCE(IORD)	tIGHEH	20		ns
REG Setup before IORD	tsuREG(IORD)	tRGLIGL	5		ns
REG Hold following IORD	thREG(IORD)	tIGHRGH	0		ns
INPACK Delay Falling from IORD	tdfINPACK(IORD)	tIGLIAL	0	45	ns
INPACK Delay Rising from IORD	tdrINPACK(IORD)	tIGHIAH		45	ns
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35	ns
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35	ns

T10-11.0 1316

1. All AC specifications are guaranteed by design.
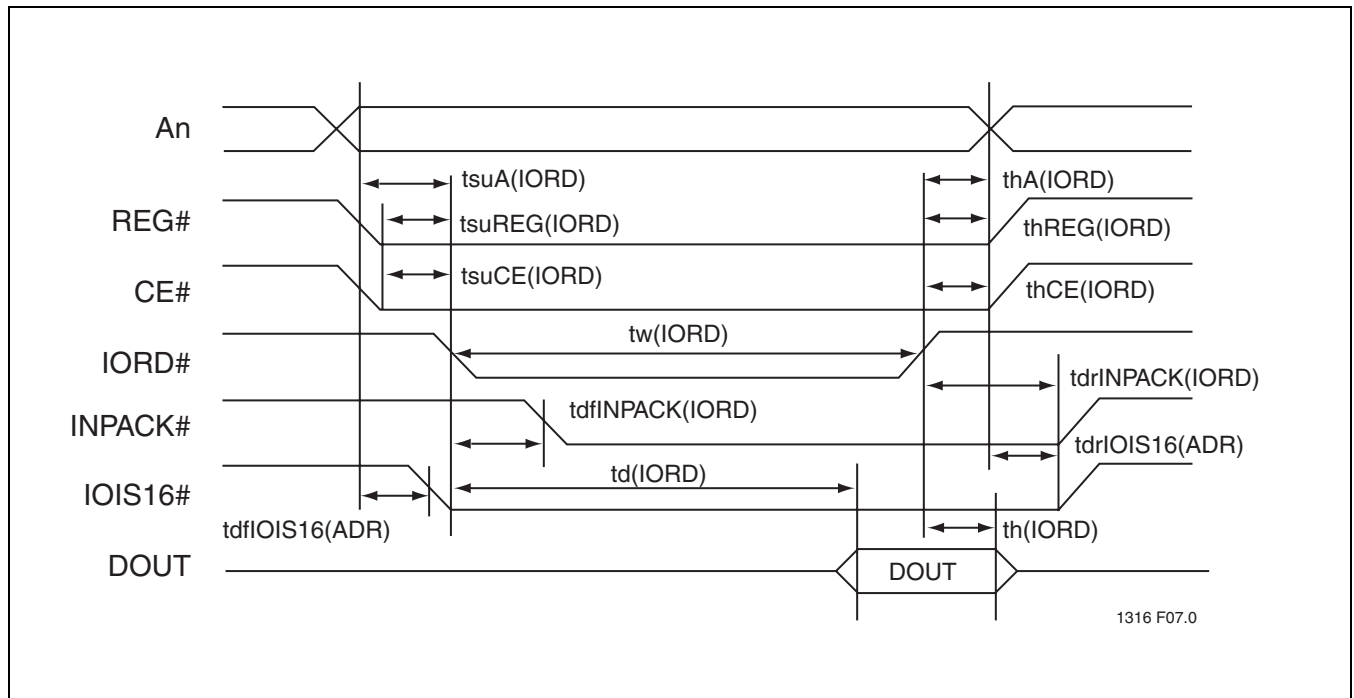**Note:** The maximum load on -INPACK and IOIS16# is 1 LSTTL with 50pF total load.

FIGURE 10-6: I/O Read Timing Diagram

10.2.6 I/O Output (Write) Timing Specification

TABLE 10-12:I/O Write Timing

Item	Symbol	IEEE Symbol	Min[1]	Max[1]	Units
Data Setup before IOWR	tsu(IOWR)	tDVIWH	60		ns
Data Hold following IOWR	th(IOWR)	tIWHDX	30		ns
IOWR Width Time	tw(IOWR)	tIWLIWH	165		ns
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	70		ns
Address Hold following IOWR	thA(IOWR)	tIWHAX	20		ns
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	5		ns
CE Hold following IOWR	thCE(IOWR)	tIWHEH	20		ns
REG Setup before IOWR	tsuREG(IOWR)	tRGLIWL	5		ns
REG Hold following IOWR	thREG(IOWR)	tIWHRGH	0		ns
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		35	ns
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		35	ns

T10-12.0 1316

1. All AC specifications are guaranteed by design.
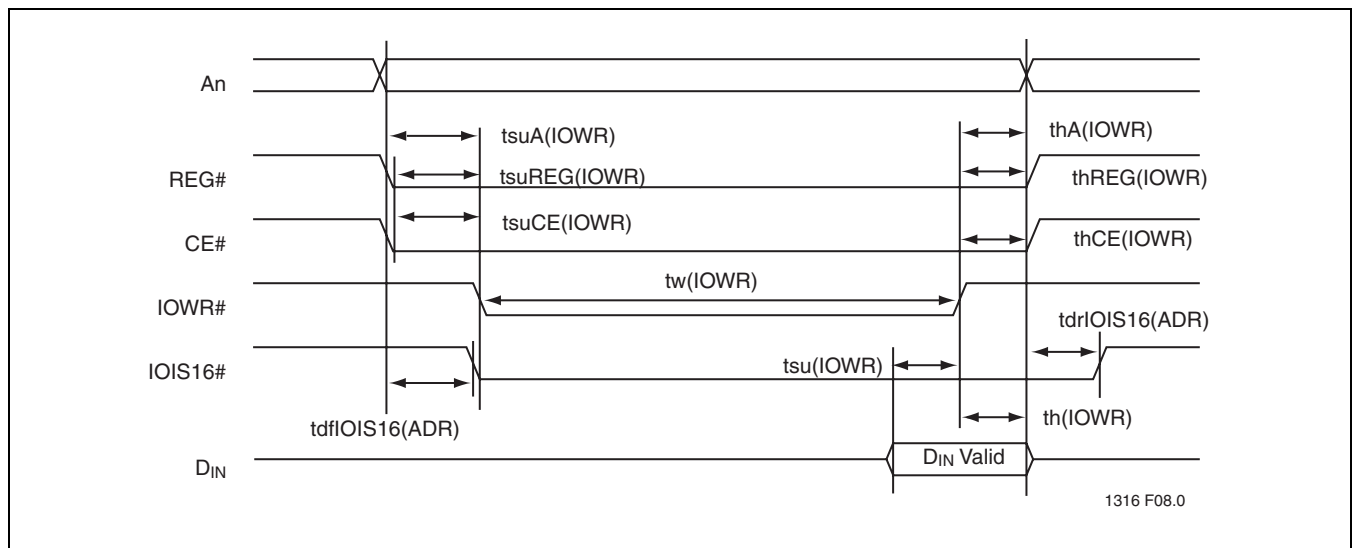**Note:** The maximum load on -INPACK, and IOIS16# is 1 LSTTL with 50pF total load.

FIGURE   10-7: I/O Write Timing Diagram

S71316-00-000   3/06

Advance Information

10.2.7 True IDE Mode I/O Input (Read) Timing Specification

TABLE 10-13:True IDE Mode I/O Read Timing Diagram

Item	Symbol	IEEE Symbol	Min	Max	Units
Data Delay after IORD	td(IORD)	tIGLQV		50	ns
Data Hold following IORD	th(IORD)	tIGHQX	5		ns
IORD Width Time	tw(IORD)	tIGLIGH	70		ns
Address Setup before IORD	tsuA(IORD)	tAVIGL	25		ns
Address Hold following IORD	thA(IORD)	tIGHAX	10		ns
CE Setup before IORD	tsuCE(IORD)	tELIGL	10		ns
CE Hold following IORD	thCE(IORD)	tIGHEH	5		ns
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		20	ns
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		20	ns

T10-13.0 1316

Note: The maximum load on IOIS16# is 1 LSTTL with 50pF total load.
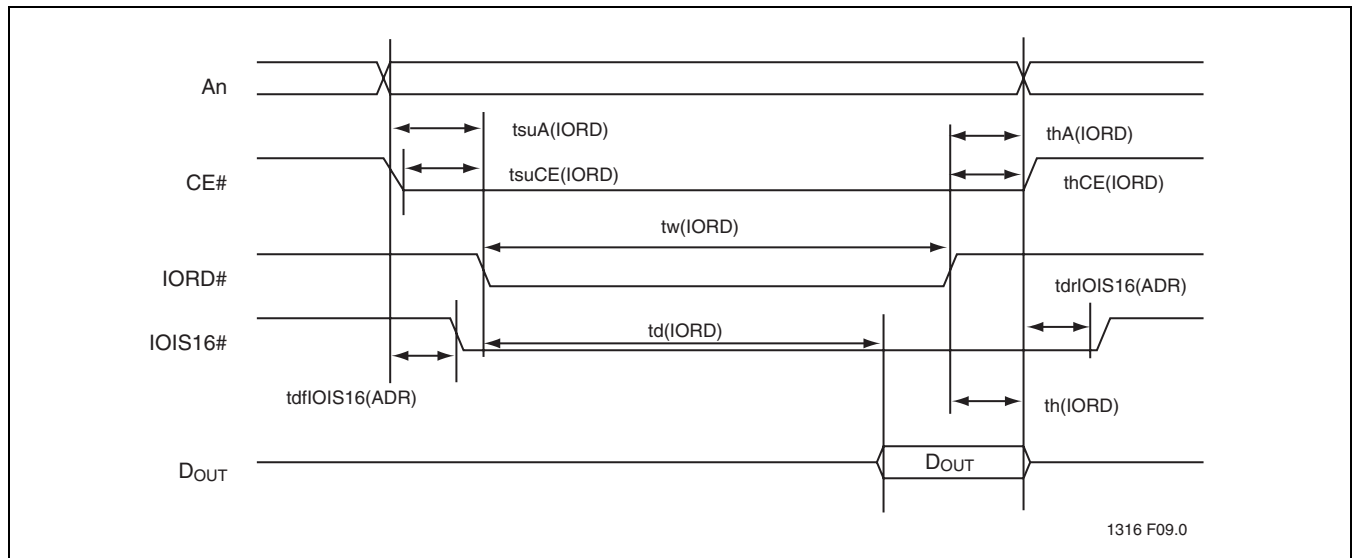All AC specifications are guaranteed by design.

FIGURE   10-8: True IDE Mode I/O Read Timing Diagram

10.2.8 True IDE Mode I/O Output (Write) Timing Specification

TABLE 10-14:True IDE Mode I/O Write Timing

Item	Symbol	IEEE Symbol	Min[1]	Max[1]
Data Setup before IOWR	tsu(IOWR)	tDVIWH	20	
Data Hold following IOWR	th(IOWR)	tIWHDX	10	
IOWR Width Time	tw(IOWR)	tIWLIWH	70	
Address Setup before IOWR	tsuA(IOWR)	tAVIWL	25	
Address Hold following IOWR	thA(IOWR)	tIWHAX	10	
CE Setup before IOWR	tsuCE(IOWR)	tELIWL	10	
CE Hold following IOWR	thCE(IOWR)	tIWHEH	5	
IOIS16 Delay Falling from Address	tdfIOIS16(ADR)	tAVISL		20
IOIS16 Delay Rising from Address	tdrIOIS16(ADR)	tAVISH		20

T10-14.0 1316

1. All times are in nanoseconds.
Note: The maximum load on IOIS16# is 1 LSTTL with 50pF total load.
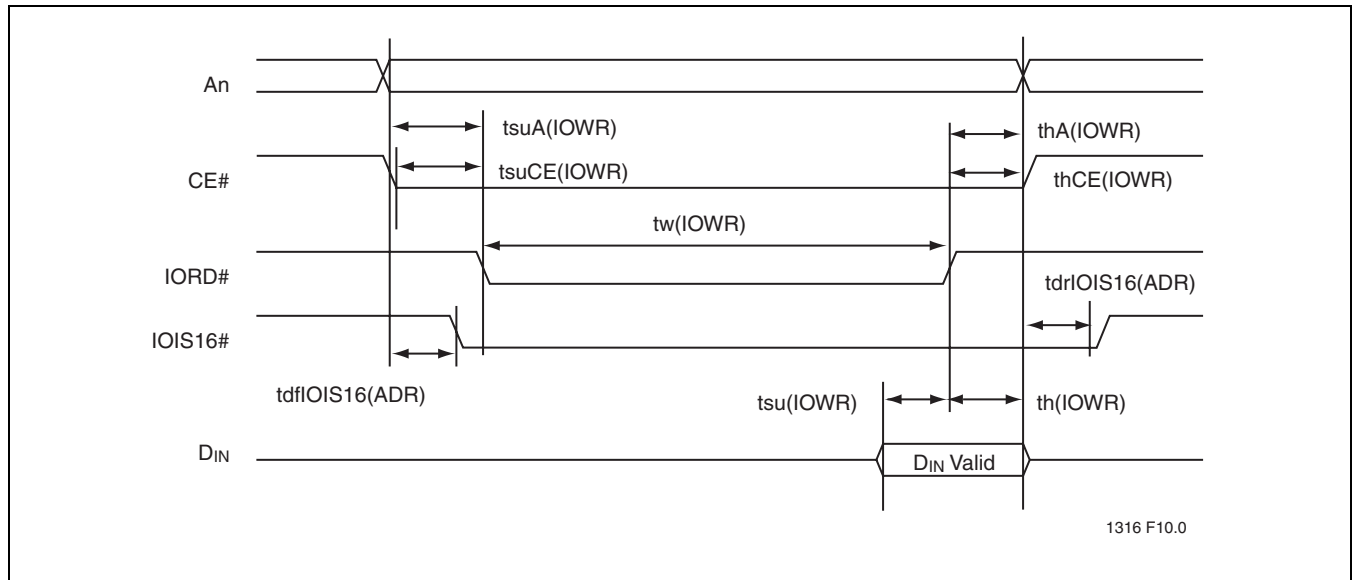All AC specifications are guaranteed by design.

FIGURE   10-9: True IDE Mode I/O Write Timing Diagram

Advance Information

10.2.9 Media Side Interface I/O Timing Specifications

TABLE 10-15: Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{CLS}	FCLE Setup Time	20	-	ns
T_{CLH}	FCLE Hold Time	40	-	ns
T_{CS}	FCE# Setup Time	40	-	ns
T_{CH}	FCE# Hold Time for Command/Data Write Cycle	40	-	ns
T_{CHR}	FCE# Hold Time for Sequential Read Last Cycle	-	40	ns
T_{WP}	FWE# Pulse Width	20	-	ns
T_{WH}	FWE# High Hold Time	20	-	ns
T_{WC}	Write Cycle Time	40	-	ns
T_{ALS}	FALE Setup Time	20	-	ns
T_{ALH}	FALE Hold Time	40	-	ns
T_{DS}	FAD[15:0] Setup Time	20	-	ns
T_{DH}	FAD[15:0] Hold Time	20	-	ns
T_{RP}	FRE# Pulse Width	20	-	ns
T_{RR}	Ready to FRE# Low	40	-	ns
T_{RES}	FRE# Data Setup Access Time	20	-	ns
T_{RC}	Read Cycle Time	40	-	ns
T_{REH}	FRE# High Hold Time	20	-	ns
T_{RHZ}	FRE# High to Data Hi-Z	5	-	ns

T10-15.0 1316
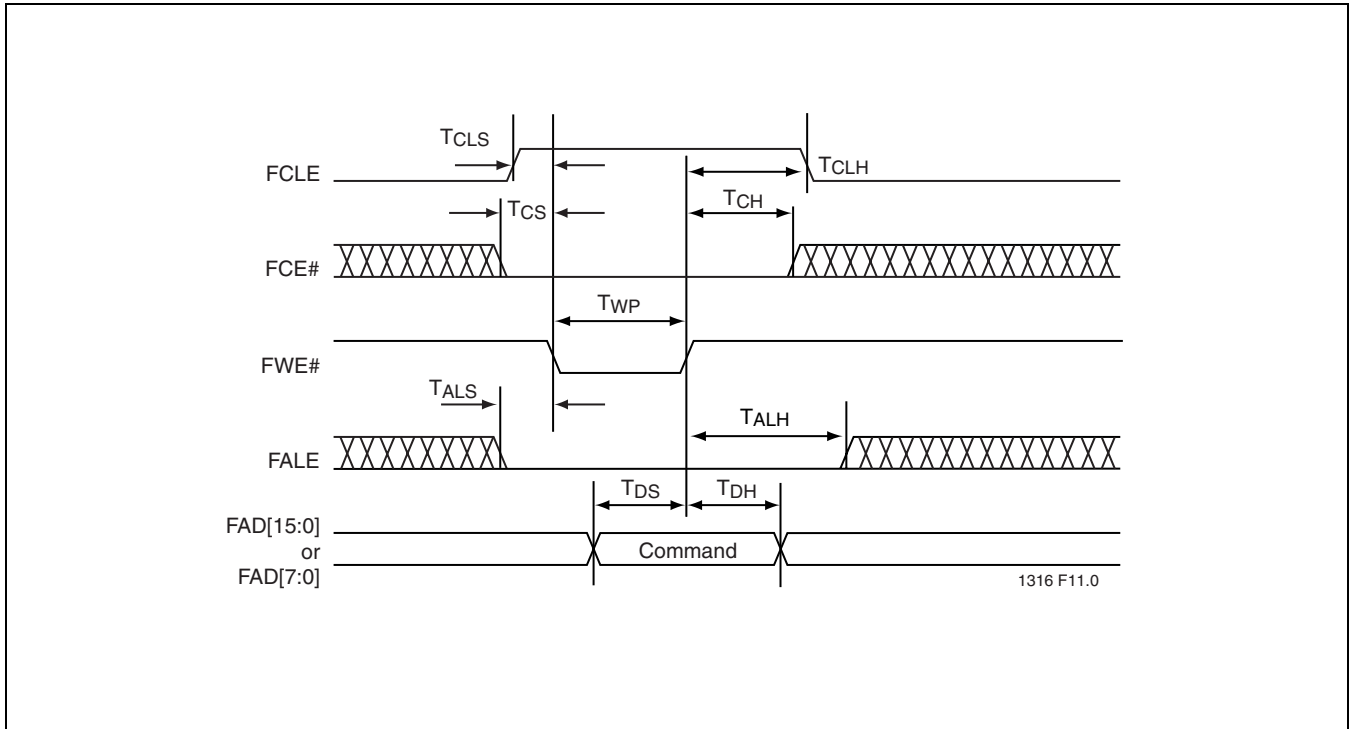
Note: All AC specifications are guaranteed by design.
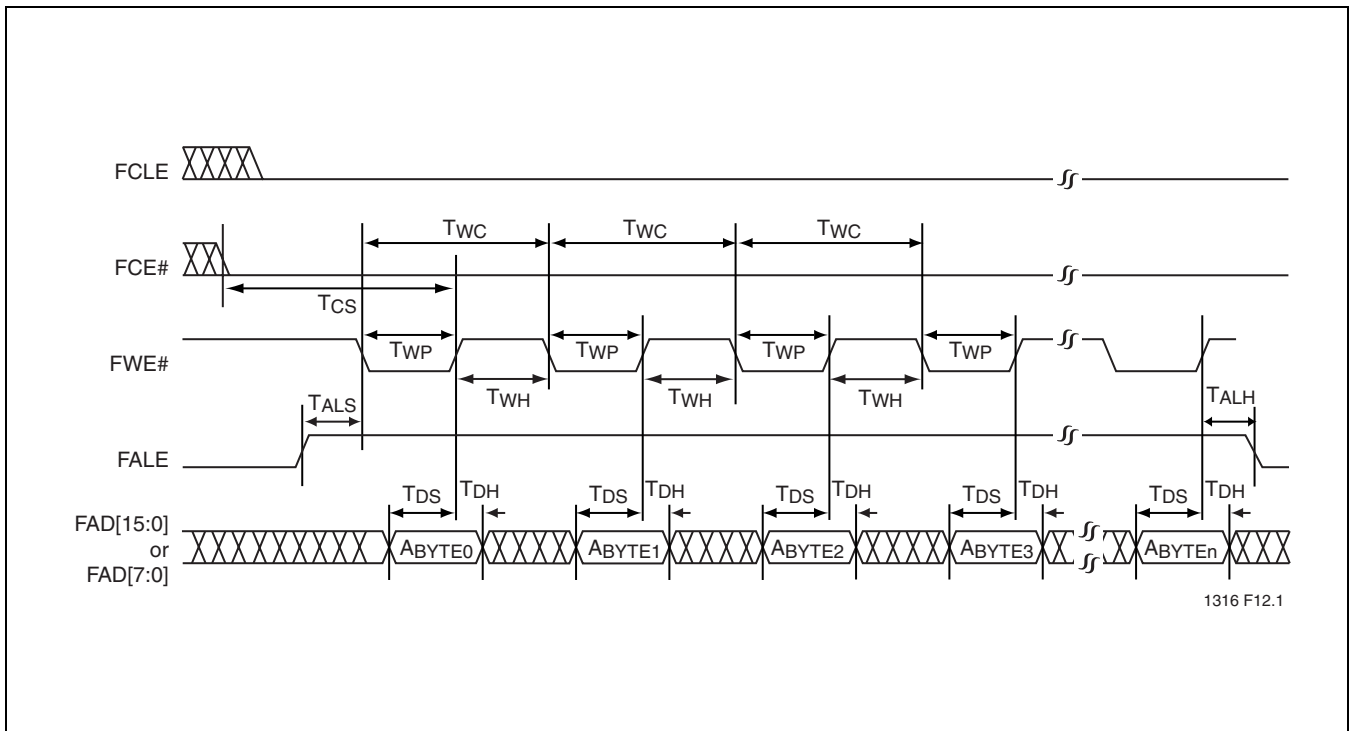
FIGURE 10-10: Media Command Latch Cycle

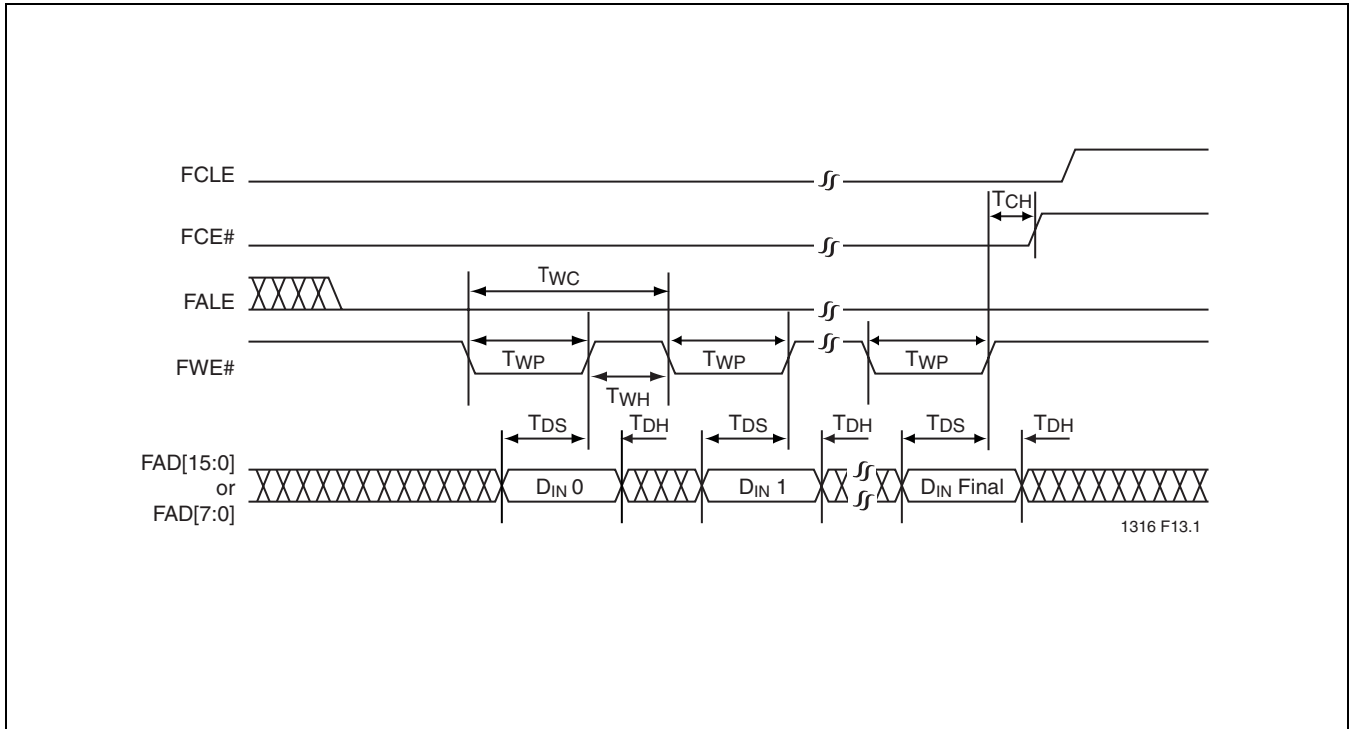**FIGURE 10-11: Media Address Latch Cycle**

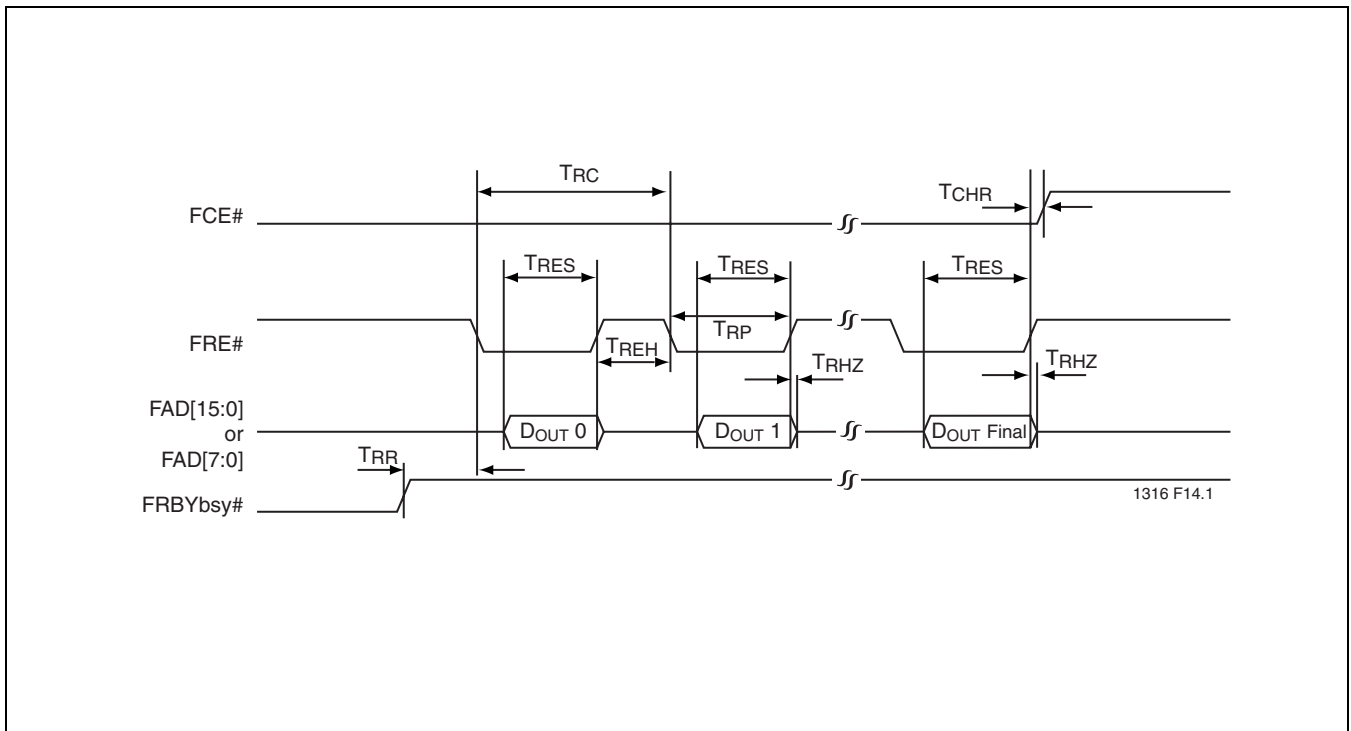**FIGURE 10-12: Media Data Loading Latch Cycle**

FIGURE 10-13: Media Data Read Cycle

11.0 APPENDIX

11.1 Differences between CF-ATA and PC Card-ATA/True IDE

This section details differences between CF-ATA vs. PC Card ATA and the differences between CF-ATA vs. True IDE.

11.1.1 Electrical Differences

11.1.1.1 TTL Compatibility
CF is not TTL compatible, it is a purely CMOS interface. Refer to Section 2.3.2 of this specification.

11.1.1.2 Pull Up Resistor Input Leakage Current
The minimum pull up resistor input leakage current is 50K ohms rather than the 10K ohms stated in the PCMCIA specification.

11.1.2 Functional Differences

11.1.2.1 Additional Set Features Codes in CF-ATA
The following Set Features codes are not PC Card ATA or True IDE, but provide additional functionality in CF-ATA.

- 69H, Accepted for backward compatibility
- 96H, Accepted for backward compatibility
- 97H, Accepted for backward compatibility
- 9AH, Set the host current source capability

11.1.2.2 Additional Commands in CF-ATA
The following commands are not standard PC Card ATA commands, but provide additional functionality in CF-ATA.

The command codes for the commands below are defined as vendor unique in PC Card ATA/True IDE.

- C0H, Erase-Sectors
- 87H, Translate-Sector
- F5H, Wear-Level

The command codes for the commands below are defined as reserved in PC Card ATA/True IDE:

- 03H, Request-Sense
- 38H, Write-Without-Erase
- CDH, Write-Multiple-Without-Erase
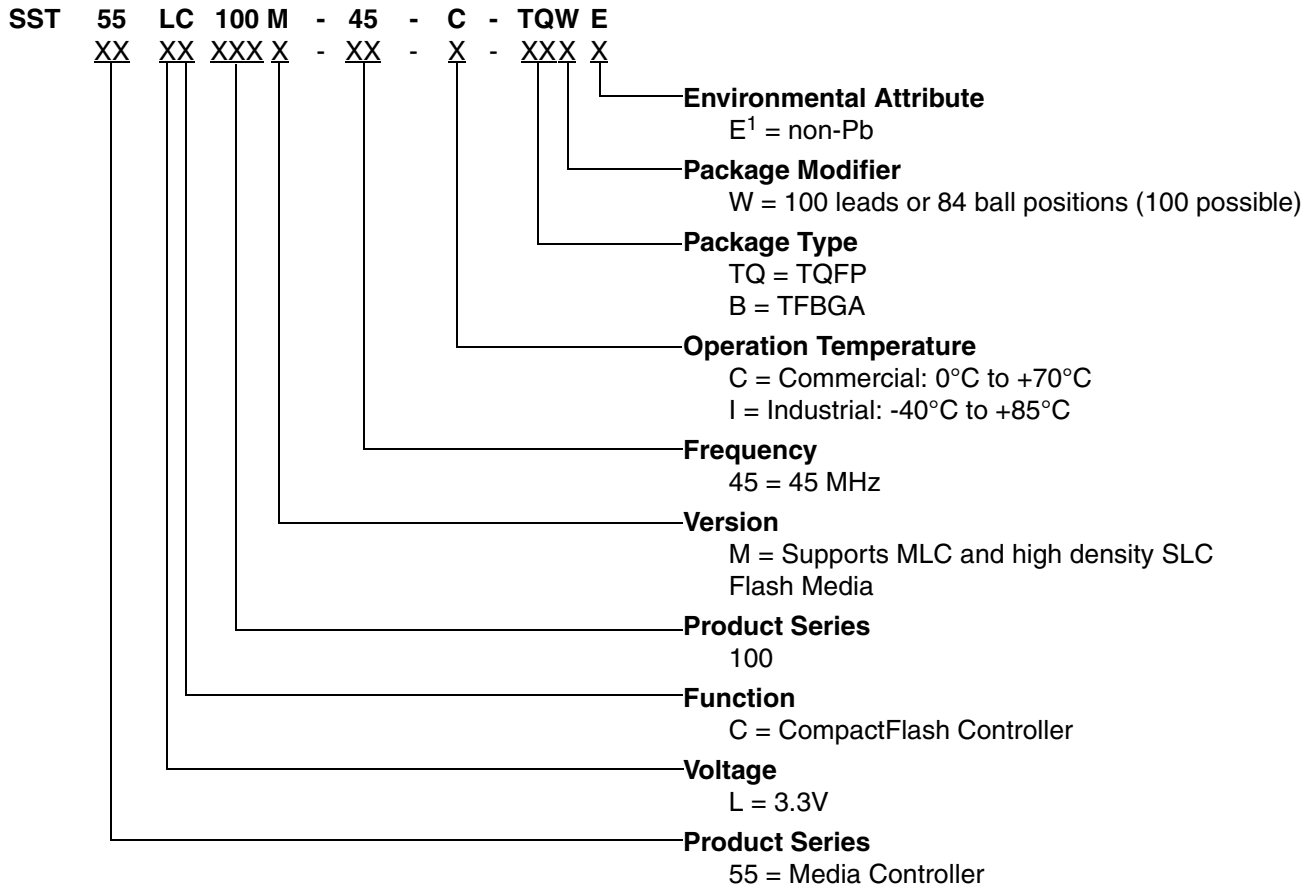
11.1.2.3 Idle Timer
The Idle timer uses an incremental value of 5 ms, rather than the 5 sec minimum increment value specified in PC Card ATA/True IDE.

11.1.2.4 Recovery from Sleep Mode
For CF devices, recovery from sleep mode is accomplished by simply issuing another command to the device. A hardware or software reset is not required.

Advance Information

12.0 PRODUCT ORDERING INFORMATION

```
SST   55   LC  100 M  -  45  -  C  -  TQW E
      XX   XX  XXX X  -  XX  -  X  -  XXX X
```

Environmental Attribute
   E[1] = non-Pb

Package Modifier
   W = 100 leads or 84 ball positions (100 possible)

Package Type
   TQ = TQFP
   B = TFBGA

Operation Temperature
   C = Commercial: 0°C to +70°C
   I = Industrial: -40°C to +85°C

Frequency
   45 = 45 MHz

Version
   M = Supports MLC and high density SLC
   Flash Media

Product Series
   100

Function
   C = CompactFlash Controller

Voltage
   L = 3.3V

Product Series
   55 = Media Controller

1. Environmental suffix "E" denotes non-Pb solder.
   SST non-Pb solder devices are "RoHS Compliant".

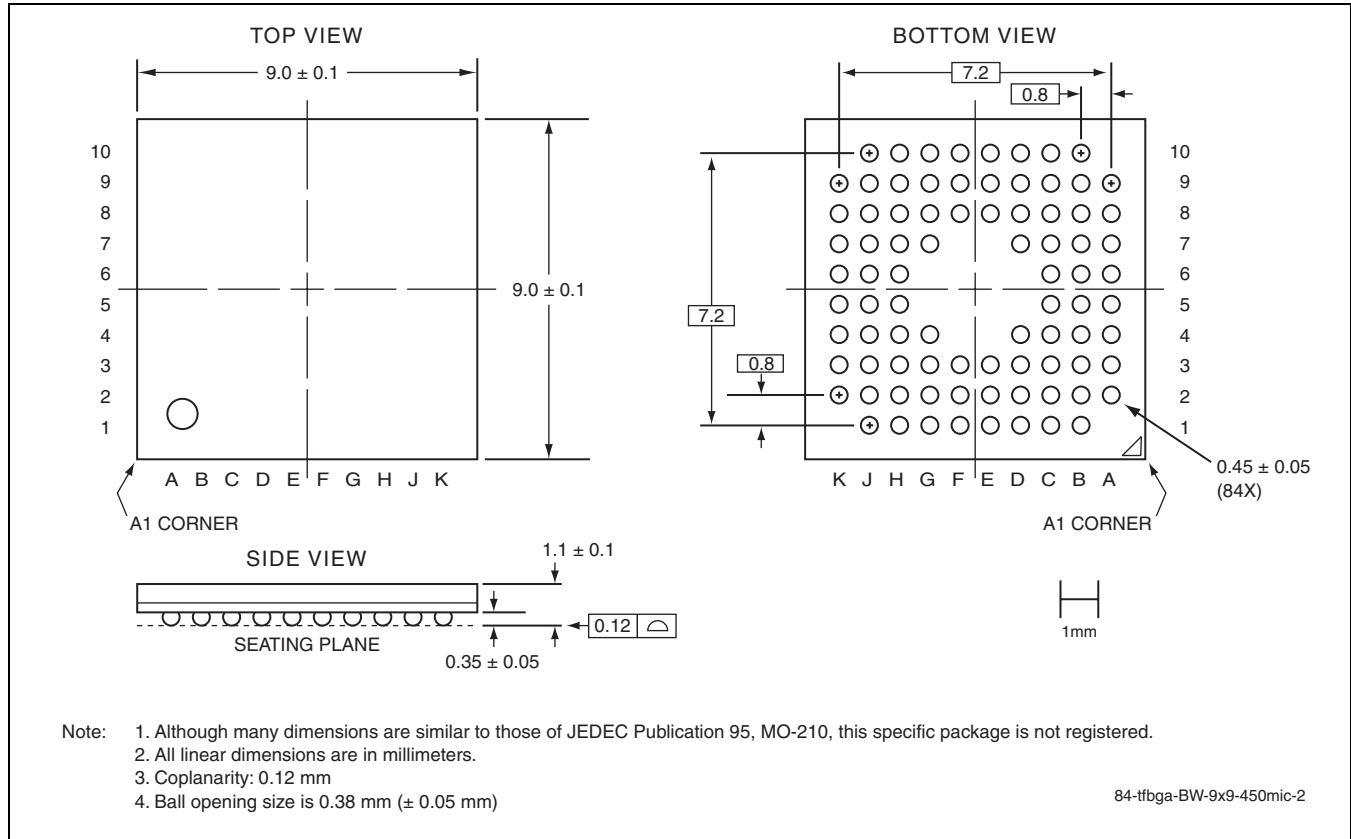## 12.1 Valid Combinations

Valid combinations for SST55LC100M

SST55LC100M-45-C-TQWE   SST55LC100M-45-C-BWE
SST55LC100M-45-I-TQWE   SST55LC100M-45-I-BWE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales
representative to confirm availability of valid combinations and to determine availability of new combinations.

13.0 PACKAGING DIAGRAM

TOP VIEW

9.0 ± 0.1

9.0 ± 0.1

10
9
8
7
6
5
4
3
2
1

A B C D E F G H J K

A1 CORNER

BOTTOM VIEW

7.2

0.8

7.2

0.8

10
9
8
7
6
5
4
3
2
1

K J H G F E D C B A

A1 CORNER

0.45 ± 0.05
(84X)

SIDE VIEW

1.1 ± 0.1

SEATING PLANE

0.35 ± 0.05

0.12

1mm

Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
              2. All linear dimensions are in millimeters.
              3. Coplanarity: 0.12 mm
              4. Ball opening size is 0.38 mm (± 0.05 mm)

84-tfbga-BW-9x9-450mic-2

FIGURE   13-1: 84-ball Thin, Fine-pitch, Ball Grid Array (TFBGA)
SST Package Code: BW

Advance Information
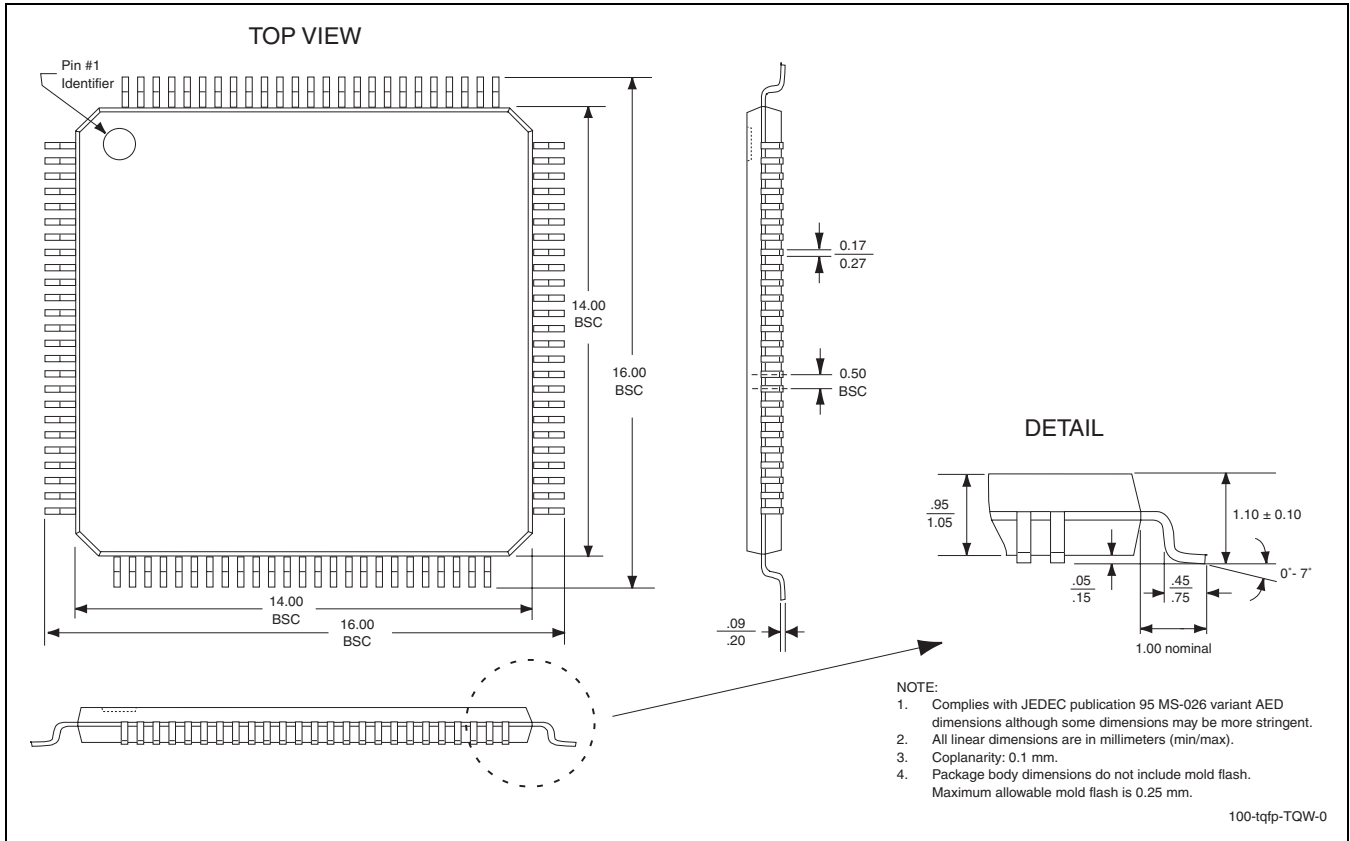
FIGURE 13-2: 100-lead Thin Quad Flat Pack (TQFP)
SST Package Code: TQW

NOTE:
1. Complies with JEDEC publication 95 MS-026 variant AED dimensions although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (min/max).
3. Coplanarity: 0.1 mm.
4. Package body dimensions do not include mold flash. Maximum allowable mold flash is 0.25 mm.

100-tqfp-TQW-0

TABLE 13-1: Revision History

Number	Description	Date
00	• Initial release of the data sheet (Advance Information)	Mar 2006

14.0 PCMCIA STANDARD

CompactFlash memory cards are fully electrically compatible with the PCMCIA specifications listed below. These specifications may be obtained from:

PCMCIA
2635 North First St. Ste. 209
San Jose, CA 95131 USA

Phone: 408-433-2273
Fax: 408-433-9558

15.0 COMPACTFLASH SPECIFICATION

CompactFlash memory cards are fully compatible with the CompactFlash Specification published by the Compact-Flash Association. Contact the CompactFlash Association for more information.

CompactFlash Association
P.O. Box 51537
Palo Alto, CA 94303 USA

Silicon Storage Technology, Inc. • 1171 Sonora Court • Sunnyvale, CA 94086 • Telephone 408-735-9110 • Fax 408-735-9036
www.SuperFlash.com or www.sst.com

S71316-00-000   3/06