

32 Mbit Dual-Bank Flash + 4 Mbit SRAM ComboMemory

SST34HF324G



Data Sheet

FEATURES:

- **Flash Organization: 2M x16**
 - 32 Mbit: 24Mbit + 8Mbit
- **Concurrent Operation**
 - Read from or Write to SRAM while Erase/Program Flash
- **SRAM Organization:**
 - 4 Mbit: 256K x16
- **Single 2.7-3.3V Read and Write Operations**
- **Superior Reliability**
 - Endurance: 100,000 Cycles (typical)
 - Greater than 100 years Data Retention
- **Low Power Consumption: (typical values @ 5 MHz)**
 - Active Current: Flash 10 mA (typical)
SRAM 6 mA (typical)
 - Standby Current: 10 μ A (typical)
- **Hardware Sector Protection (WP#)**
 - Protects 4 outer most sectors (8 KWord) in the smaller bank by holding WP# low and unprotects by holding WP# high
- **Hardware Reset Pin (RST#)**
 - Resets the internal state machine to reading data array
- **Sector-Erase Capability**
 - Uniform 2 KWord sectors
- **Block-Erase Capability**
 - Uniform 32 KWord blocks
- **Read Access Time**
 - Flash: 70 ns
 - SRAM: 70 ns
- **Erase-Suspend / Erase-Resume Capabilities**
- **Latched Address and Data**
- **Fast Erase and Word-Program (typical):**
 - Sector-Erase Time: 18 ms
 - Block-Erase Time: 18 ms
 - Chip-Erase Time: 35 ms
 - Program Time: 7 μ s
- **Automatic Write Timing**
 - Internal V_{PP} Generation
- **End-of-Write Detection**
 - Toggle Bit
 - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Packages Available**
 - 48-ball LFBGA (6mm x 8mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST34HF324G ComboMemory devices integrate a 2M x16 CMOS flash memory bank with 256K x16 CMOS SRAM memory bank in a multi-chip package (MCP). These devices are fabricated using SST's proprietary, high-performance CMOS SuperFlash technology incorporating the split-gate cell design and thick-oxide tunneling injector to attain better reliability and manufacturability compared with alternate approaches. The SST34HF324G devices are ideal for applications such as cellular phones, GPS devices, PDAs, and other portable electronic devices in a low power and small form factor system.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles. The SST34HF324G devices offer a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years. With high-performance Program operations, the flash memory banks provide a typical Pro-

gram time of 7 μ sec. The entire flash memory bank can be erased and programmed word-by-word in 4 seconds (typically) for the SST34HF324G, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST34HF324G devices contain on-chip hardware and software data protection schemes.

The flash and SRAM operate as two independent memory banks with respective bank enable signals. The memory bank selection is done by two bank enable signals. The SRAM bank enable signal, BES#, selects the SRAM bank. The flash memory bank enable signal, BEF#, has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The memory banks are superimposed in the same memory address space where they share common address lines, data lines, WE# and OE# which minimize power consumption and area. See Table 3 for memory organization.



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Designed, manufactured, and tested for applications requiring low power and small form factor, the SST34HF324G are offered in both commercial and extended temperatures and a small footprint package to meet board space constraint requirements. See Figure 2 for pin assignments.

Device Operation

The SST34HF324G use BES# and BEF# to control operation of either the flash or the SRAM memory bank. When BEF# is low, the flash bank is activated for Read, Program or Erase operation. When BES# is low the SRAM is activated for Read and Write operation. BEF# and BES# cannot be at low level at the same time. **If all bank enable signals are asserted, bus contention will result and the device may suffer permanent damage.** All address, data, and control lines are shared by flash and SRAM memory banks which minimizes power consumption and loading. The device goes into standby when BEF# and BES# bank enables are raised to V_{IHc} (Logic High) or when BEF# is high.

Concurrent Read/Write Operation

The SST34HF324G provide the unique benefit of being able to read from or write to SRAM, while simultaneously erasing or programming the flash. This allows data alteration code to be executed from SRAM, while altering the data in flash. The following table lists all valid states.

Concurrent Read/Write State Table

Flash	SRAM
Program/Erase	Read
Program/Erase	Write

The device will ignore all SDP commands when an Erase or Program operation is in progress. Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

Flash Read Operation

The Read operation of the SST34HF324G is controlled by BEF# and OE#, both have to be low for the system to obtain data from the outputs. BEF# is used for device selection. When BEF# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either BEF# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 6).

Flash Program Operation

These devices are programmed on a word-by-word basis. Before programming, one must ensure that the sector which is being programmed is fully erased.

The Program operation is accomplished in three steps:

1. Software Data Protection is initiated using the three-byte load sequence.
2. Address and data are loaded.

During the Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first.

3. The internal Program operation is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed typically within 7 μ s.

See Figures 7 and 8 for WE# and BEF# controlled Program operation timing diagrams and Figure 20 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during an internal Program operation are ignored.

Flash Sector- /Block-Erase Operation

These devices offer both Sector-Erase and Block-Erase operations. These operations allow the system to erase the devices on a sector-by-sector (or block-by-block) basis. The sector architecture is based on a uniform sector size of 2 KWord. The Block-Erase mode is based on a uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with a Sector-Erase command (50H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (30H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. Any commands issued during the Block- or Sector-Erase operation are ignored except Erase-Suspend and Erase-Resume. See Figures 12 and 13 for timing waveforms.



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Flash Chip-Erase Operation

The SST34HF324G provide a Chip-Erase operation, which allows the user to erase all sectors/blocks to the “1” state. This is useful when the device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or BEF#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bits or Data# Polling. See Table 6 for the command sequence, Figure 11 for timing diagram, and Figure 23 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Flash Erase-Suspend/-Resume Operations

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location, or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing a one-byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode within 20 μ s after the Erase-Suspend command had been issued. Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ₂ toggling and DQ₆ at “1”. While in Erase-Suspend mode, a Program operation is allowed except for the sector or block selected for Erase-Suspend. To resume Sector-Erase or Block-Erase operation which has been suspended, the system must issue an Erase-Resume command. The operation is executed by issuing a one-byte command sequence with Erase Resume command (30H) at any address in the one-byte sequence.

Flash Write Operation Status Detection

The SST34HF324G provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ₇) and Toggle Bit (DQ₆). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling (DQ₇) or Toggle Bit (DQ₆) read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ₇ or DQ₆. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Flash Data# Polling (DQ₇)

When the device is in an internal Program operation, any attempt to read DQ₇ will produce the complement of the true data. Once the Program operation is completed, DQ₇ will produce true data. During internal Erase operation, any attempt to read DQ₇ will produce a ‘0’. Once the internal Erase operation is completed, DQ₇ will produce a ‘1’. The Data# Polling is valid after the rising edge of fourth WE# (or BEF#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or BEF#) pulse. See Figure 9 for Data# Polling (DQ₇) timing diagram and Figure 21 for a flowchart.

Toggle Bits (DQ₆ and DQ₂)

During the internal Program or Erase operation, any consecutive attempts to read DQ₆ will produce alternating “1”s and “0”s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ₆ bit will stop toggling. The device is then ready for the next operation. The toggle bit is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operations. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ₆) is valid after the rising edge of sixth WE# (or BEF#) pulse. DQ₆ will be set to “1” if a Read operation is attempted on an Erase-suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ₆ will toggle.

An additional Toggle Bit is available on DQ₂, which can be used in conjunction with DQ₆ to check whether a particular sector is being actively erased or erase-suspended. Table 1 shows detailed status bit information. The Toggle Bit (DQ₂) is valid after the rising edge of the last WE# (or BEF#) pulse of a Write operation. See Figure 10 for Toggle Bit timing diagram and Figure 21 for a flowchart.



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TABLE 1: Write Operation Status

Status		DQ ₇	DQ ₆	DQ ₂
Normal Operation	Standard Program	DQ7#	Toggle	No Toggle
	Standard Erase	0	Toggle	Toggle
Erase-Suspend Mode	Read From Erase Suspended Sector/Block	1	1	Toggle
	Read From Non-Erase Suspended Sector/Block	Data	Data	Data
	Program	DQ7#	Toggle	No Toggle

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Note: DQ₇, DQ₆, and DQ₂ require a valid address when reading status information.

Data Protection

The SST34HF324G provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST34HF324G provide a hardware block protection which protects the outermost 8 KWord in Bank 1. The block is protected when WP# is held low. See Figure 3 for Block-Protection location.

A user can disable block protection by driving WP# high thus allowing erase or program of data into the protected sectors. WP# must be held high prior to issuing the write command and remain stable until after the entire Write operation has completed.

Hardware Reset (RST#)

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see Figure 17). When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 16).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity. See Figures 16 and 17 for timing diagrams.

Software Data Protection (SDP)

The SST34HF324G provide the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST34HF324G are shipped with the Software Data Protection permanently enabled. See Table 6 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ₁₅-DQ₈ are “Don’t Care” during any SDP command sequence.



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Product Identification

The Product Identification mode identifies the device as SST34HF324G and the manufacturer as SST. This mode may be accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers cannot be used on this device because of the shared lines between flash and SRAM in the multi-chip package. Therefore, application of high voltage to pin A₉ may damage this device. Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Tables 5 and 6 for software operation, Figure 14 for the Software ID Entry and Read timing diagram and Figure 22 for the ID Entry command sequence flowchart.

TABLE 2: Product Identification

	ADDRESS	DATA
Manufacturer's ID	BK0000H	00BFH
Device ID SST34HF324G	BK0001H	7353H

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Note: BK = Bank Address (A₂₀-A₁₈)

Product Identification Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 6 for software command codes, Figure 15 for timing waveform and Figure 22 for a flowchart.

SRAM Operation

With BES# low and BEF# high, the SST34HF324G operates as either 256K x16 CMOS SRAM, with fully static operation requiring no external clocks or timing strobes. When BES# and BEF# are high, all memory banks are deselected and the device enters standby. Read and Write cycle times are equal. The control signals UBS# and LBS# provide access to the upper data byte and lower data byte. See Table 5 for SRAM Read and Write data byte control modes of operation.

SRAM Read

The SRAM Read operation of the SST34HF324G is controlled by OE# and BES#, both have to be low with WE# high for the system to obtain data from the outputs. BES# is used for SRAM bank selection. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 3, for further details.

SRAM Write

The SRAM Write operation of the SST34HF324G is controlled by WE# and BES#, both have to be low for the system to write to the SRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of either BES# or WE# whichever occurs first. The write time is measured from the last falling edge of BES# or WE# to the first rising edge of BES# or WE#. Refer to the Write cycle timing diagrams, Figures 4 and 5, for further details.



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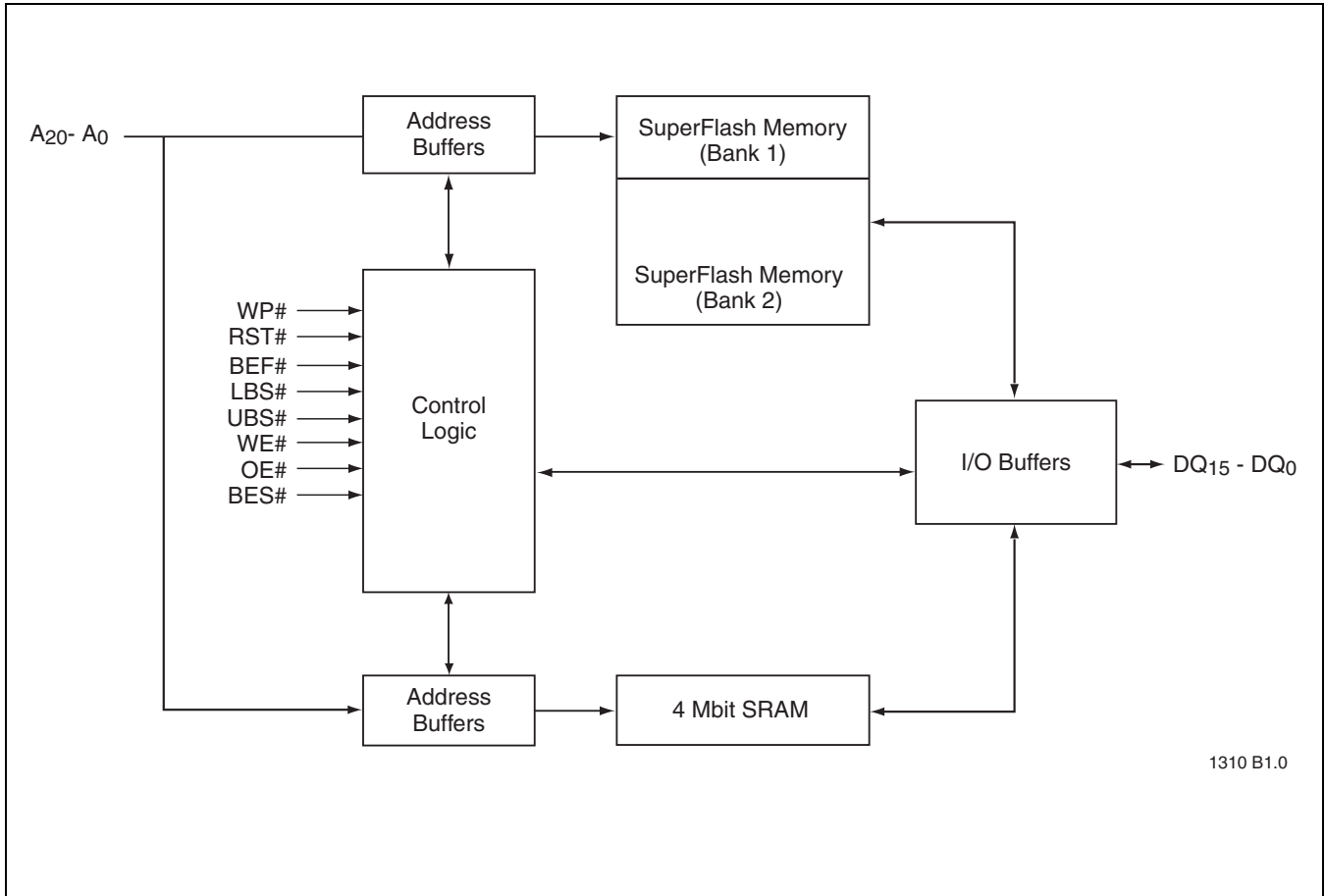


FIGURE 1: Functional Block Diagram

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TABLE 3: Dual-Bank Memory Organization (1 of 2)

SST34HF324G	Block	Block Size	Address Range x8	Address Range x16
Bank 1	BA63	8 KW / 16 KB	3FC000H–3FFFFFFH	1FE000H–1FFFFFFH
		24 KW / 48 KB	3F0000H–3FBFFFFH	1F8000H–1FDFFFFH
	BA62	32 KW / 64 KB	3E0000H–3EFFFFFFH	1F0000H–1F7FFFFH
	BA61	32 KW / 64 KB	3D0000H–3DFFFFFFH	1E8000H–1EFFFFFFH
	BA60	32 KW / 64 KB	3C0000H–3CFFFFFFH	1E0000H–1E7FFFFH
	BA59	32 KW / 64 KB	3B0000H–3BFFFFFFH	1D8000H–1DFFFFFFH
	BA58	32 KW / 64 KB	3A0000H–3AFFFFFFH	1D0000H–1D7FFFFH
	BA57	32 KW / 64 KB	390000H–39FFFFFFH	1C8000H–1CFFFFFFH
	BA56	32 KW / 64 KB	380000H–38FFFFFFH	1C0000H–1C7FFFFH
	BA55	32 KW / 64 KB	370000H–37FFFFFFH	1B8000H–1BFFFFFFH
	BA54	32 KW / 64 KB	360000H–36FFFFFFH	1B0000H–1B7FFFFH
	BA53	32 KW / 64 KB	350000H–35FFFFFFH	1A8000H–1AFFFFFFH
	BA52	32 KW / 64 KB	340000H–34FFFFFFH	1A0000H–1A7FFFFH
	BA51	32 KW / 64 KB	330000H–33FFFFFFH	198000H–19FFFFFFH
	BA50	32 KW / 64 KB	320000H–32FFFFFFH	190000H–197FFFFH
	Bank 2	BA49	32 KW / 64 KB	310000H–31FFFFFFH
BA48		32 KW / 64 KB	300000H–30FFFFFFH	180000H–187FFFFH
BA47		32 KW / 64 KB	2F0000H–2FFFFFFH	178000H–17FFFFFFH
BA46		32 KW / 64 KB	2E0000H–2EFFFFFFH	170000H–177FFFFH
BA45		32 KW / 64 KB	2D0000H–2DFFFFFFH	168000H–16FFFFFFH
BA44		32 KW / 64 KB	2C0000H–2CFFFFFFH	160000H–167FFFFH
BA43		32 KW / 64 KB	2B0000H–2BFFFFFFH	158000H–15FFFFFFH
BA42		32 KW / 64 KB	2A0000H–2AFFFFFFH	150000H–157FFFFH
BA41		32 KW / 64 KB	290000H–29FFFFFFH	148000H–14FFFFFFH
BA40		32 KW / 64 KB	280000H–28FFFFFFH	140000H–147FFFFH
BA39		32 KW / 64 KB	270000H–27FFFFFFH	138000H–13FFFFFFH
BA38		32 KW / 64 KB	260000H–26FFFFFFH	130000H–137FFFFH
BA37		32 KW / 64 KB	250000H–25FFFFFFH	128000H–12FFFFFFH
BA36		32 KW / 64 KB	240000H–24FFFFFFH	120000H–127FFFFH
BA35		32 KW / 64 KB	230000H–23FFFFFFH	118000H–11FFFFFFH
BA34		32 KW / 64 KB	220000H–22FFFFFFH	110000H–117FFFFH
BA33		32 KW / 64 KB	210000H–21FFFFFFH	108000H–10FFFFFFH
BA32		32 KW / 64 KB	200000H–20FFFFFFH	100000H–107FFFFH
BA31		32 KW / 64 KB	1F0000H–1FFFFFFH	0F8000H–0FFFFFFH
BA30		32 KW / 64 KB	1E0000H–1EFFFFFFH	0F0000H–0F7FFFFH
BA29		32 KW / 64 KB	1D0000H–1DFFFFFFH	0E8000H–0EFFFFFFH
BA28		32 KW / 64 KB	1C0000H–1CFFFFFFH	0E0000H–0E7FFFFH
BA27	32 KW / 64 KB	1B0000H–1BFFFFFFH	0D8000H–0DFFFFFFH	
BA26	32 KW / 64 KB	1A0000H–1AFFFFFFH	0D0000H–0D7FFFFH	
BA25	32 KW / 64 KB	190000H–19FFFFFFH	0C8000H–0CFFFFFFH	
BA24	32 KW / 64 KB	180000H–18FFFFFFH	0C0000H–0C7FFFFH	
BA23	32 KW / 64 KB	170000H–17FFFFFFH	0B8000H–0BFFFFFFH	
BA22	32 KW / 64 KB	160000H–16FFFFFFH	0B0000H–0B7FFFFH	



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TABLE 3: Dual-Bank Memory Organization (Continued) (2 of 2)

SST34HF324G	Block	Block Size	Address Range x8	Address Range x16
Bank 2	BA21	32 KW / 64 KB	150000H—15FFFFH	0A8000H—0AFFFFH
	BA20	32 KW / 64 KB	140000H—14FFFFH	0A0000H—0A7FFFH
	BA19	32 KW / 64 KB	130000H—13FFFFH	098000H—09FFFFH
	BA18	32 KW / 64 KB	120000H—12FFFFH	090000H—097FFFH
	BA17	32 KW / 64 KB	110000H—11FFFFH	088000H—08FFFFH
	BA16	32 KW / 64 KB	100000H—10FFFFH	080000H—087FFFH
	BA15	32 KW / 64 KB	0F0000H—0FFFFFH	078000H—07FFFFH
	BA14	32 KW / 64 KB	0E0000H—0EFFFFH	070000H—077FFFH
	BA13	32 KW / 64 KB	0D0000H—0DFFFFH	068000H—06FFFFH
	BA12	32 KW / 64 KB	0C0000H—0CFFFFH	060000H—067FFFH
	BA11	32 KW / 64 KB	0B0000H—0BFFFFH	058000H—05FFFFH
	BA10	32 KW / 64 KB	0A0000H—0AFFFFH	050000H—057FFFH
	BA9	32 KW / 64 KB	090000H—09FFFFH	048000H—04FFFFH
	BA8	32 KW / 64 KB	080000H—08FFFFH	040000H—047FFFH
	BA7	32 KW / 64 KB	070000H—07FFFFH	038000H—03FFFFH
	BA6	32 KW / 64 KB	060000H—06FFFFH	030000H—037FFFH
	BA5	32 KW / 64 KB	050000H—05FFFFH	028000H—02FFFFH
	BA4	32 KW / 64 KB	040000H—04FFFFH	020000H—027FFFH
	BA3	32 KW / 64 KB	030000H—03FFFFH	018000H—01FFFFH
	BA2	32 KW / 64 KB	020000H—02FFFFH	010000H—017FFFH
BA1	32 KW / 64 KB	010000H—01FFFFH	008000H—00FFFFH	
BA0	32 KW / 64 KB	000000H—00FFFFH	000000H—007FFFH	

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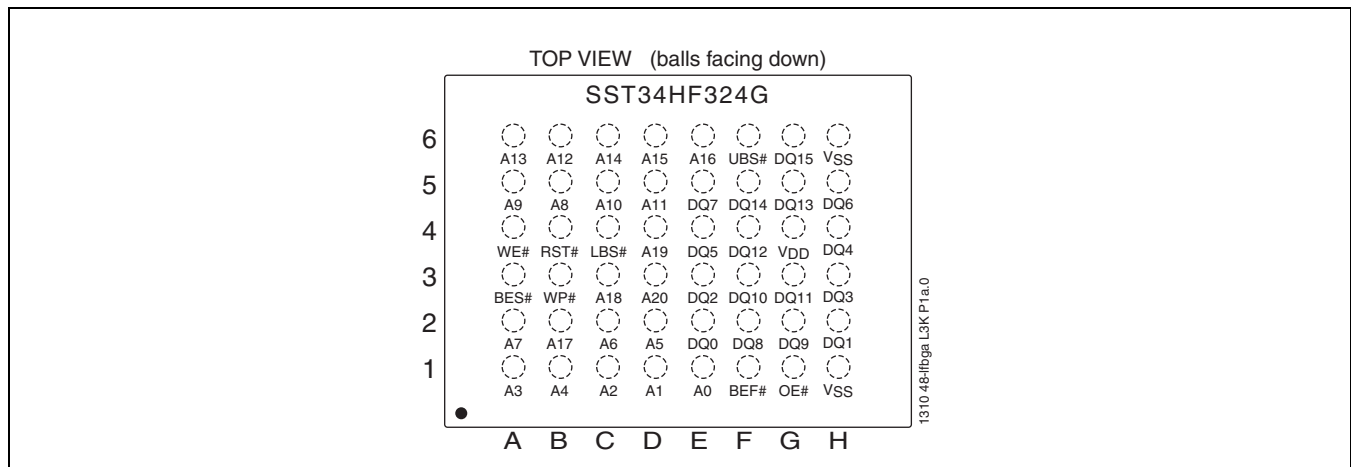


FIGURE 2: Pin Assignments for 48-ball LFBGA (6mm x 8mm)



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TABLE 4: Pin Description

Symbol	Pin Name	Functions
A_{MS}^1 to A_0	Address Inputs	To provide Flash address, $A_{20}-A_0$. To provide SRAM address, $A_{17}-A_0$
$DQ_{15}-DQ_0$	Data Inputs/Outputs	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when $OE\#$, $BES\#$, and $BEF\#$ are high.
$BEF\#$	Flash Memory Bank Enable	To activate the Flash memory bank when $BEF\#$ is low
$BES\#$	SRAM Memory Bank Enable	To activate the SRAM memory bank when $BES\#$ is low
$OE\#$	Output Enable	To gate the data output buffers
$WE\#$	Write Enable	To control the Write operations
$UBS\#$	Upper Byte Control (SRAM)	To enable $DQ_{15}-DQ_8$
$LBS\#$	Lower Byte Control (SRAM)	To enable DQ_7-DQ_0
$WP\#$	Write Protect	To protect and unprotect the bottom 8 KWord (4 sectors) from Erase or Program operation
$RST\#$	Reset	To Reset and return the device to Read mode
V_{SS}	Ground	
V_{DD}	Power Supply	2.7-3.3V Power Supply

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1. A_{MS} = Most Significant Address



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TABLE 5: Operational Modes Selection for SRAM

Mode	BEF# ¹	BES# ^{1,2}	OE# ²	WE# ²	LBS# ²	UBS# ²	DQ ₁₅₋₀	DQ ₁₅₋₈	
Full Standby	V _{IH}	V _{IH}	X	X	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		X	X	X	X	X			
Output Disable	V _{IH}	V _{IL}	V _{IH}	V _{IH}	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		V _{IL}	X	X	V _{IH}	V _{IH}			
	V _{IL}	V _{IH}	V _{IH}	V _{IH}	X	X	HIGH-Z	HIGH-Z	HIGH-Z
Flash Read	V _{IL}	V _{IH}	V _{IL}	V _{IH}	X	X	D _{OUT}	D _{OUT}	DQ ₁₅₋₈ =HIGH-Z
		X							
Flash Write	V _{IL}	V _{IH}	V _{IH}	V _{IL}	X	X	D _{IN}	D _{IN}	DQ ₁₅₋₈ =HIGH-Z
		X							
Flash Erase	V _{IL}	V _{IH}	V _{IH}	V _{IL}	X	X	X	X	X
		X							
SRAM Read	V _{IH}	V _{IL}	V _{IL}	V _{IH}	V _{IL}	V _{IL}	D _{OUT}	D _{OUT}	D _{OUT}
					V _{IH}	V _{IL}	HIGH-Z	D _{OUT}	D _{OUT}
					V _{IL}	V _{IH}	D _{OUT}	HIGH-Z	HIGH-Z
SRAM Write	V _{IH}	V _{IL}	X	V _{IL}	V _{IL}	V _{IL}	D _{IN}	D _{IN}	D _{IN}
					V _{IH}	V _{IL}	HIGH-Z	D _{IN}	D _{IN}
					V _{IL}	V _{IH}	D _{IN}	HIGH-Z	HIGH-Z
Product Identification ³	V _{IL}	V _{IH}	V _{IL}	V _{IH}	X	X	Manufacturer's ID ⁴ Device ID ⁴		

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1. Do not apply BEF# = V_{IL} and BES# = V_{IL} at the same time
2. X can be V_{IL} or V_{IH}, but no other value.
3. Software mode only
4. With A₂₀-A₁₈ = V_{IL}, SST Manufacturer's ID = BFH, is read with A₀=0,
SST34HF324G Device ID = 7353H, is read with A₀=1



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TABLE 6: Software Command Sequence

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²	Addr ¹	Data ²
Program	555H	AAH	2AAH	55H	555H	A0H	WA ³	Data				
Sector-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA _X ⁴	50H
Block-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA _X ⁴	30H
Chip-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Erase-Suspend	XXXXH	B0H										
Erase-Resume	XXXXH	30H										
Software ID Entry ⁵	555H	AAH	2AAH	55H	BK _X ⁶ 555H	90H						
Software ID Exit	555H	AAH	2AAH	55H	555H	F0H						
Software ID Exit	XXH	F0H										

T6.0 1310

1. Address format A₁₀-A₀ (Hex), Addresses A₂₀-A₁₁ can be V_{IL} or V_{IH}, but no other value, for the command sequence.
2. DQ₁₅-DQ₈ can be V_{IL} or V_{IH}, but no other value, for the command sequence
3. WA = Program word address
4. SA_X for Sector-Erase; uses A₂₀-A₁₁ address lines
BA_X for Block-Erase; uses A₂₀-A₁₅ address lines
BK_X for Bank address; uses A₂₀-A₁₅ address lines
5. The device does not remain in Software Product Identification mode if powered down.
6. A₂₀-A₁₈ = V_{IL}

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under “Absolute Maximum Stress Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature -20°C to +85°C
 Storage Temperature -65°C to +125°C
 D. C. Voltage on Any Pin to Ground Potential -0.5V to V_{DD}+0.3V
 Transient Voltage (<20 ns) on Any Pin to Ground Potential -1.0V to V_{DD}+1.0V
 Package Power Dissipation Capability (Ta = 25°C) 1.0W
 Surface Mount Solder Reflow Temperature: 260°C for 10 seconds
 Output Short Circuit Current¹ 50 mA

1. Outputs shorted for no more than one second. No more than one output shorted at a time.

Operating Range

Range	Ambient Temp	V _{DD}
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

AC Conditions of Test

Input Rise/Fall Time	5 ns
Output Load	C _L = 30 pF
See Figures 18 and 19	



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TABLE 7: DC Operating Characteristics ($V_{DD} = V_{DDF}$ and $V_{DDs} = 2.7-3.3V$)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}^1	Active V_{DD} Current				Address input = V_{ILT}/V_{IHT} , at $f=5$ MHz, $V_{DD}=V_{DD}$ Max, all DQs open
	Read				$OE\#=V_{IL}$, $WE\#=V_{IH}$
	Flash		15	mA	$BEF\#=V_{IL}$, $BES\#=V_{IH}$
	SRAM		10	mA	$BEF\#=V_{IH}$, $BES\#=V_{IL}$
	Concurrent Operation		45	mA	$BEF\#=V_{IH}$, $BES\#=V_{IL}$
	Write ²				$WE\#=V_{IL}$
	Flash		40	mA	$BEF\#=V_{IL}$, $BES\#=V_{IH}$, $OE\#=V_{IH}$
	SRAM		30	mA	$BEF\#=V_{IH}$, $BES\#=V_{IL}$
I_{SB}	Standby V_{DD} Current		30	μA	$V_{DD} = V_{DD}$ Max, $BEF\#=BES\#=V_{IHC}$
I_{RT}	Reset V_{DD} Current		30	μA	$RST\#=GND$
I_{LI}	Input Leakage Current		1	μA	$V_{IN}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
I_{LIW}	Input Leakage Current on WP# pin and RST# pin		10	μA	$WP\#=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max $RST\#=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	μA	$V_{OUT}=GND$ to V_{DD} , $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	$V_{DD}=V_{DD}$ Max
V_{IH}	Input High Voltage	0.7 V_{DD}		V	$V_{DD}=V_{DD}$ Max
V_{IHC}	Input High Voltage (CMOS)	$V_{DD}-0.3$		V	$V_{DD}=V_{DD}$ Max
V_{OL}	Flash and SRAM Output Low Voltage		0.2	V	$I_{OL}=100 \mu A$, $V_{DD}=V_{DD}$ Min
V_{OH}	Flash and SRAM Output High Voltage	$V_{DD}-0.2$		V	$I_{OH}=-100 \mu A$, $V_{DD}=V_{DD}$ Min

T7.0 1310

1. See Figure 18
2. I_{DD} active while Erase or Program is in progress.



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TABLE 8: Recommended System Power-up Timings

Symbol	Parameter	Minimum	Units
$T_{PU-READ}^1$	Power-up to Read Operation	100	μs
$T_{PU-WRITE}^1$	Power-up to Write Operation	100	μs

T8.0 1310

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: Capacitance ($T_a = 25^\circ C$, $f=1$ Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}^1$	I/O Pin Capacitance	$V_{I/O} = 0V$	20 pF
C_{IN}^1	Input Capacitance	$V_{IN} = 0V$	16 pF

T9.0 1310

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 10: Flash Reliability Characteristics

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}^1	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}^1	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}^1	Latch Up	$100 + I_{DD}$	mA	JEDEC Standard 78

T10.0 1310

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



Data Sheet

AC CHARACTERISTICS

TABLE 11: SRAM Read Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T _{RCS}	Read Cycle Time	70		ns
T _{AAS}	Address Access Time		70	ns
T _{BES}	Bank Enable Access Time		70	ns
T _{OES}	Output Enable Access Time		35	ns
T _{BYES}	UBS#, LBS# Access Time		70	ns
T _{BLZS} ¹	BES# to Active Output	0		ns
T _{OLZS} ¹	Output Enable to Active Output	0		ns
T _{BYLZS} ¹	UBS#, LBS# to Active Output	0		ns
T _{BHZS} ¹	BES# to High-Z Output		25	ns
T _{OHZS} ¹	Output Disable to High-Z Output		25	ns
T _{BYHZS} ¹	UBS#, LBS# to High-Z Output		35	ns
T _{OHS}	Output Hold from Address Change	10		ns

T11.0 1310

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 12: SRAM Write Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T _{WCS}	Write Cycle Time	70		ns
T _{BWS}	Bank Enable to End-of-Write	60		ns
T _{AWS}	Address Valid to End-of-Write	60		ns
T _{ASTS}	Address Set-up Time	0		ns
T _{WPS}	Write Pulse Width	60		ns
T _{WRS}	Write Recovery Time	0		ns
T _{BYWS}	UBS#, LBS# to End-of-Write	60		ns
T _{ODWS}	Output Disable from WE# Low		30	ns
T _{OEWS}	Output Enable from WE# High	0		ns
T _{DSS}	Data Set-up Time	30		ns
T _{DHS}	Data Hold from Write Time	0		ns

T12.0 1310

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TABLE 13: Flash Read Cycle Timing Parameters $V_{DD} = 2.7-3.3V$

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	70		ns
T_{CE}	Chip Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		35	ns
T_{CLZ}^1	BEF# Low to Active Output	0		ns
T_{OLZ}^1	OE# Low to Active Output	0		ns
T_{CHZ}^1	BEF# High to High-Z Output		16	ns
T_{OHZ}^1	OE# High to High-Z Output		16	ns
T_{OH}^1	Output Hold from Address Change	0		ns
$T_{RP}^{1,2}$	RST# Pulse Width	500		ns
$T_{RHR}^{1,2}$	RST# High Before Read	50		ns
$T_{RY}^{1,2,3}$	RST# Pin Low to Read		20	μ s

T13.0 1310

1. This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.
2. L3K package only
3. This parameter applies to Sector-Erase, Block-Erase and Program operations. This parameter does not apply to Chip-Erase.

TABLE 14: Flash Program/Erase Cycle Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{BP}	Program Time		12	μ s
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{CS}	WE# and BEF# Setup Time	0		ns
T_{CH}	WE# and BEF# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	BEF# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}^1	WE# Pulse Width High	30		ns
T_{CPH}^1	BEF# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}^1	Data Hold Time	0		ns
T_{IDA}^1	Software ID Access and Exit Time		150	ns
T_{ES}	Erase-Suspend Latency		10	μ s
T_{BR}^1	Bus# Recovery Time		1	μ s
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms

T14.1 1310

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



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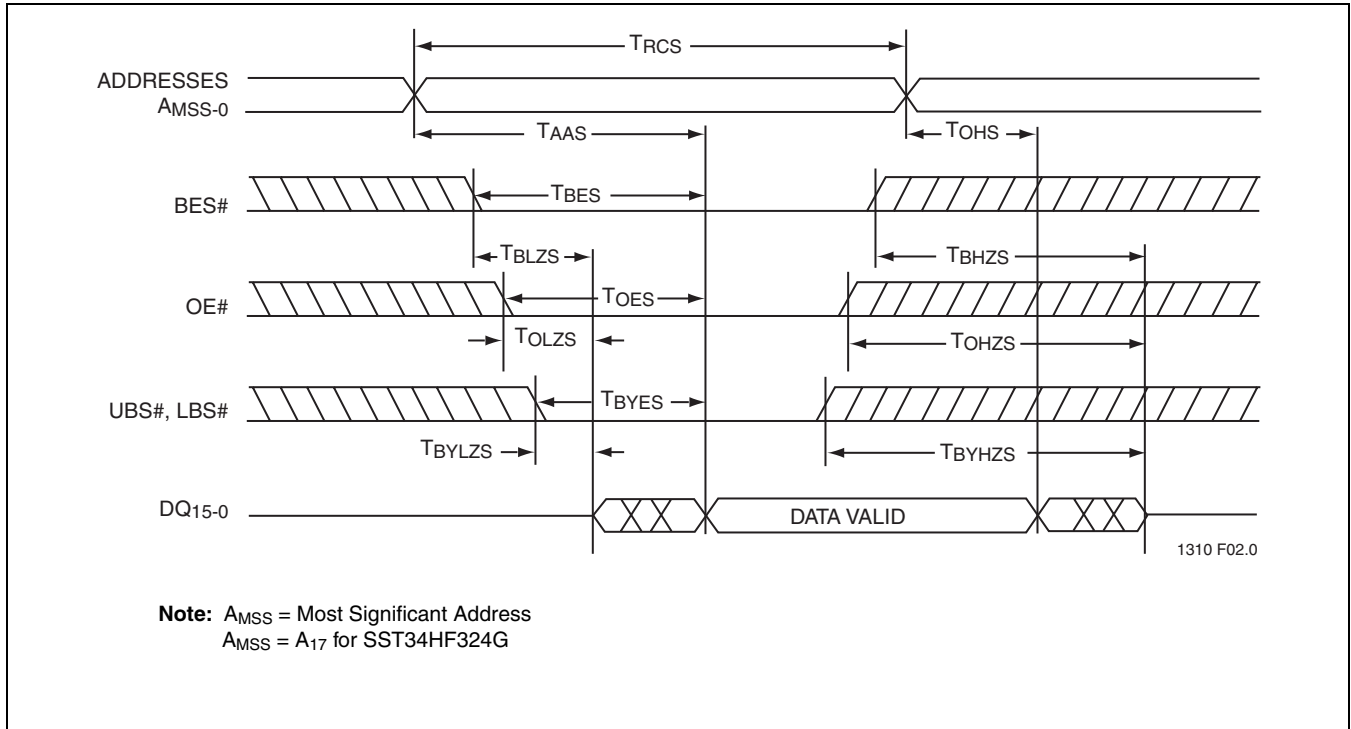


FIGURE 3: SRAM Read Cycle Timing Diagram

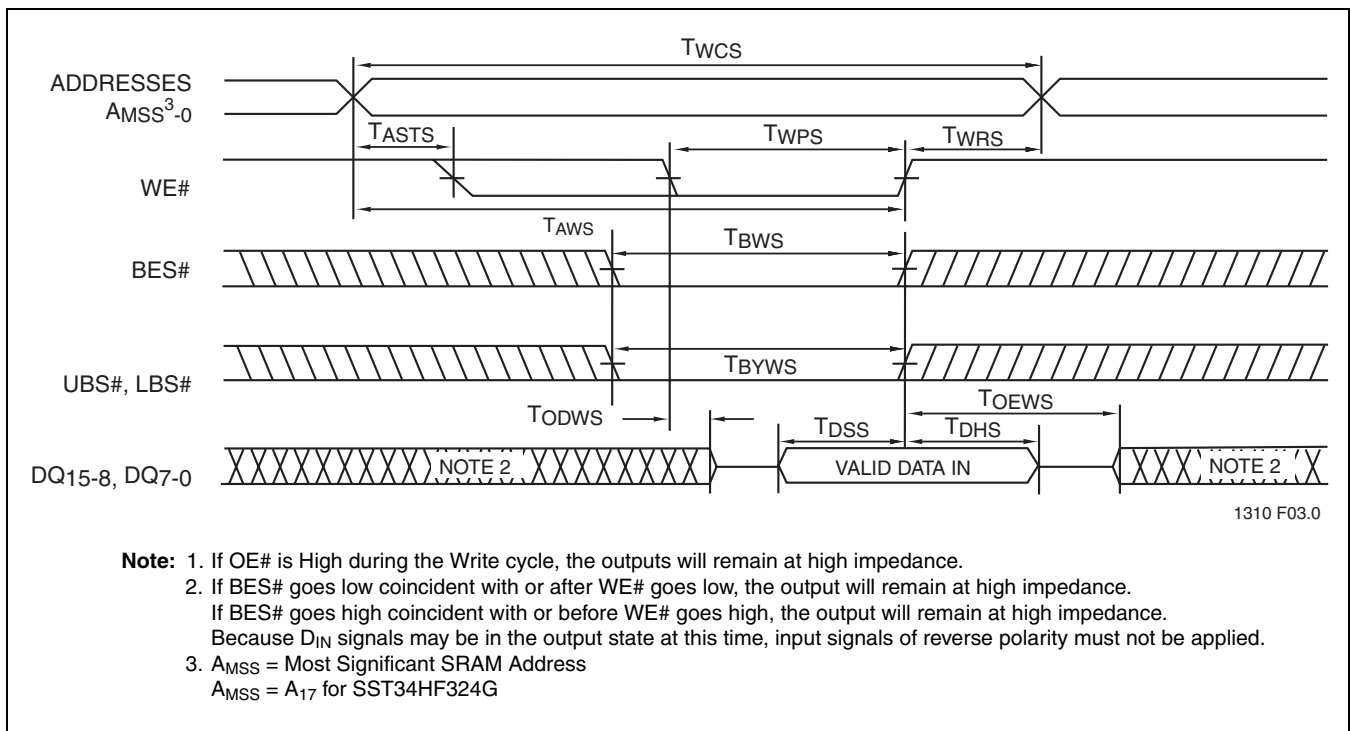


FIGURE 4: SRAM Write Cycle Timing Diagram (WE# Controlled)

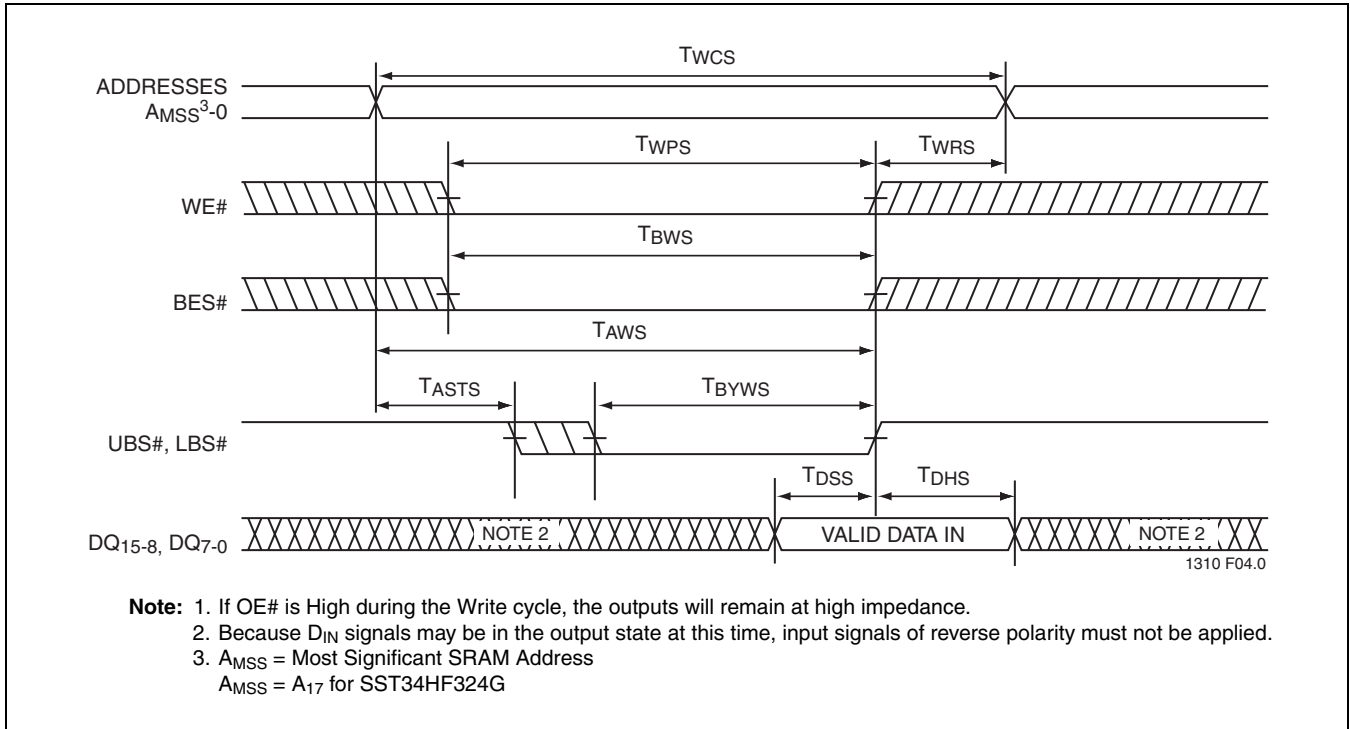


FIGURE 5: SRAM Write Cycle Timing Diagram (UBS#, LBS# Controlled)

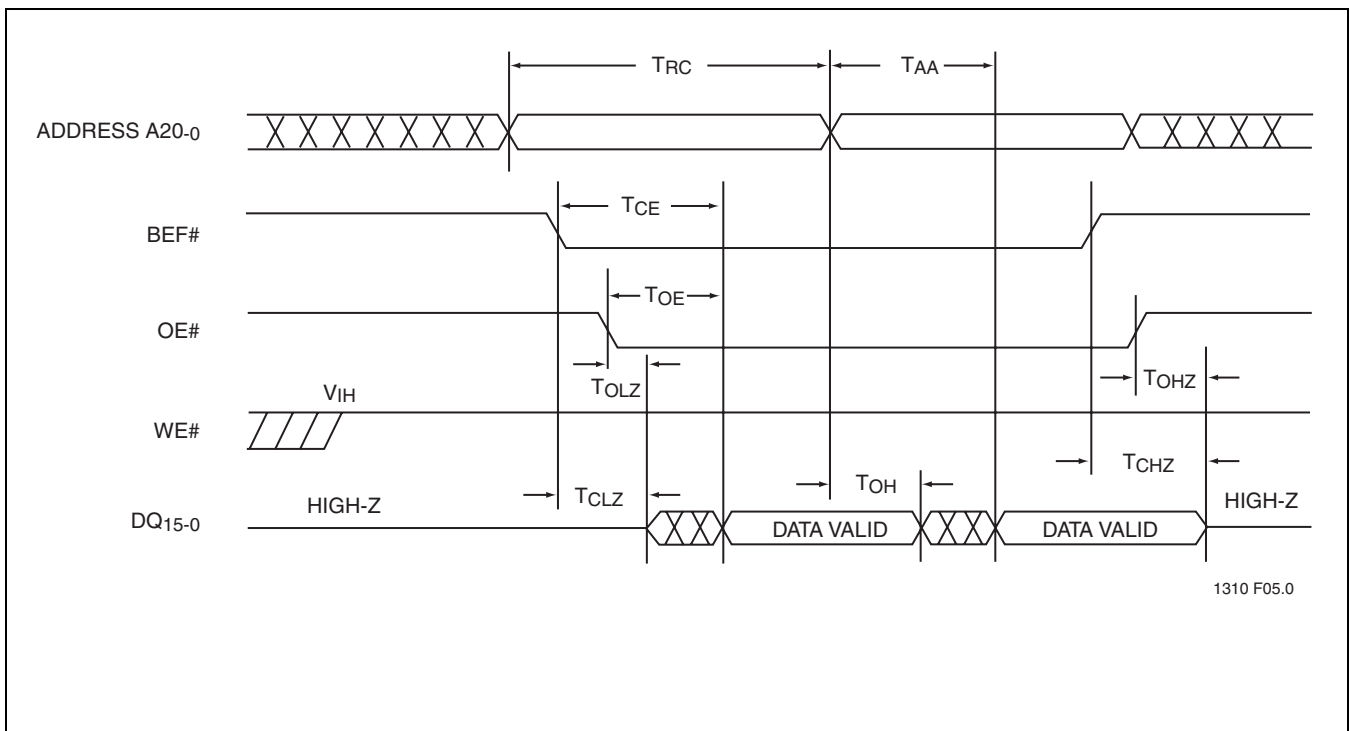


FIGURE 6: Flash Read Cycle Timing Diagram



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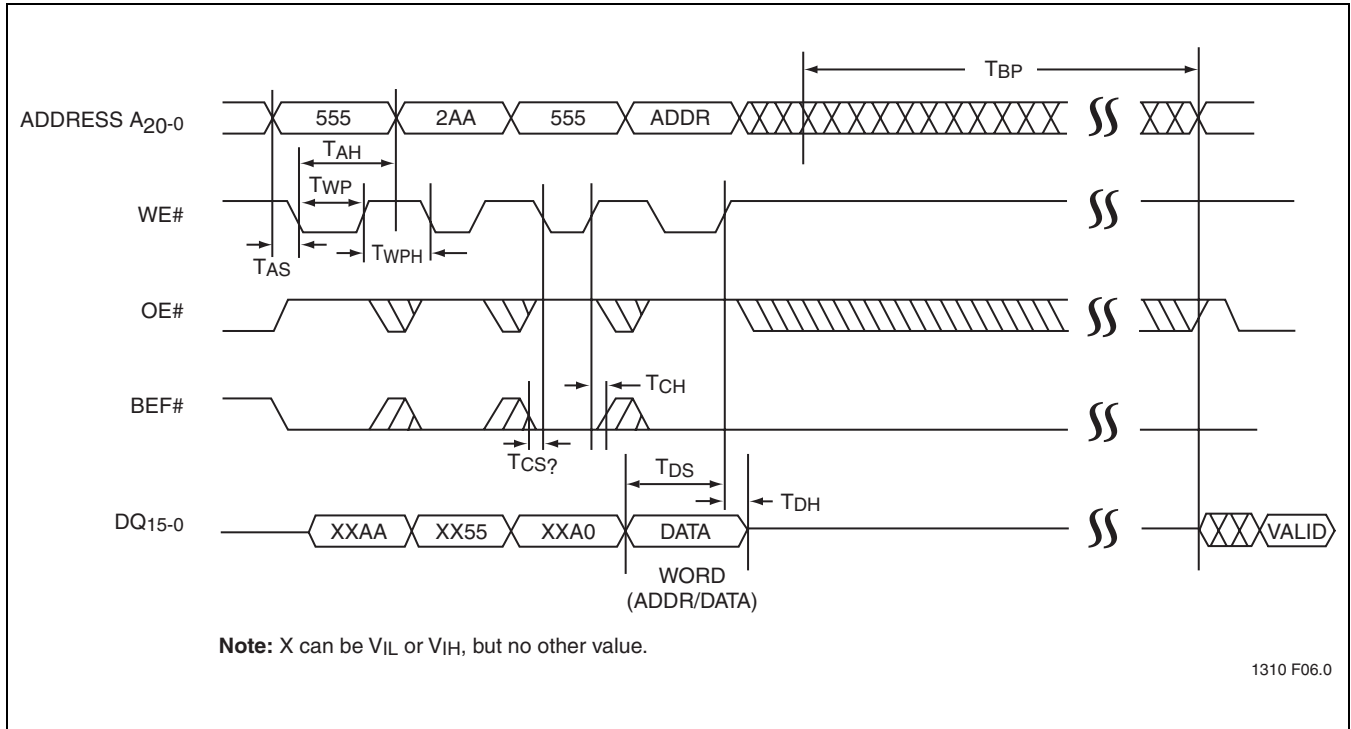


FIGURE 7: Flash WE# Controlled Program Cycle Timing Diagram

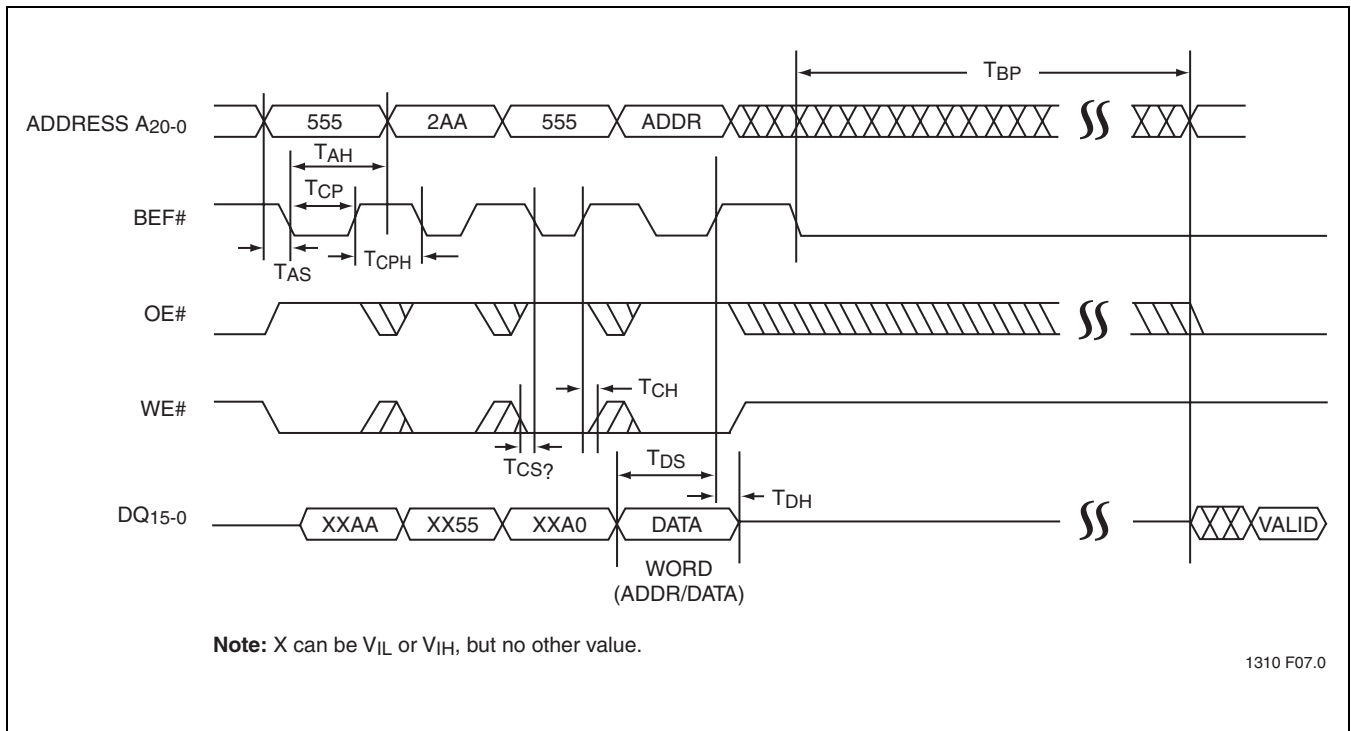


FIGURE 8: Flash BEF# Controlled Program Cycle Timing Diagram

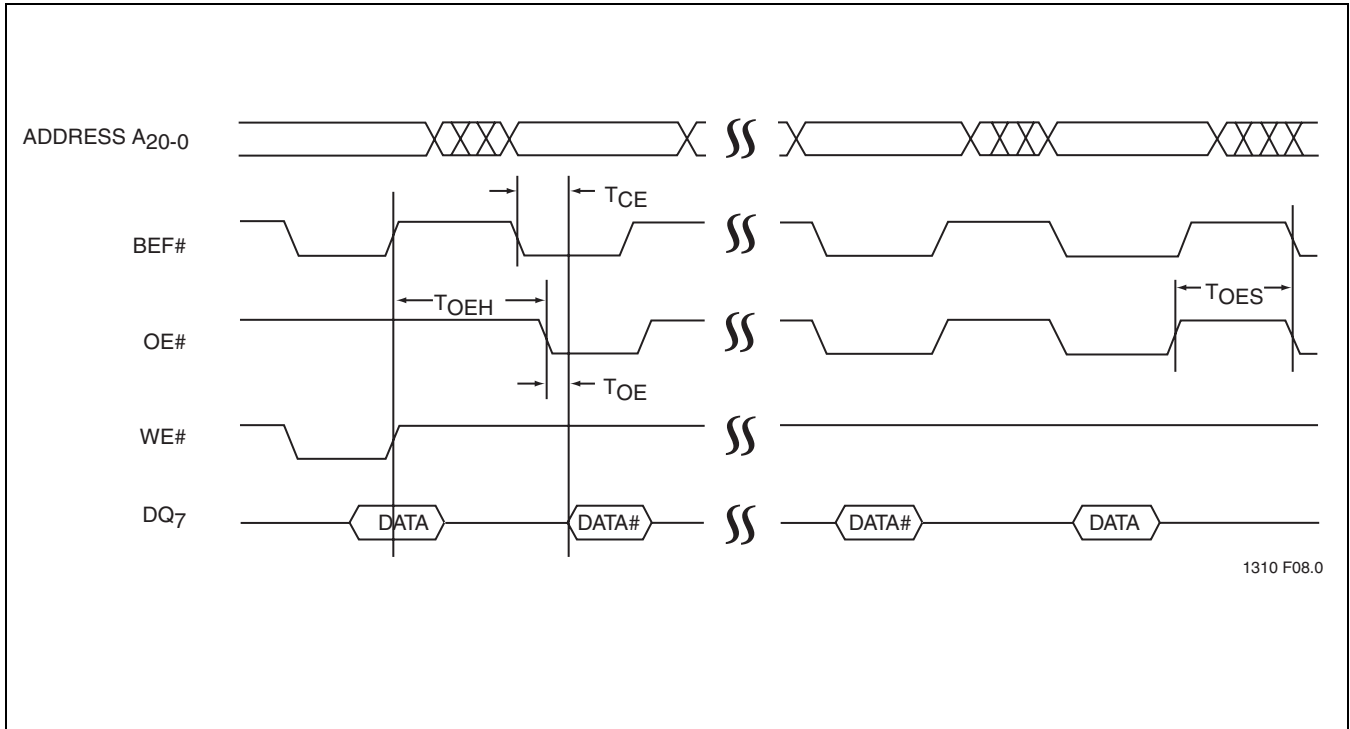


FIGURE 9: Flash Data# Polling Timing Diagram

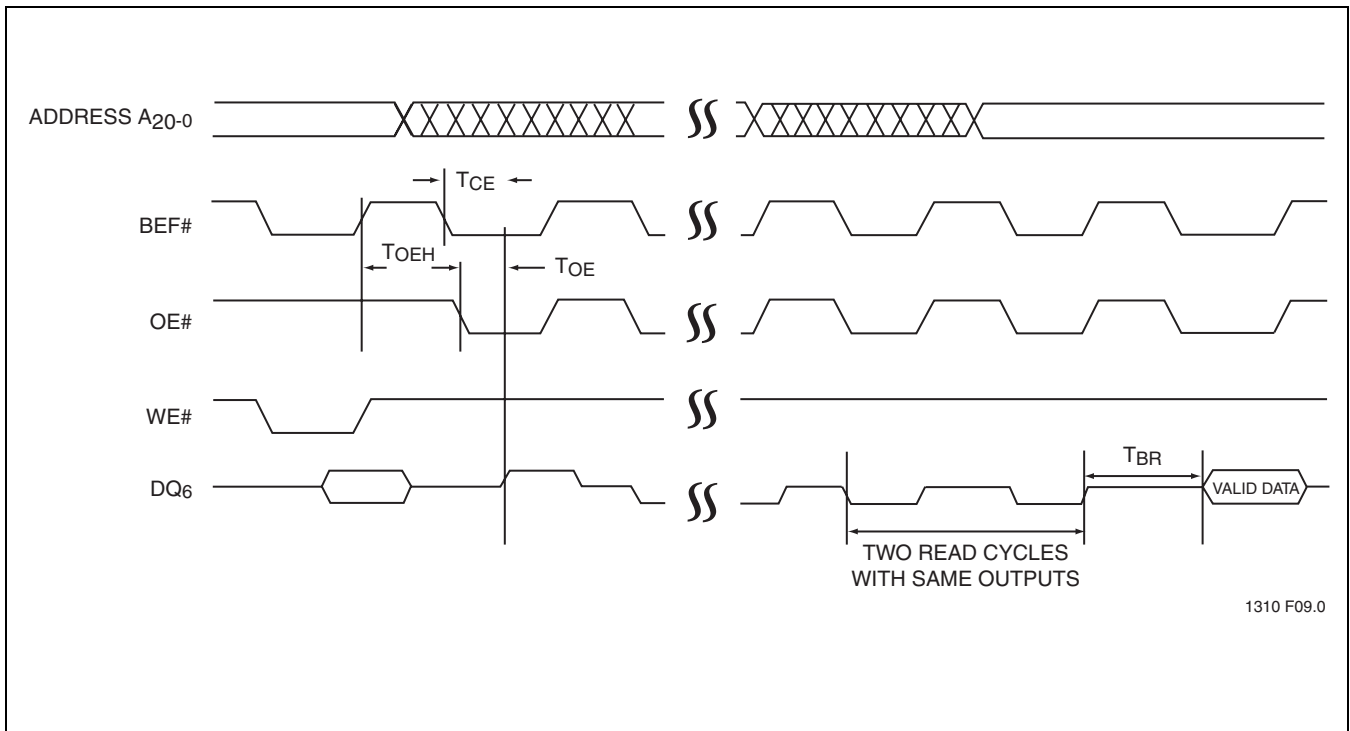


FIGURE 10: Flash Toggle Bit Timing Diagram



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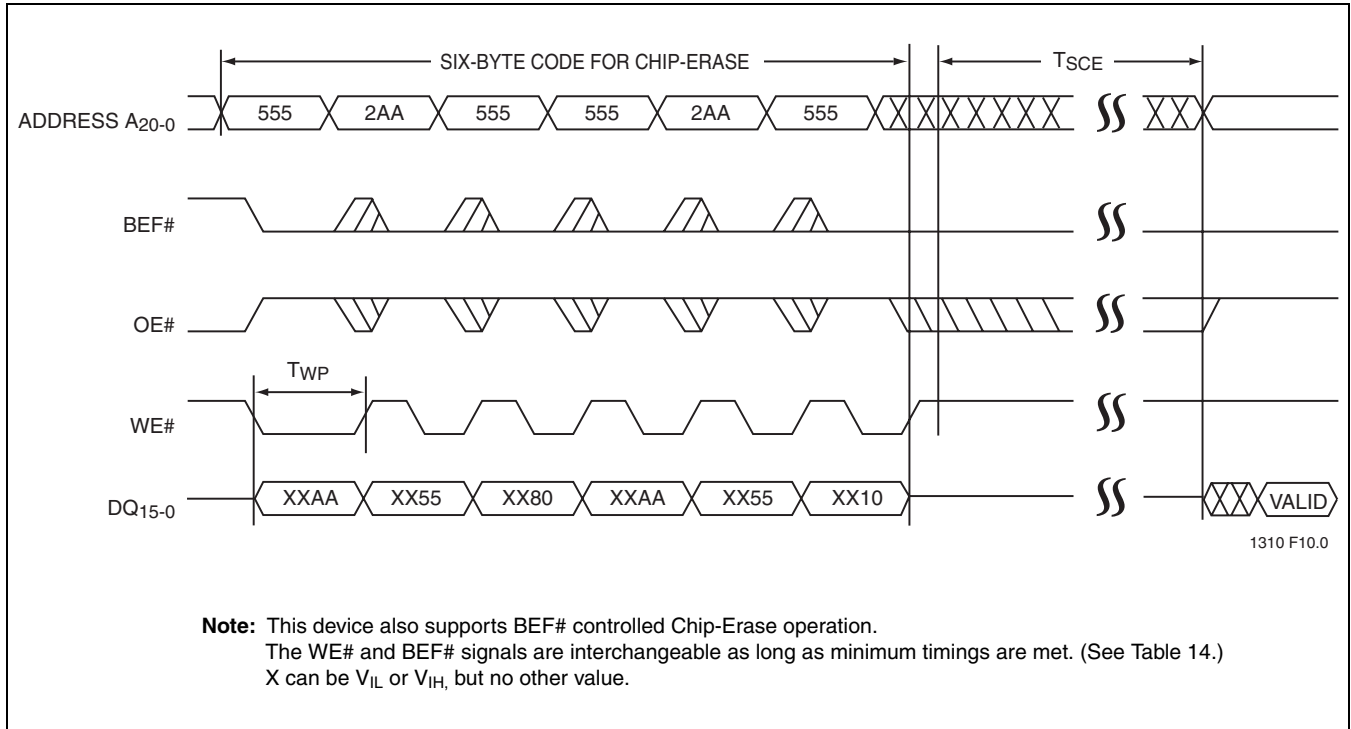


FIGURE 11: Flash WE# Controlled Chip-Erase Timing Diagram

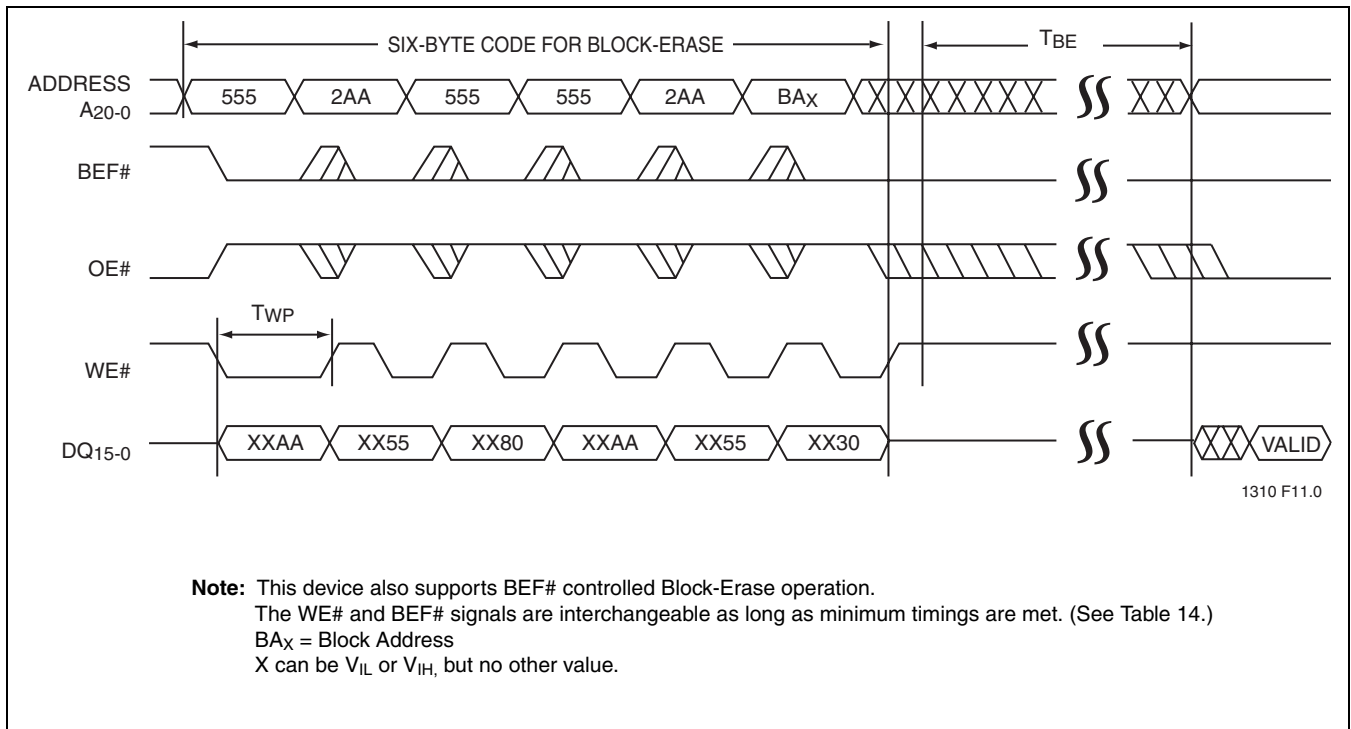


FIGURE 12: Flash WE# Controlled Block-Erase Timing Diagram

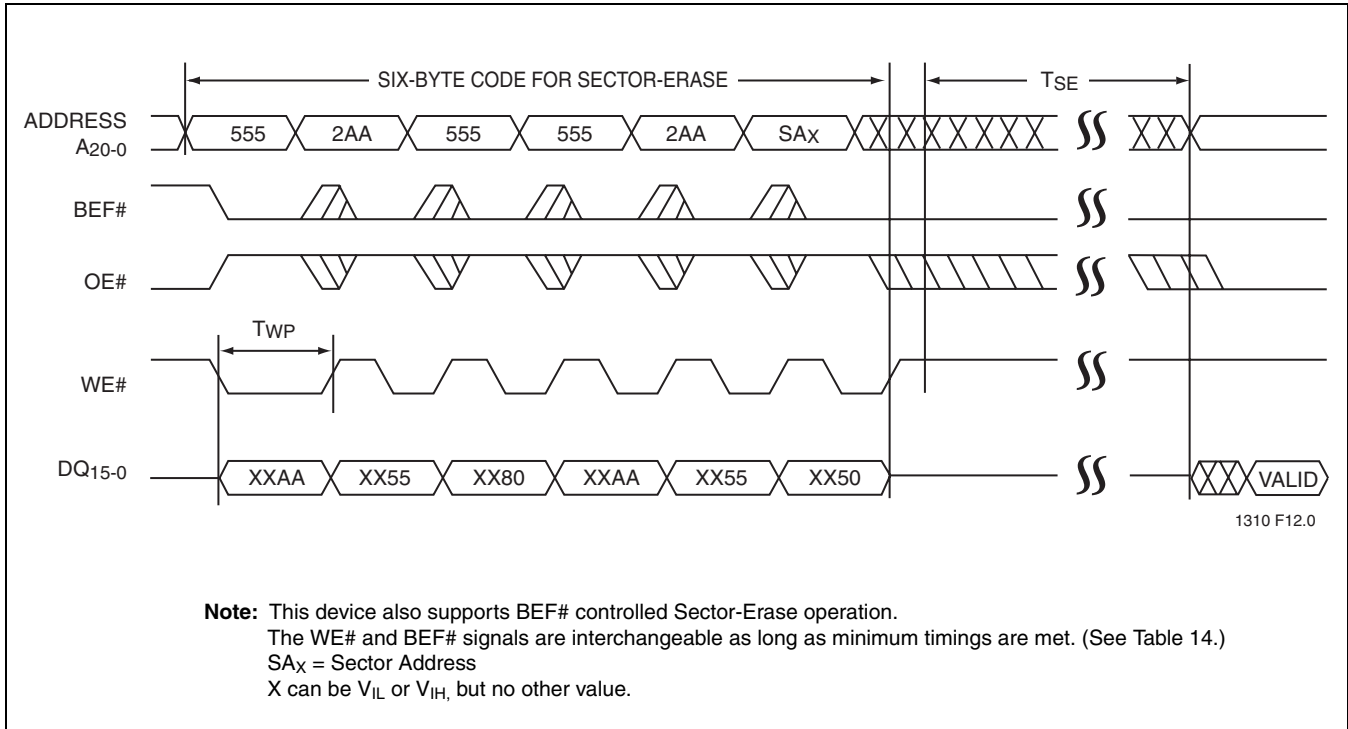


FIGURE 13: Flash WE# Controlled Sector-Erase Timing Diagram

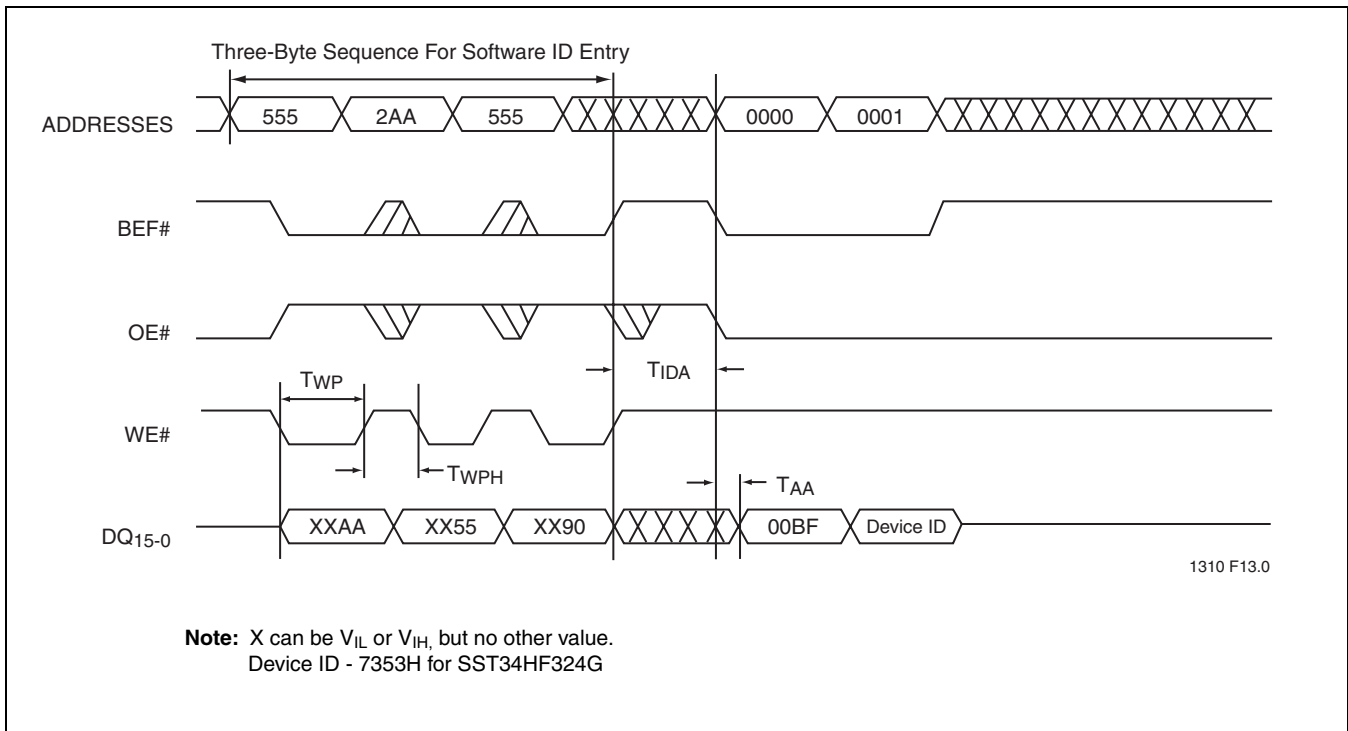


FIGURE 14: Flash Software ID Entry and Read

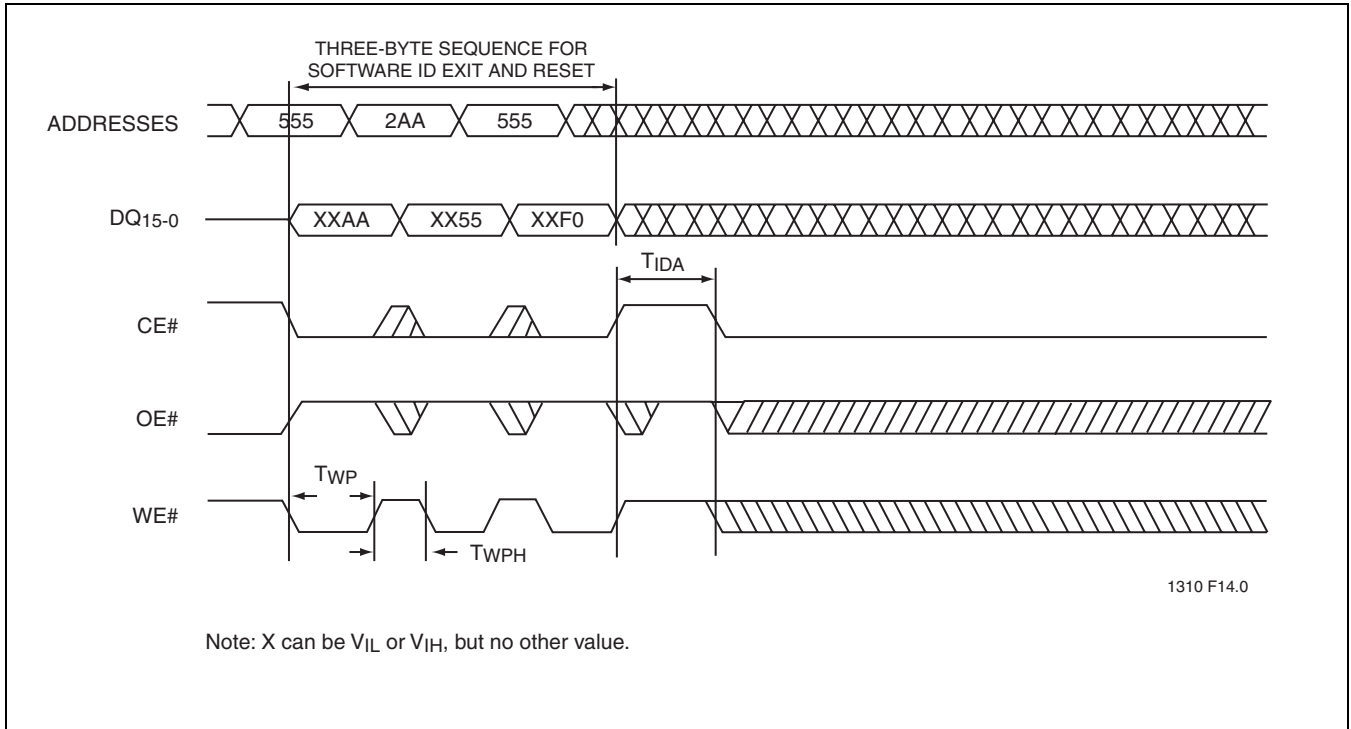


FIGURE 15: Flash Software ID Exit

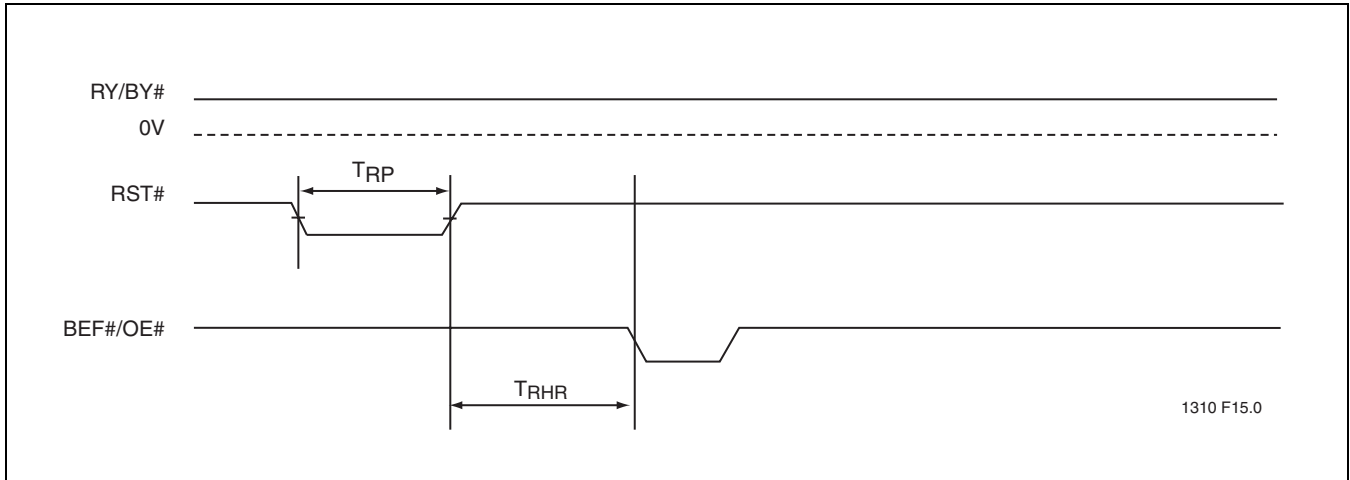


FIGURE 16: RST# Timing (when no internal operation is in progress)

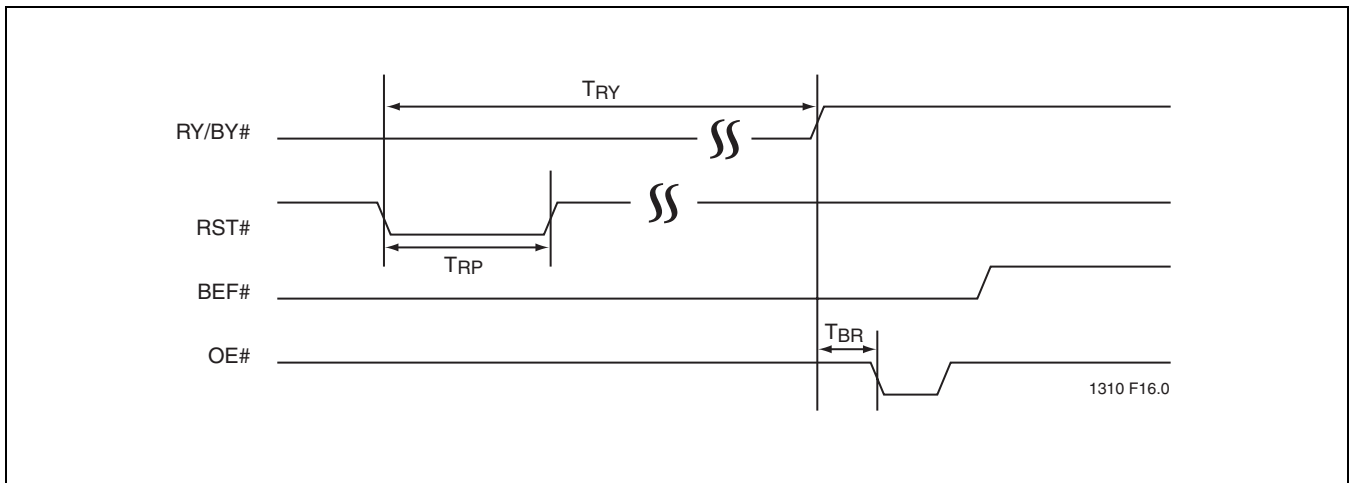
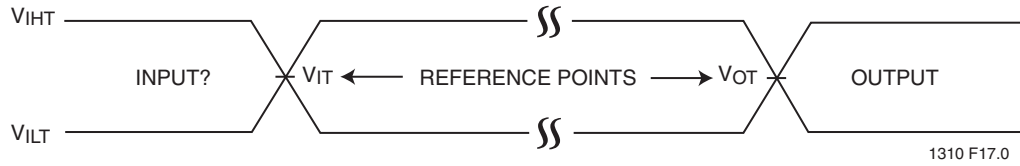


FIGURE 17: RST# Timing (during Sector- or Block-Erase operation)



AC test inputs are driven at V_{IHT} ($0.9 V_{DD}$) for a logic "1" and V_{ILT} ($0.1 V_{DD}$) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} ($0.5 V_{DD}$) and V_{OT} ($0.5 V_{DD}$). Input rise and fall times (10% \leftrightarrow 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
 V_{OT} - V_{OUTPUT} Test
 V_{IHT} - V_{INPUT} HIGH Test
 V_{ILT} - V_{INPUT} LOW Test

FIGURE 18: AC Input/Output Reference Waveforms

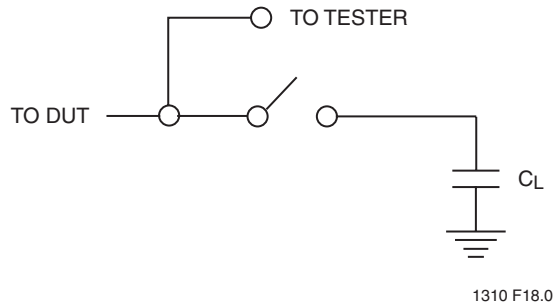


FIGURE 19: A Test Load Example

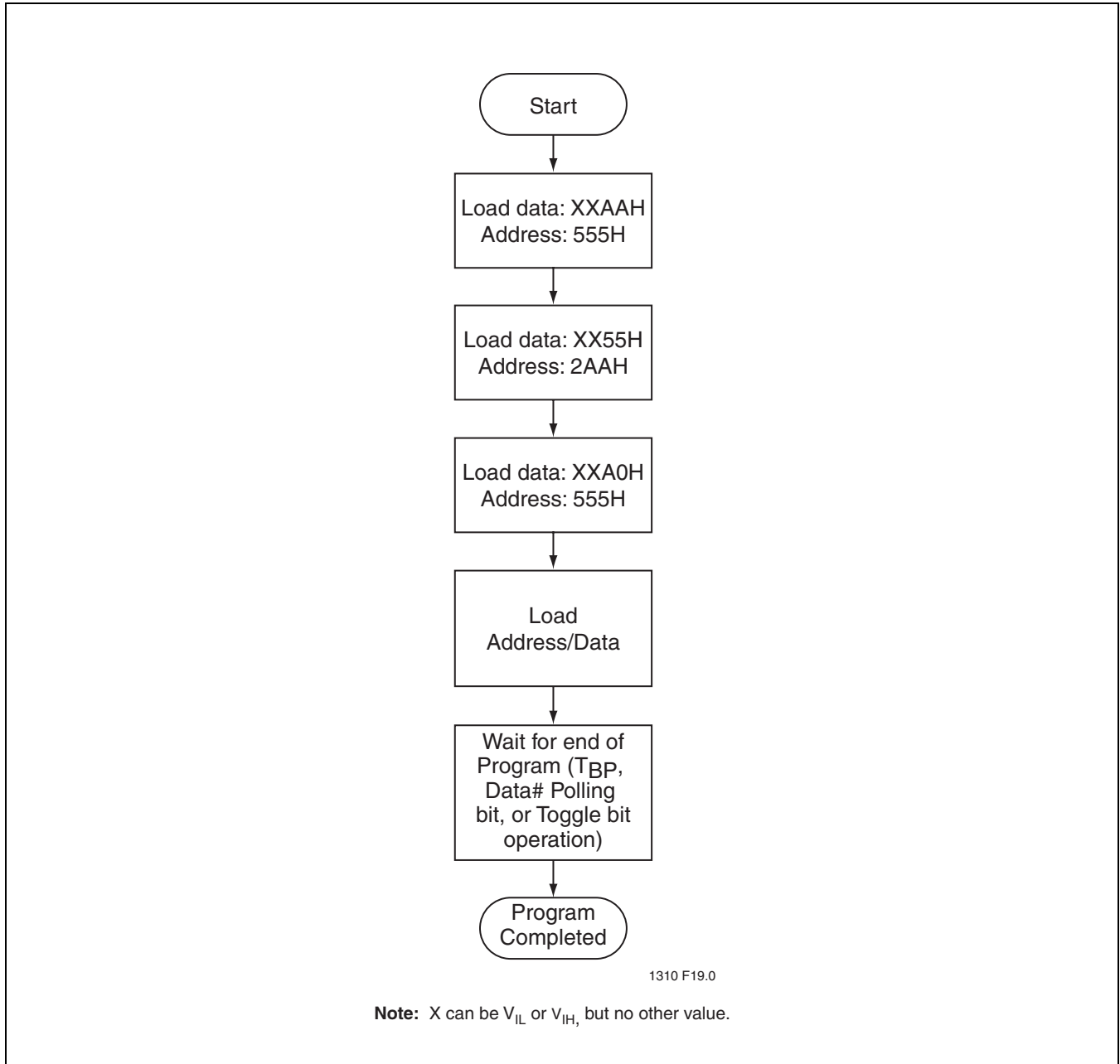


FIGURE 20: Program Algorithm

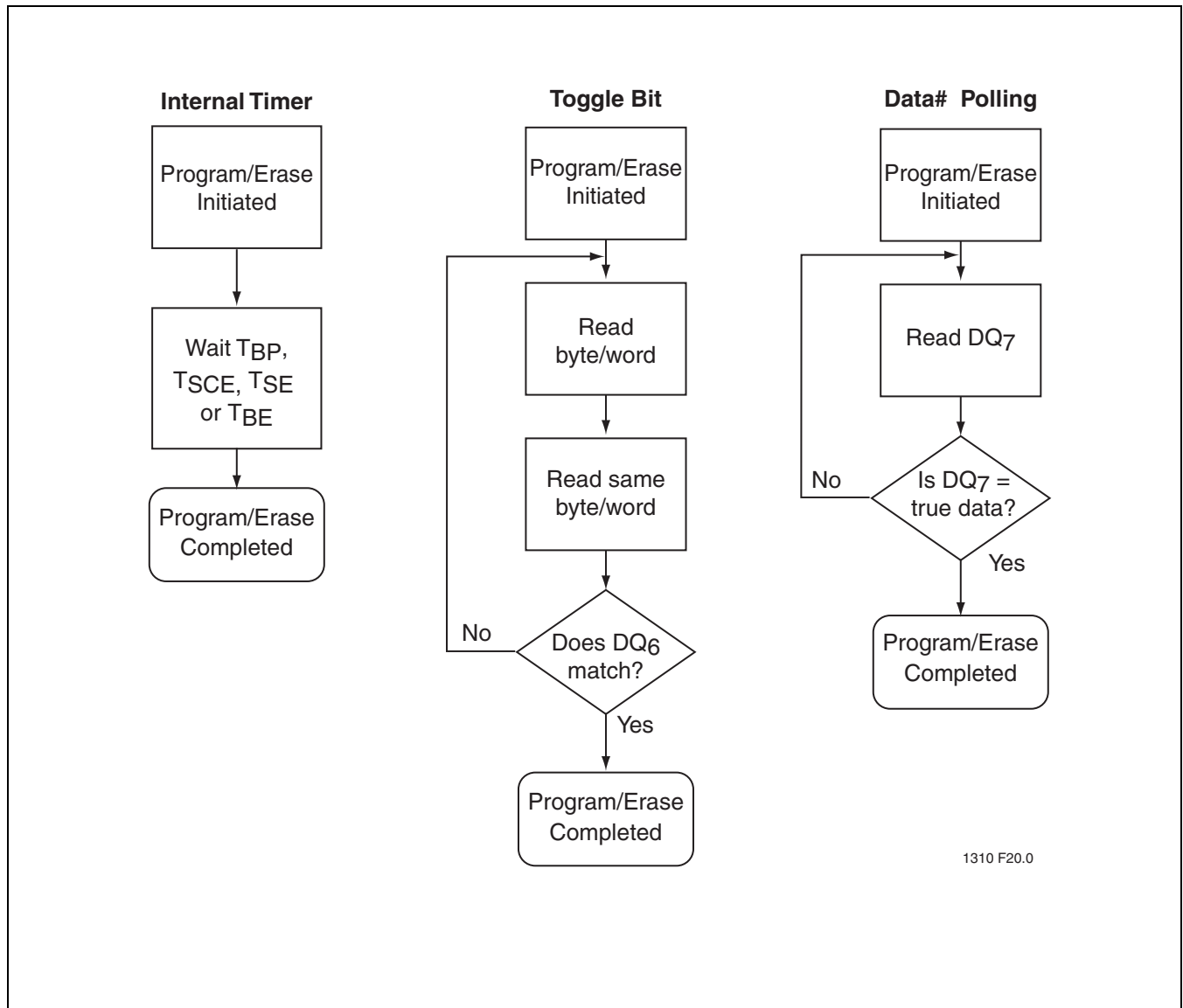


FIGURE 21: Wait Options

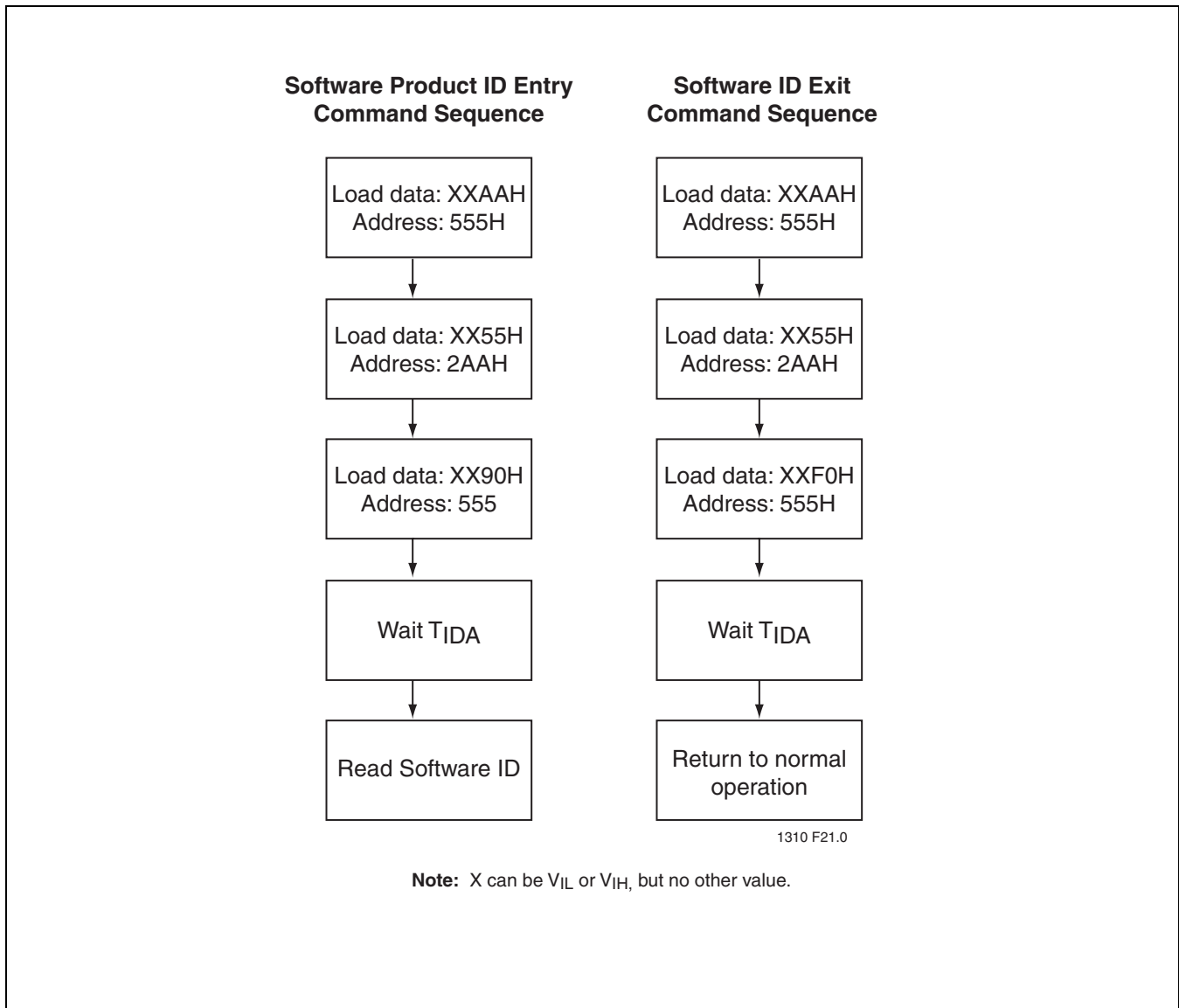


FIGURE 22: Software Product ID Command Flowcharts

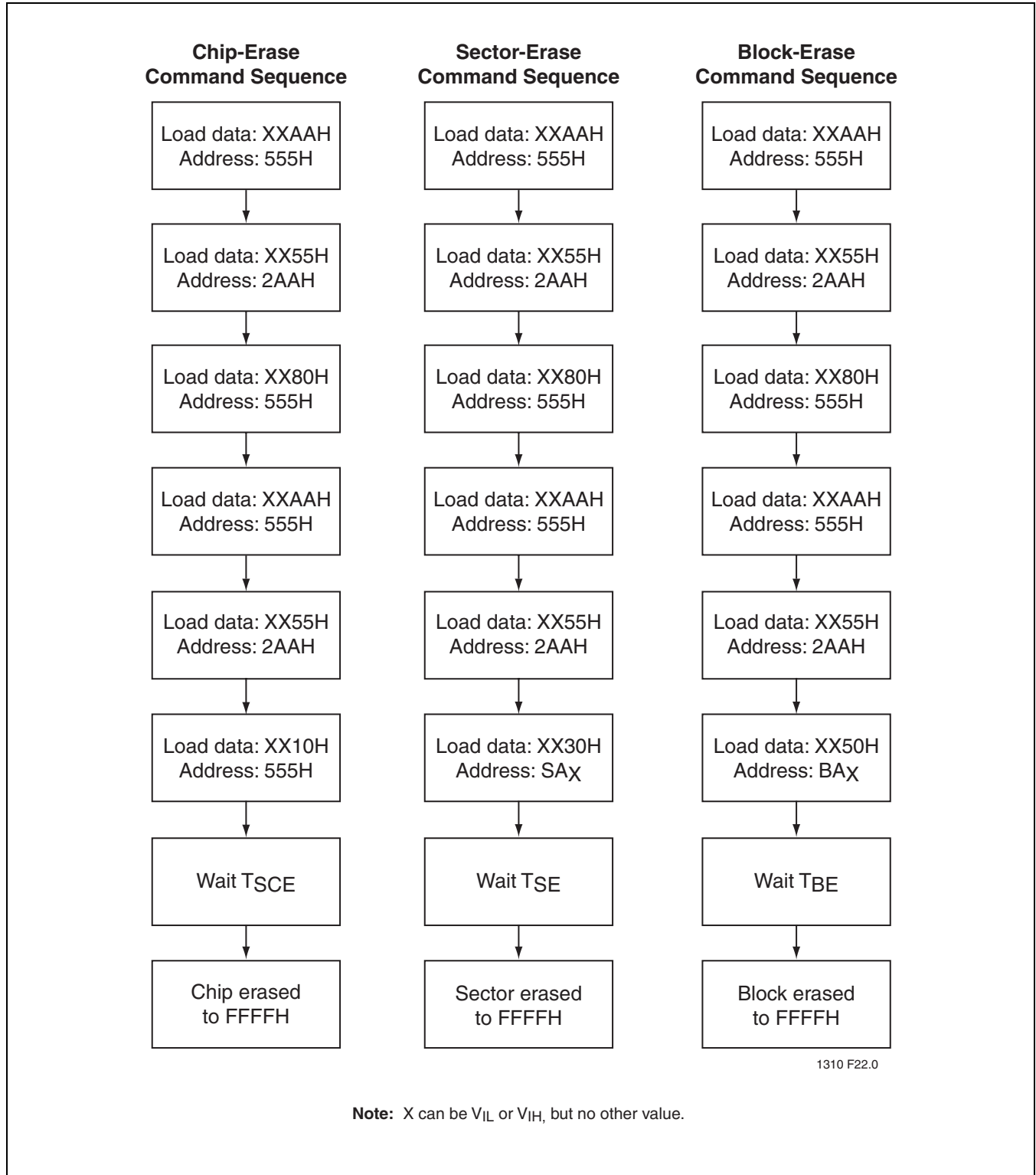


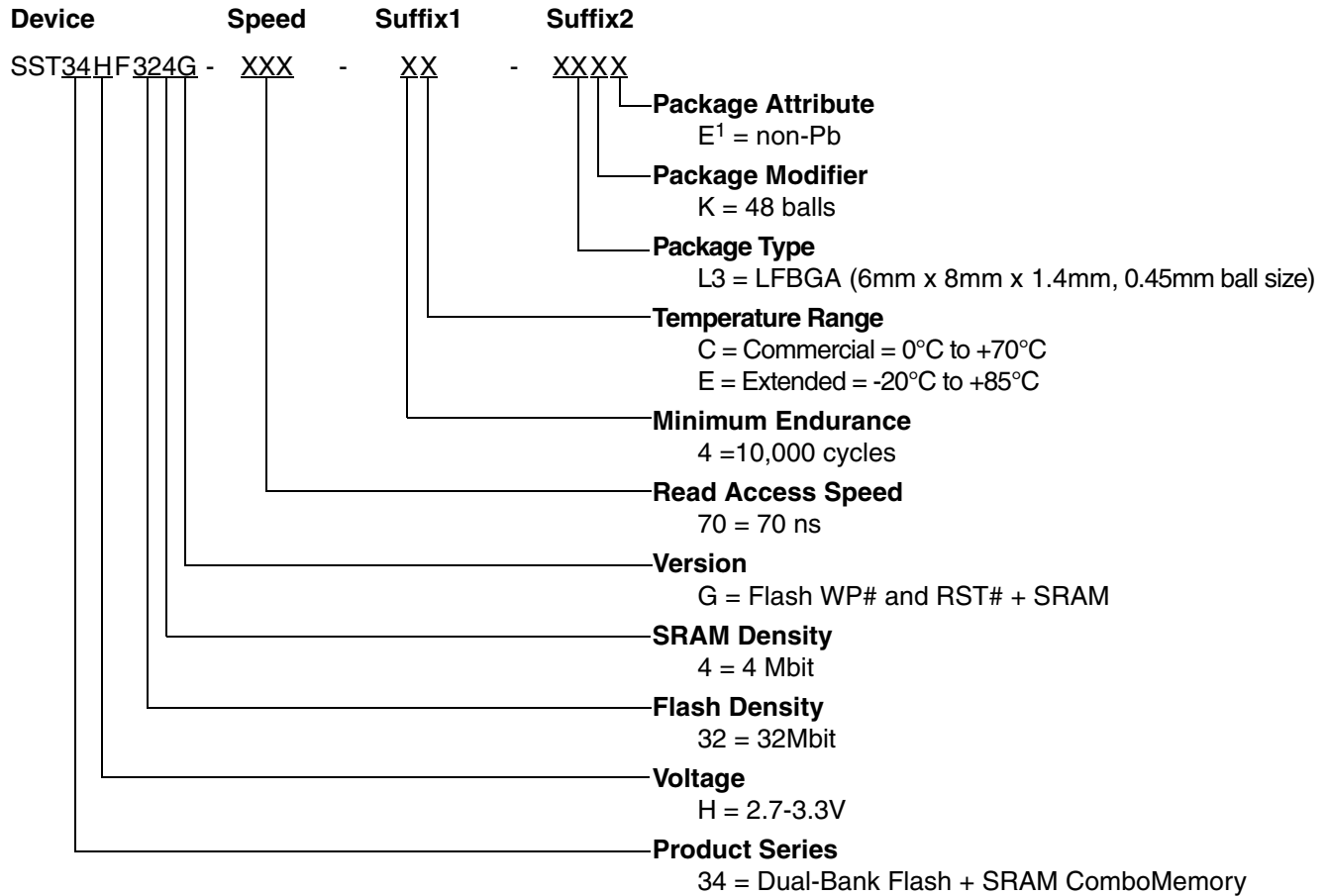
FIGURE 23: Erase Command Sequence



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PRODUCT ORDERING INFORMATION



1. Environmental suffix "E" denotes non-Pb solder.
SST non-Pb solder devices are "RoHS Compliant".

Valid combinations for SST34HF324G

SST34HF324G-70-4C-L3KE

SST34HF324G-70-4E-L3KE

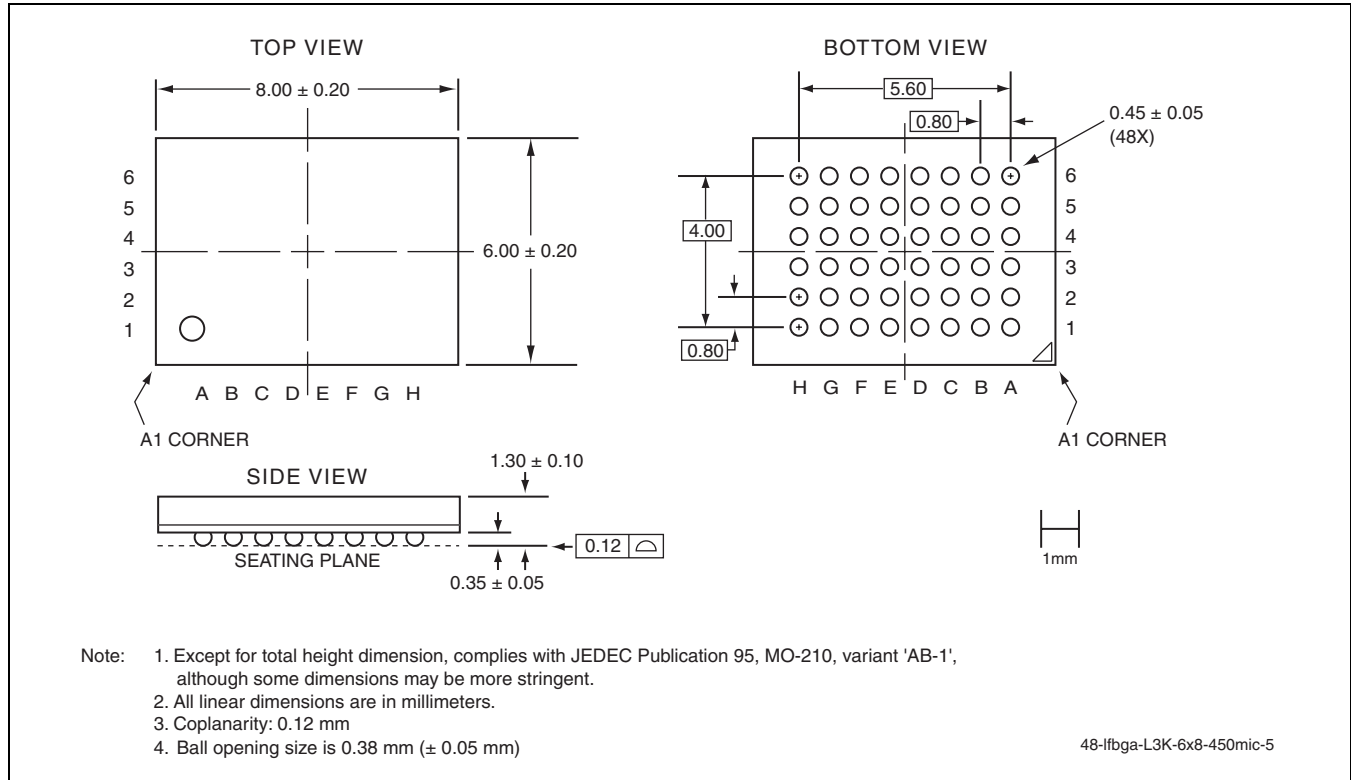
Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.



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PACKAGING DIAGRAMS



48-ball Low-profile, Fine-pitch Ball Grid Array (LFBGA) 6mm x 8mm
SST Package Code: L3K

TABLE 15: Revision History

Number	Description	Date
00	• Initial Release	Jun 2006