

N-CHANNEL INSULATED-GATE BIPOLAR TRANSISTOR

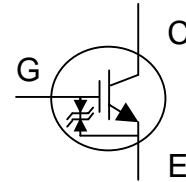
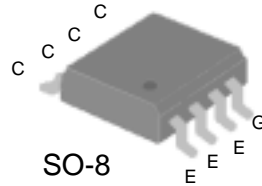
High input impedance

High peak current capability

4.5V gate drive

V_{CE} 450V

I_{CP} 150A



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CE}	Collector-Emitter Voltage	450	V
V_{GE}	Gate-Emitter Voltage	± 6	V
V_{GEP}	Pulsed Gate-Emitter Voltage	± 8	V
I_{CP}	Pulsed Collector Current	150	A
$P_D @ T_C=25^\circ C^1$	Maximum Power Dissipation	2.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Electrical Characteristics @ $T_J=25^\circ C$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
I_{GES}	Gate-Emitter Leakage Current	$V_{GE}=\pm 6V, V_{CE}=0V$	-	-	10	μA
I_{CES}	Collector-Emitter Leakage Current ($T_J=25^\circ C$)	$V_{CE}=450V, V_{GE}=0V$	-	-	10	μA
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$V_{GE}=4.5V, I_{CP}=150A$ (Pulsed)	-	6	8	V
$V_{GE(th)}$	Gate Threshold Voltage	$V_{CE}=V_{GE}, I_C=250\mu A$	0.35	-	1.2	V
Q_g	Total Gate Charge	$I_C=50A$	-	64.5	-	nC
Q_{ge}	Gate-Emitter Charge	$V_{CE}=360V$	-	7	-	nC
Q_{gc}	Gate-Collector Charge	$V_{GE}=5V$	-	30	-	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{CC}=225V$	-	11.5	-	ns
t_r	Rise Time	$I_C=50A$	-	24.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=25\Omega$	-	150	-	ns
t_f	Fall Time	$V_{GE}=5V$	-	3.3	-	μs
C_{ies}	Input Capacitance	$V_{GE}=0V$	-	2227	-	pF
C_{oes}	Output Capacitance	$V_{CE}=25V$	-	200	-	pF
C_{res}	Reverse Transfer Capacitance	$f=1.0MHz$	-	79	-	pF
R_{thJA}^1	Thermal Resistance Junction-Ambient		-	-	50	$^\circ C/W$

Notes:

1. Surface mounted on 1 in² copper pad of FR4 board ; 125 $^\circ C/W$ when mounted on min. copper pad.

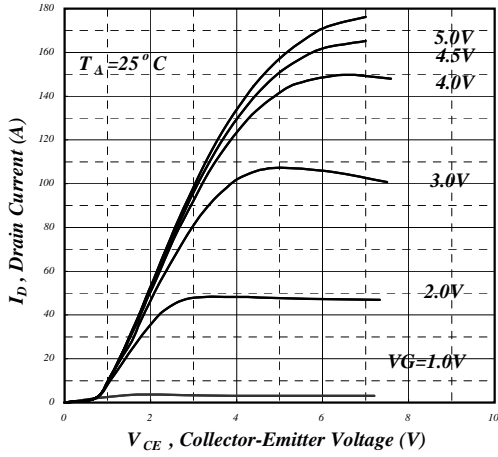


Fig 1. Typical Output Characteristics

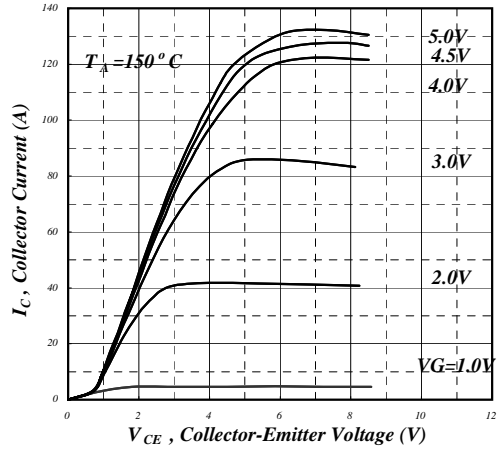


Fig 2. Typical Output Characteristics

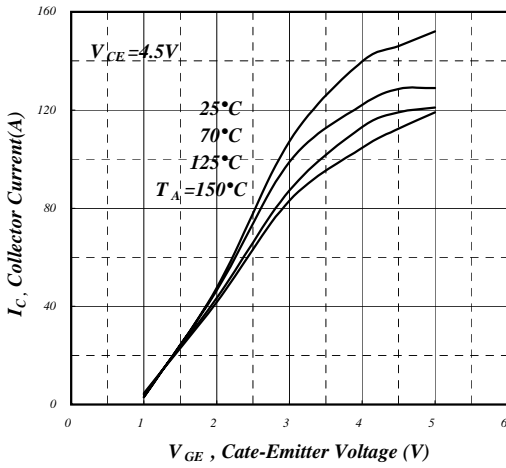


Fig 3. Collector Current vs. Gate-Emitter Voltage

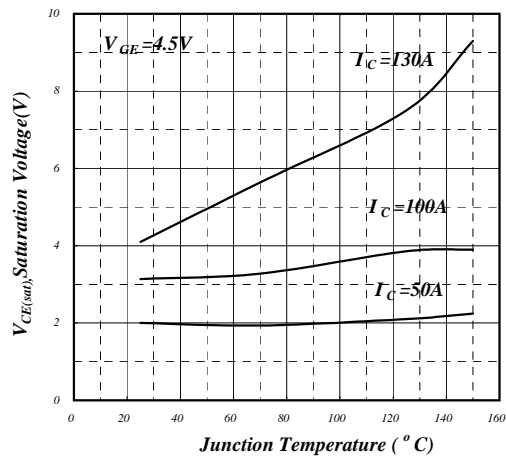


Fig 4. Collector-Emitter Saturation Voltage vs. Junction Temperature

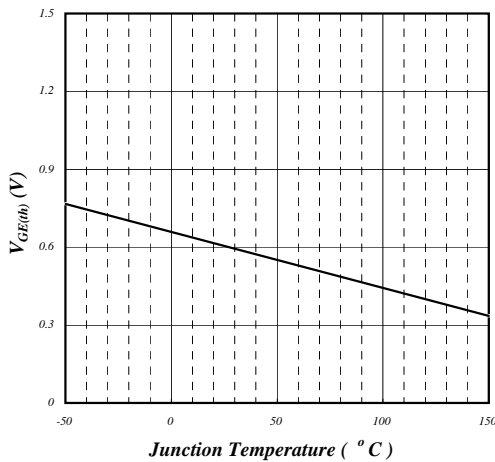


Fig 5. Gate Threshold Voltage vs. Junction Temperature

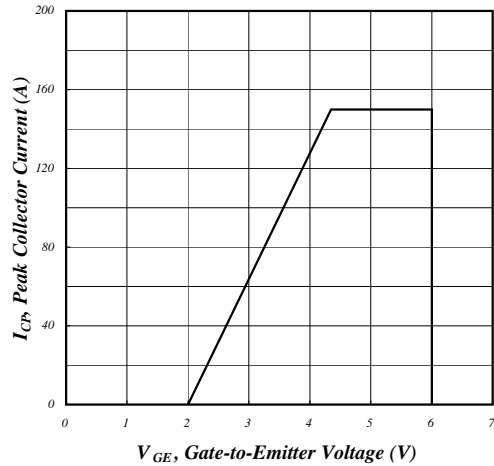


Fig 6. Minimum Gate Drive Area

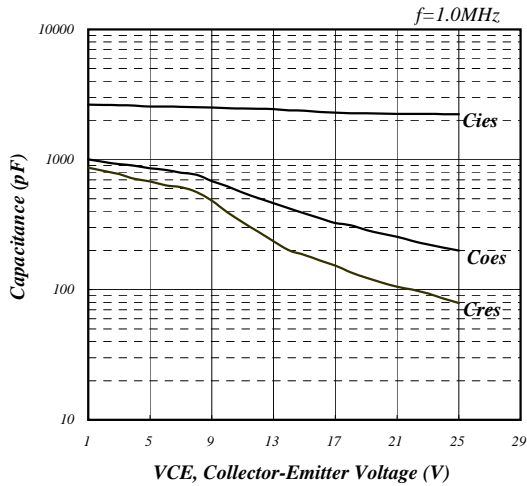


Fig 7. Typical Capacitance Characteristics

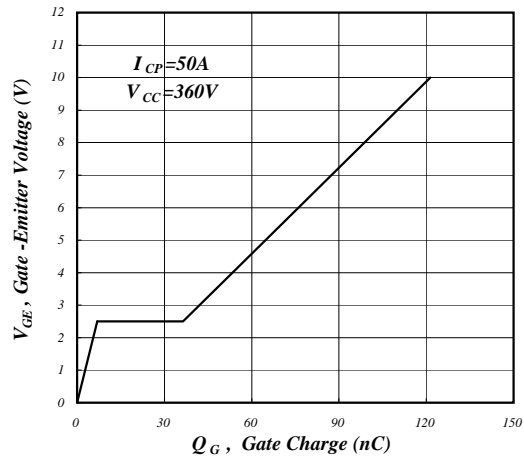


Fig 8. Gate Charge Waveform

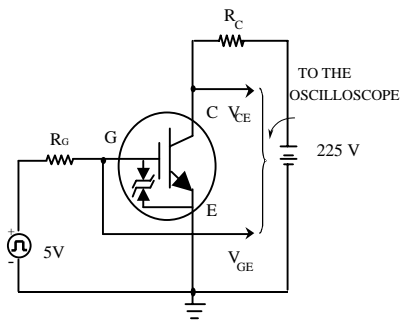


Fig 9. Switching Time Test Circuit

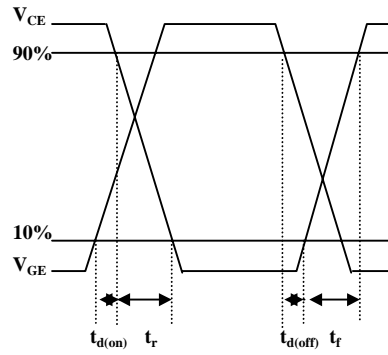


Fig 10. Switching Time Waveform

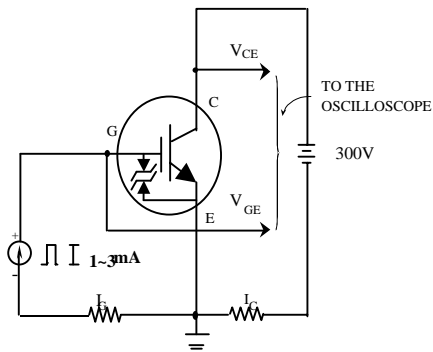


Fig 11. Gate Charge Test Circuit

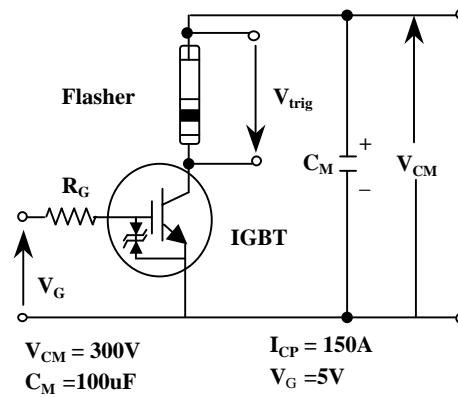


Fig 12. Application Test Circuit

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