

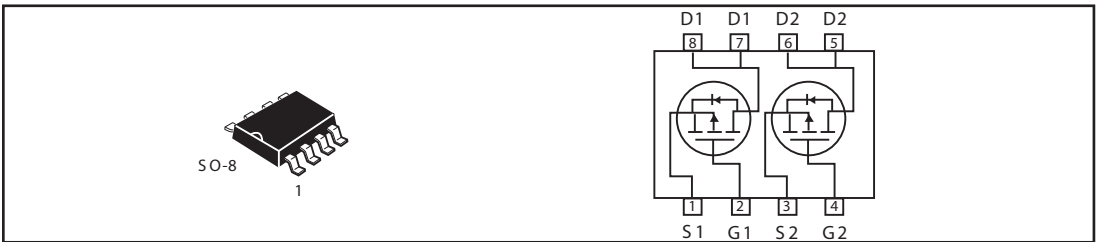


## Dual P-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> ( mΩ ) MAX
-20V	-5.3A	50 @ V <sub>GS</sub> = -4.5V
		75 @ V <sub>GS</sub> = -2.7V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25 °C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	-20	V
Gate-Source Voltage	V <sub>GS</sub>	±12	V
Drain Current-Continuous <sup>a</sup> @ T <sub>J</sub> =125°C -Pulsed <sup>b</sup> (300us Pulse Width)	I <sub>D</sub>	±5.3	A
	I <sub>DM</sub>	±21	A
Drain-Source Diode Forward Current <sup>a</sup>	I <sub>S</sub>	2.5	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	2	W
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to 150	°C

### THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient <sup>a</sup>	R θ <sub>JA</sub>	62.5	°C/W
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ELECTRICAL CHARACTERISTICS ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=-16V, V_{GS}=0V$			-1	$\mu A$
Gate-Body Leakage	$I_{GSS}$	$V_{GS}=\pm 12V, V_{DS}=0V$			$\pm 100$	nA
<b>ON CHARACTERISTICS<sup>b</sup></b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.7			V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=-4.5V, I_D=-2.9A$			50	m-ohm
		$V_{GS}=-2.7V, I_D=-1.5A$			75	m-ohm
On-State Drain Current	$I_{D(on)}$	$V_{DS}=-5V, V_{GS}=-4.5V$	-20			A
Forward Transconductance	$g_{FS}$	$V_{DS}=-15V, I_D=-4.9A$		13		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
Input Capacitance	$C_{ISS}$	$V_{DS}=-10V, V_{GS}=0V$ $f=1.0MHz$		1190		pF
Output Capacitance	$C_{OSS}$			700		pF
Reverse Transfer Capacitance	$C_{RSS}$			250		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
Turn-On Delay Time	$t_{D(on)}$	$V_D=-10V,$ $R_L=10\text{ ohm}$ $I_D=-1A,$ $V_{GEN}=-4.5V,$ $R_{GEN}=6\text{ ohm}$		19	40	ns
Rise Time	$t_r$			18	70	ns
Turn-Off Delay Time	$t_{D(off)}$			49	120	ns
Fall Time	$t_f$			28	130	ns
Total Gate Charge	$Q_g$	$V_{DS}=-10V, I_D=-1A,$ $V_{GS}=-4.5V$		20	25	nC
Gate-Source Charge	$Q_{gs}$			3.7		nC
Gate-Drain Charge	$Q_{gd}$			4.2		nC

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## ELECTRICAL CHARACTERISTICS ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ <sup>c</sup>	Max	Unit
<b>DRAIN-SOURCE DIODE CHARACTERISTICS<sup>b</sup></b>						
Diode Forward Voltage	$V_{SD}$	$V_{GS} = 0V, I_s = -1.7A$		-0.87	-1.2	V

### Notes

- a. Surface Mounted on FR4 Board,  $t \leq 10\text{sec}$ .
- b. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- c. Guaranteed by design, not subject to production testing.

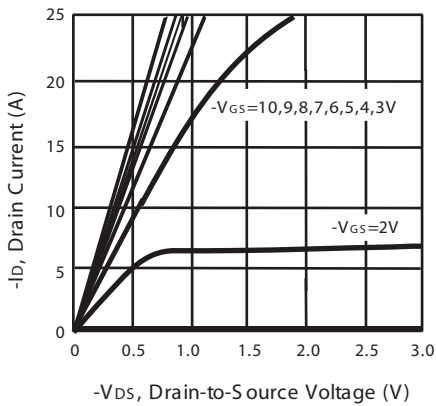


Figure 1. Output Characteristics

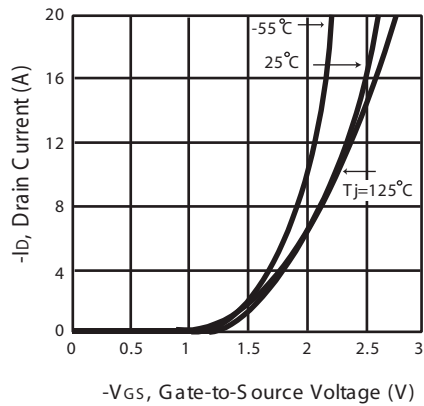


Figure 2. Transfer Characteristics

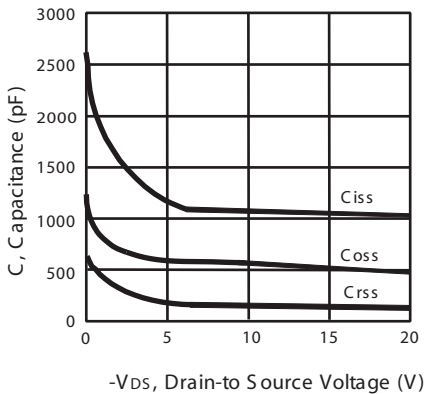


Figure 3. Capacitance

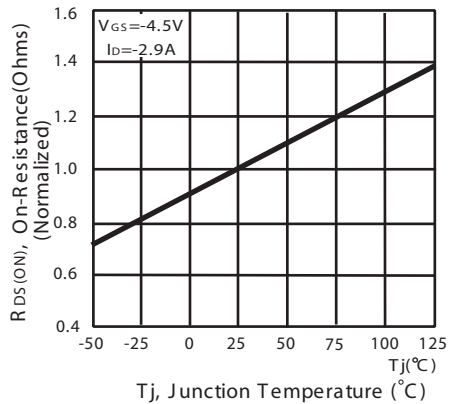
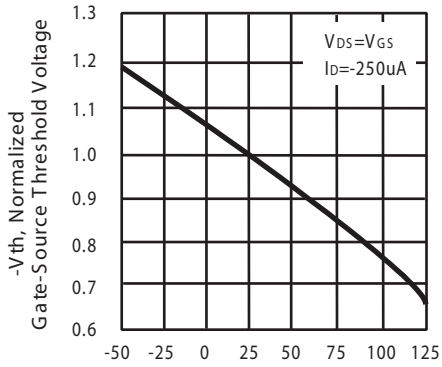


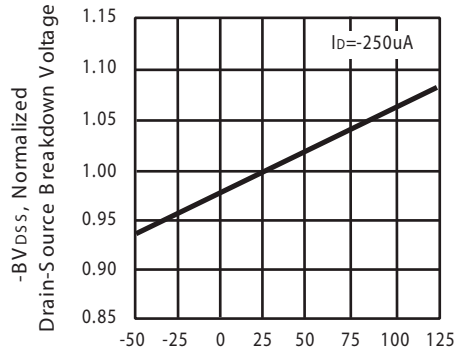
Figure 4. On-Resistance Variation with Temperature

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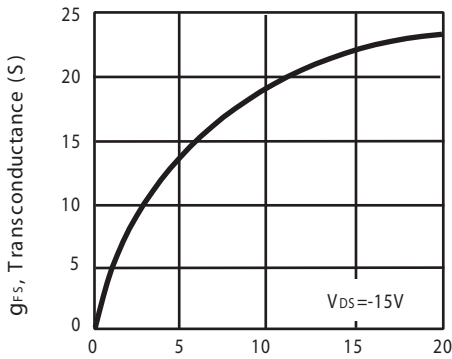
Tj, Junction Temperature (°C)

Figure 5. Gate Threshold Variation with Temperature



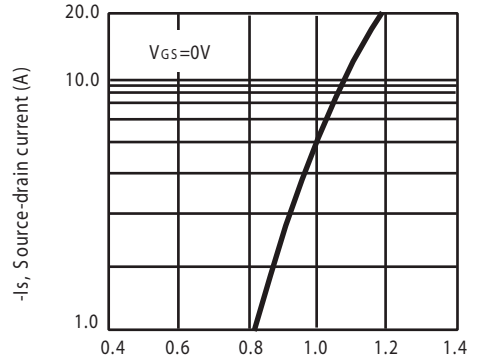
Tj, Junction Temperature (°C)

Figure 6. Breakdown Voltage Variation with Temperature



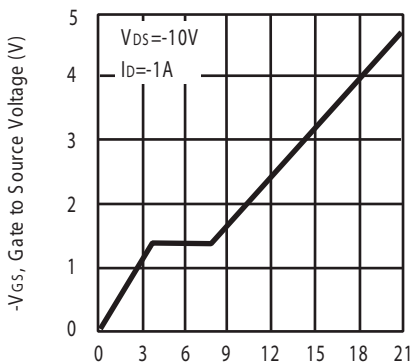
-ID, Drain-Source Current (A)

Figure 7. Transconductance Variation with Drain Current



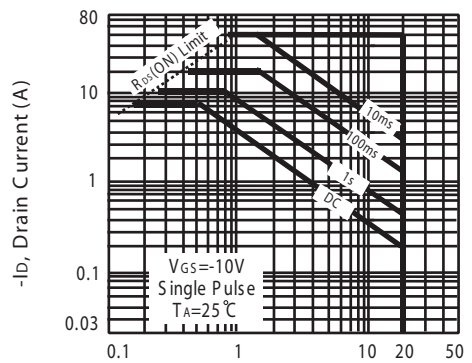
-VSD, Body Diode Forward Voltage (V)

Figure 8. Body Diode Forward Voltage Variation with Source Current



Qg, Total Gate Charge (nC)

Figure 9. Gate Charge



-VDS, Drain-Source Voltage (V)

Figure 10. Maximum Safe Operating Area

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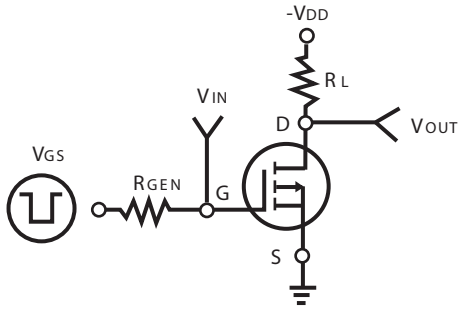


Figure 11. Switching Test Circuit

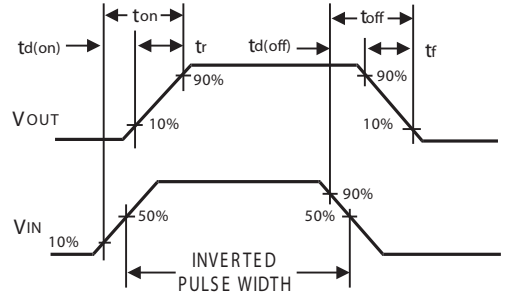


Figure 12. Switching Waveforms

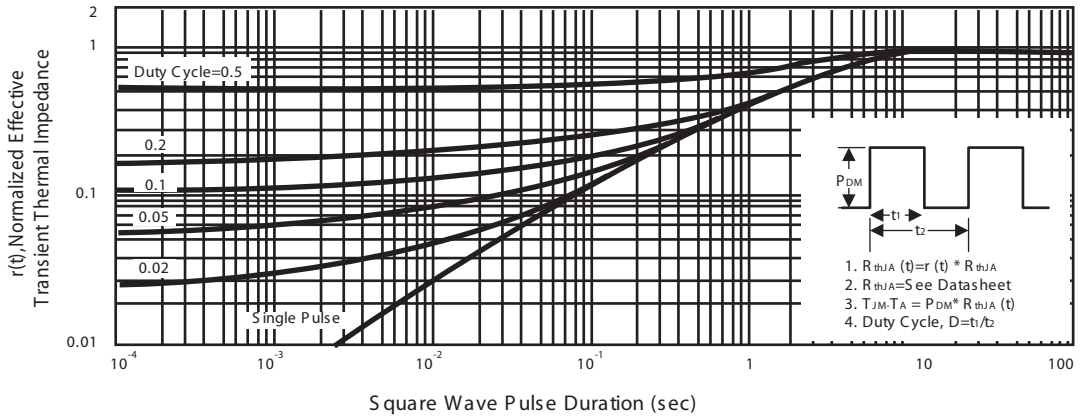


Figure 13. Normalized Thermal Transient Impedance Curve