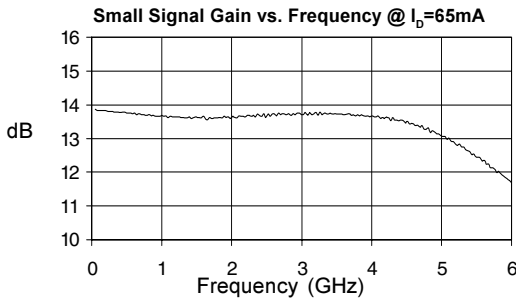


Product Description

Stanford Microdevices' SCA-3 is a high performance Gallium Arsenide Heterojunction Bipolar Transistor MMIC Amplifier. A Darlington configuration is utilized for broadband performance up to 5GHz. The heterojunction increases breakdown voltage and minimizes leakage current between junctions. Cancellation of emitter junction non-linearities results in higher suppression of intermodulation products. Typical IP₃ at 850 MHz with 65mA is 32.8 dBm.

These unconditionally stable amplifiers provide 13.7 dB of gain and 17.3 dBm of 1dB compressed power and require only a single positive voltage supply. Only 2 DC-blocking capacitors, a bias resistor and an optional inductor are needed for operation. This MMIC is an ideal choice for wireless applications such as cellular, PCS, CDPD, wireless data and SONET.



Electrical Specifications

Symbol	Parameters: Test Conditions: Z ₀ = 50 Ohms, I _b = 65mA, T = 25°C	Units	Min.	Typ.	Max.
P _{1dB}	Output Power at 1dB Compression	f = 850 MHz dBm f = 1950 MHz dBm f = 2400 MHz dBm		17.3 17.6 17.4	
IP ₃	Third Order Intercept Point Power out per tone = 0 dBm	f = 850 MHz dBm f = 1950 MHz dBm f = 2400 MHz dBm	29.8	32.8 30.3 29.1	
S ₂₁	Small Signal Gain	f = 850 MHz dB f = 1950 MHz dB f = 2400 MHz dB	12.3	13.7 13.6 13.6	
Bandwidth	(Determined by S ₁₁ , S ₂₂ Values)	MHz		5000	
S ₁₁	Input VSWR	f = DC-5000 MHz	-	1.7:1	
S ₂₂	Output VSWR	f = DC-5000 MHz	-	1.5:1	
S ₁₂	Reverse Isolation	f = 850 MHz dB f = 1950 MHz dB f = 2400 MHz dB		18.3 18.4 18.4	
NF	Noise Figure, Z _s = 50 Ohms	f = 1950 MHz		5.6	
V _D	Device Voltage	V	4.4	4.9	5.4
Rth,j-l	Thermal Resistance (junction - lead)	° C/W		224	

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SCA-3

DC-5 GHz, Cascadable GaAs HBT MMIC Amplifier

NGA-489 Recommended for New Designs



Product Features

- High Output IP₃: 32.8 dBm @ 850 MHz
- Cascadable 50 Ohm Gain Block
- Patented GaAs HBT Technology
- Operates From Single Supply

Applications

- Cellular, PCS, CDPD, Wireless Data, SONET

Absolute Maximum Ratings

Operation of this device above any one of these parameters may cause permanent damage.

Bias Conditions should also satisfy the following expression:

$$I_D V_D (\text{max}) < (T_J - T_{OP})/R_{th, j-l}$$

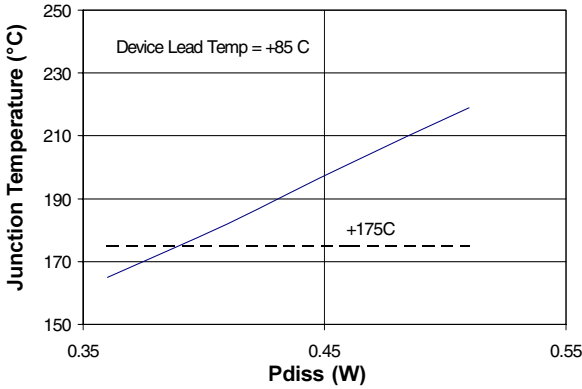
Parameter	Value	Unit
Supply Current	120	mA
Operating Temperature	-40 to +85	C
Maximum Input Power	+16	dBm
Storage Temperature Range	-40 to +150	C
Operating Junction Temperature	+175	C

Parameter	Typical		Test Condition ($I_D = 65 \text{ mA}$, unless otherwise noted)
	25°C	Unit	
500 MHz			
Gain	13.7	dB	$Z_S = 50 \text{ Ohms}$ Tone spacing = 1 MHz, Pout per tone = 0 dBm
Noise Figure	5.4	dB	
Output IP3	32.3	dBm	
Output P1dB	17.1	dBm	
Input Return Loss	12.8	dB	
Isolation	18.2	dB	
850 MHz			
Gain	13.7	dB	$Z_S = 50 \text{ Ohms}$ Tone spacing = 1 MHz, Pout per tone = 0 dBm
Noise Figure	5.5	dB	
Output IP3	32.8	dBm	
Output P1dB	17.3	dBm	
Input Return Loss	12.3	dB	
Isolation	18.3	dB	
1950 MHz			
Gain	13.6	dB	$Z_S = 50 \text{ Ohms}$ Tone spacing = 1 MHz, Pout per tone = 0 dBm
Noise Figure	5.6	dB	
Output IP3	30.3	dBm	
Output P1dB	17.6	dBm	
Input Return Loss	12.9	dB	
Isolation	18.2	dB	
2400 MHz			
Gain	13.6	dB	Tone spacing = 1 MHz, Pout per tone = 0 dBm
Output IP3	29.1	dBm	
Output P1dB	17.4	dBm	
Input Return Loss	15.2	dB	
Isolation	18.4	dB	

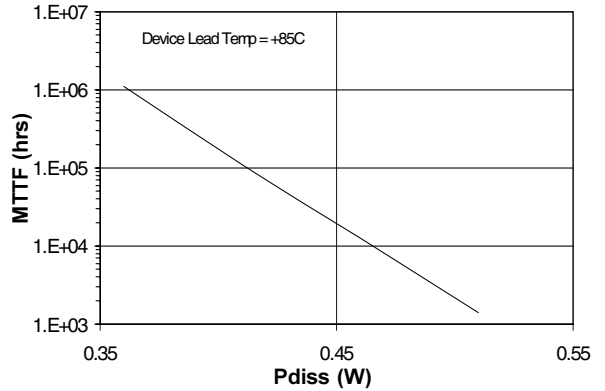
***NOTE:** While the SCA-3 can be operated at different bias currents, 65 mA is the recommended bias for lower junction temperature and longer life. This reflects typical operating conditions which we have found to be an optimal balance between high IP3 and MTTF. In general, MTTF is improved to more than 100,000 hours when biasing at 65 mA and operating up to 85°C ambient temperature.

SCA-3 DC-5GHz Cascadable MMIC Amplifier

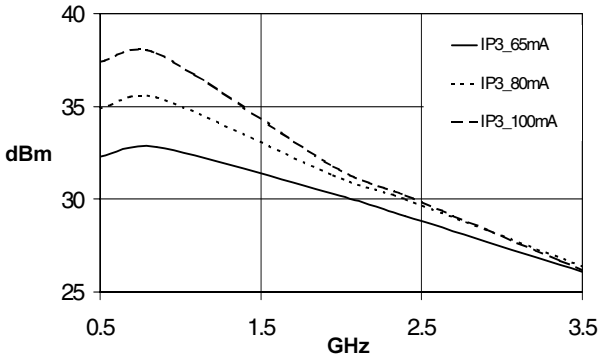
Junction Temp vs. Dissipated Power



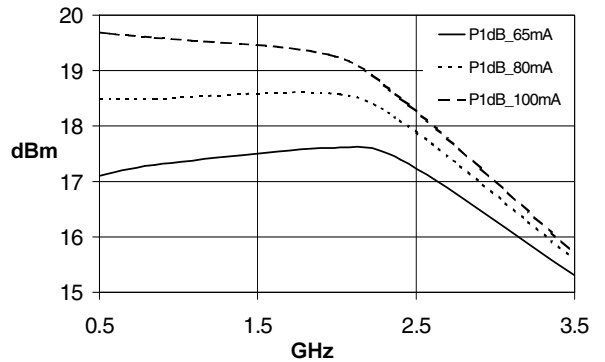
MTTF vs. Dissipated Power



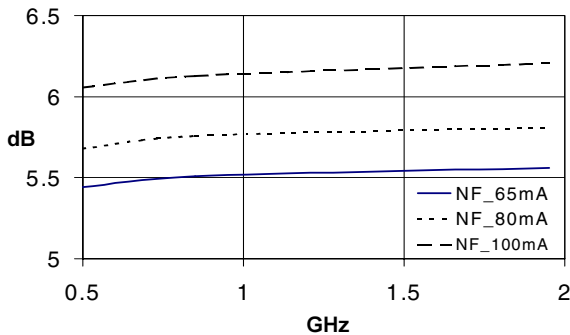
Output IP3 vs. I_D vs. Frequency



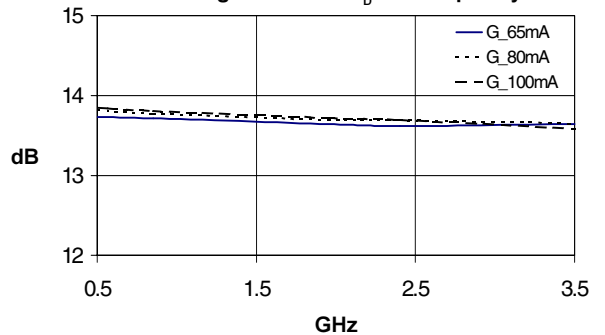
Output P1dB vs. I_D vs. Frequency



NF vs. I_D vs. Frequency



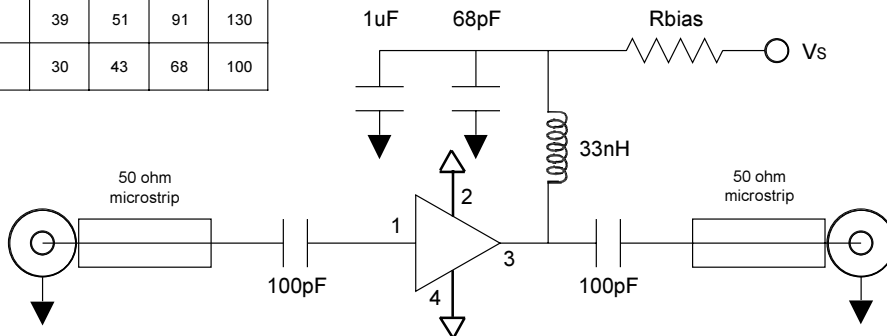
Small Signal Gain vs. I_D vs. Frequency



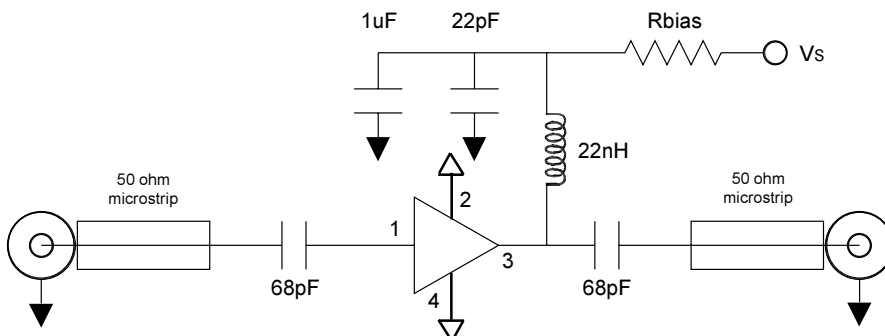
Pin #	Function	Description
1	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.
2	GND	Connection to ground. Use via holes for best performance to reduce lead inductance. Place vias as close to ground leads as possible.
3	RF OUT/Vcc	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed.
4	GND	Same as Pin 2.

Application Schematic for Operation at 850 MHz

Recommended Bias Resistor Values				
Supply Voltage(Vs)	8V	9V	12V	15V
Rbias (Ohms) @ 65 mA	47	62	110	160
Rbias (Ohms) @ 80 mA	39	51	91	130
Rbias (Ohms) @ 100 mA	30	43	68	100

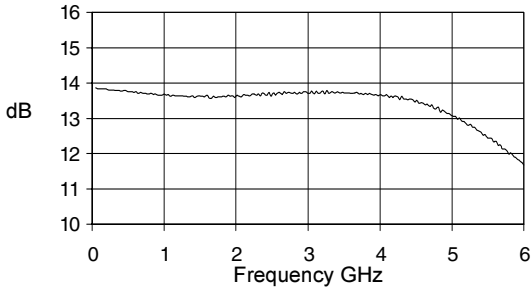


Application Schematic for Operation at 1950 MHz

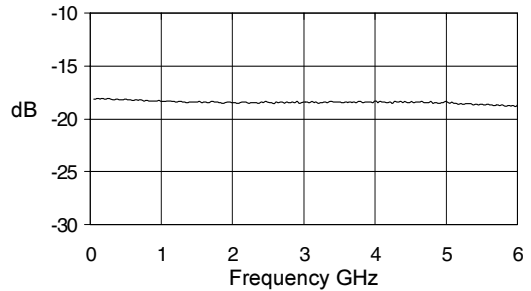


SCA-3 DC-5GHz Cascadable MMIC Amplifier

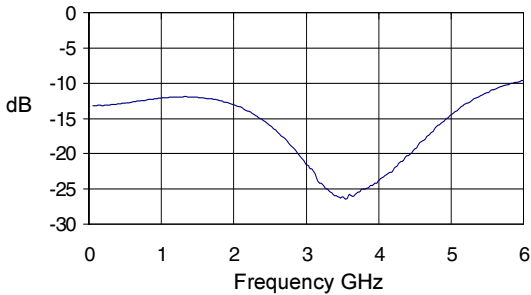
S21, $I_D=65\text{mA}$, $T=25^\circ\text{C}$



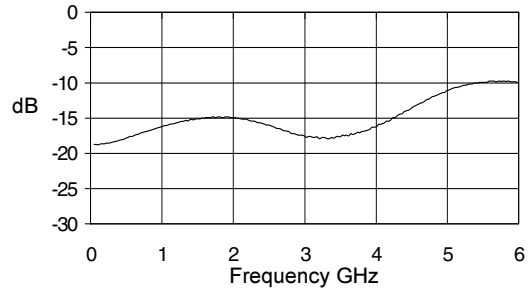
S12, $I_D=65\text{mA}$, $T=25^\circ\text{C}$



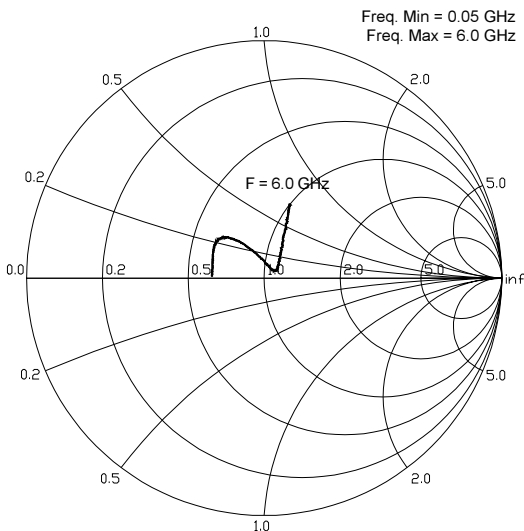
S11, $I_D=65\text{mA}$, $T=25^\circ\text{C}$



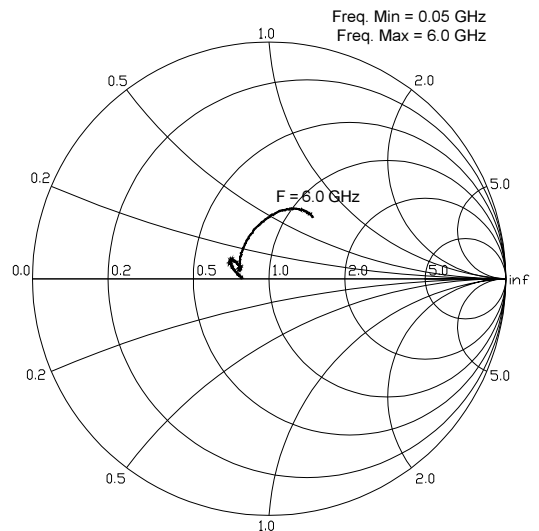
S22, $I_D=65\text{mA}$, $T=25^\circ\text{C}$



S11, $I_D=65\text{mA}$, $T_a=25^\circ\text{C}$



S22, $I_D=65\text{mA}$, $T_a=25^\circ\text{C}$



SCA-3 DC-5GHz Cascadable MMIC Amplifier



Caution: ESD Sensitive

Appropriate precautions in handling, packaging and testing devices must be observed.

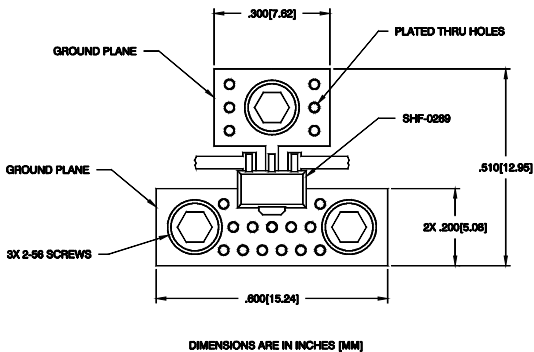
Part Symbolization

The part will be symbolized with a "C3" designator on the top surface of the package.

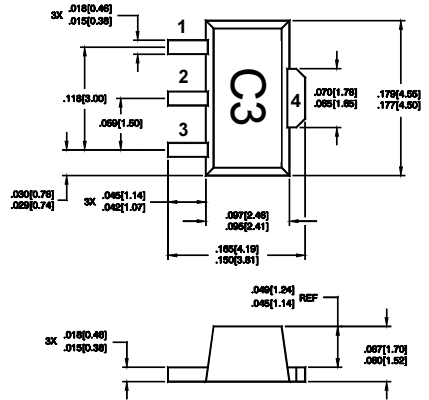
Mounting Instructions

The data shown was taken on a 31 mil thick FR-4 board with 1 ounce of copper on both sides. The board was mounted to a baseplate with 3 screws as shown. The screws bring the top side copper temperature to the same value as the baseplate.

1. Use 1 or 2 ounce copper, if possible.
2. Solder the copper pad on the backside of the device package to the ground plane.
3. Use a large ground pad area with many plated through-holes as shown.
4. If possible, use at least one screw no more than 0.2 inch from the device package to provide a low thermal resistance path to the baseplate of the package.
5. Thermal resistance from ground lead to screws is 2 deg. C/W.



Outline Drawing



Pin assignments shown for reference only, not marked on part.

PCB Pad Layout

