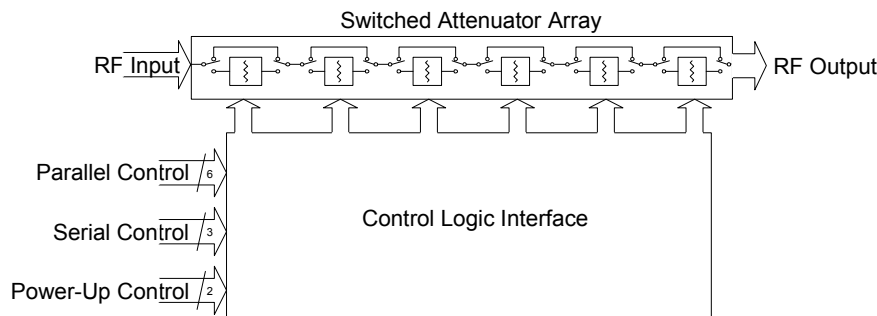


Product Description

The PE94302 is a high linearity, 6-bit UltraCMOS™ RF Digital Step Attenuator (DSA) specifically optimized for rad-hard space applications. This 50-ohm RF DSA covers a 31.5 dB attenuation range in 0.5 dB steps. It provides both parallel and serial CMOS control interface which operate on a single 3-volt supply. It also has a unique control interface that allows the user to select an initial attenuation state at power-up. The PE 94302 maintains high attenuation accuracy over frequency and temperature and exhibits very low insertion loss and power consumption.

The PE94302 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram



**50 Ω RF Digital Step Attenuator
For Rad-Hard Space Applications
6-bit, 31.5 dB, DC – 4.0 GHz**

Features

- Attenuation: 0.5 dB steps to 31.5 dB
- Flexible parallel and serial programming interfaces
- Unique power-up state selection
- Positive CMOS control logic
- High attenuation accuracy and linearity over temperature and frequency
- Very low power consumption
- Single-supply operation
- 50 Ω impedance

**Figure 2. Package Type
28-lead CQFP**

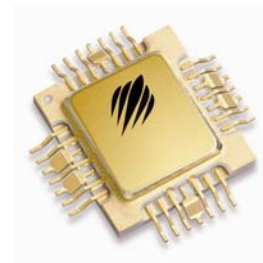


Table 1. Electrical Specifications @ +25°C, V_{DD} = 3.0 V

| Parameter | Test Conditions | Frequency | Typical | Max | Units |
|----------------------------------|--------------------------------------|-------------------|--|-----|-------|
| Operation Frequency ³ | | DC-4000 | | | MHz |
| Insertion Loss | | DC - 2.2 GHz | 1.5 | | dB |
| Attenuation Accuracy | Any Bit or Bit Combination | DC ≤ 1.0 GHz | +/- (0.25 + 3% of attenuation setting) | | dB |
| | 0.5 dB - 23.5 dB Attenuation | 1.0 GHz ≤ 2.2 GHz | +/- (0.25 + 5% of attenuation setting) | | dB |
| | 24 dB - 31.5 dB Attenuation | 1.0 GHz ≤ 2.2 GHz | +/- (11% of attenuation setting) | | dB |
| 1 dB Compression ^{1,2} | | 1 MHz - 2.2 GHz | 34 | | dBm |
| Input IP3 ¹ | Two-tone inputs | 1 MHz - 2.2 GHz | 52 | | dBm |
| Return Loss | | DC - 2.2 GHz | 20 | | dB |
| RF Input Power (50 Ω) | | | | 12 | dBm |
| Switching Speed | 50% control to 0.5 dB of final value | | 1 | | μs |

Notes: 1. Device Linearity will begin to degrade below 1 MHz
 2. Maximum Operating Power = +12 dBm
 3. Specs are guaranteed to 2.2 GHz, Characterized to 4.0 GHz

Figure 3. Pin Configuration (Top View)

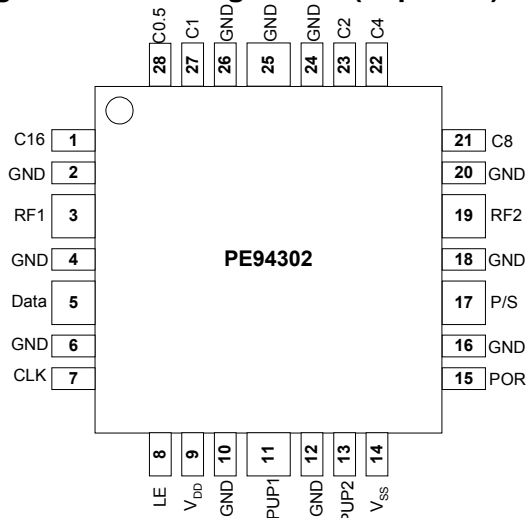


Table 2. Pin Descriptions

| Pin No. | Pin Name | Description |
|---------|-----------------|----------------------------------|
| 1 | C16 | Attenuation control bit, 16dB |
| 2 | GND | Ground connection |
| 3 | RF1 | RF port (Note 1). |
| 4 | GND | Ground connection |
| 5 | Data | Serial interface data input |
| 6 | GND | Ground connection |
| 7 | CLK | Serial interface clock input. |
| 8 | LE | Latch Enable input (Note 2). |
| 9 | V _{DD} | Power supply pin. |
| 10 | GND | Ground connection |
| 11 | PUP1 | Power-up selection bit, MSB. |
| 12 | GND | Ground connection |
| 13 | PUP2 | Power-up selection bit, LSB. |
| 14 | V _{SS} | Negative supply voltage |
| 15 | POR | Power reset |
| 16 | GND | Ground connection |
| 17 | P/S | Parallel/Serial mode select. |
| 18 | GND | Ground connection |
| 19 | RF2 | RF port (Note 1). |
| 20 | GND | Ground connection |
| 21 | C8 | Attenuation control bit, 8 dB. |
| 22 | C4 | Attenuation control bit, 4 dB. |
| 23 | C2 | Attenuation control bit, 2 dB. |
| 24 | GND | Ground connection |
| 25 | GND | Ground connection |
| 26 | GND | Ground connection |
| 27 | C1 | Attenuation control bit, 1 dB. |
| 28 | C0.5 | Attenuation control bit, 0.5 dB. |
| Paddle | GND | Ground connection |

Note 1: Both RF ports must be held at 0 V_{DC} or DC blocked with an external series capacitor.

2: Latch Enable (LE) has an internal 100 kΩ resistor to V_{DD}.

Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|------------------|---------------------------|------|-------------------|-------|
| V _{DD} | Power supply voltage | -0.3 | 4.0 | V |
| V _I | Voltage on any input | -0.3 | V _{DD} + | V |
| T _{ST} | Storage temperature range | -65 | 150 | °C |
| P _{IN} | Input power (50Ω) | | 24 | dBm |
| V _{ESD} | ESD voltage (Human Body) | | 500 | V |

Absolute Maximum Ratings are those values listed in the above table. Exceeding these values may cause permanent device damage. Functional operation should be restricted to the limits in the DC Electrical Specifications table. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 4. DC Electrical Specifications

| Parameter | Min | Typ | Max | Units |
|--------------------------------------|---------------------|-----|---------------------|-------|
| V _{DD} Power Supply Voltage | 2.7 | 3.0 | 3.3 | V |
| I _{DD} Power Supply Current | | | 100 | μA |
| T _{OP} Operating | -40 | | 85 | °C |
| Digital Input High | 0.7xV _{DD} | | | V |
| Digital Input Low | | | 0.3xV _{DD} | V |
| Digital Input Leakage | | | 1 | μA |

Exposed Solder Pad Connection

The exposed solder pad on the bottom of the package must be grounded for proper device operation.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS™ device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rate specified in Table 3.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Switching Frequency

The PE94302 has a maximum 25 kHz switching rate.

Typical Performance Data (25°C, $V_{DD}=3.0\text{ V}$)

Figure 4. Insertion Loss Vs. Frequency

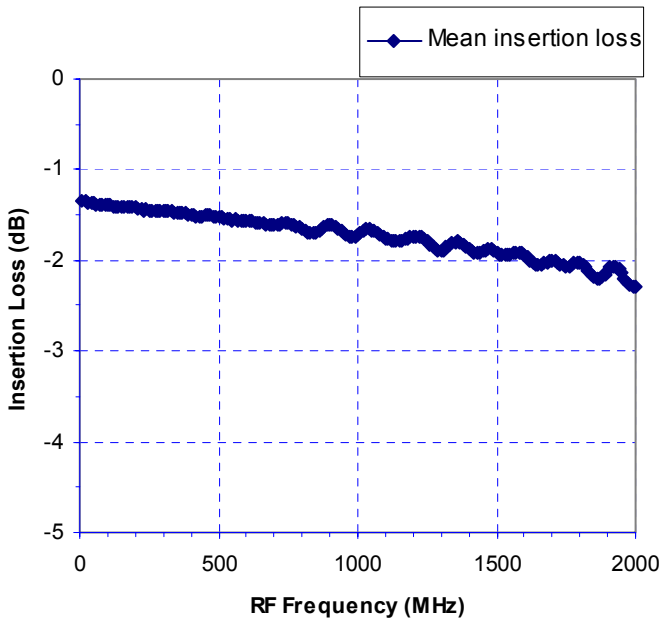


Figure 5. Attenuation Error Vs. Attenuation Setting

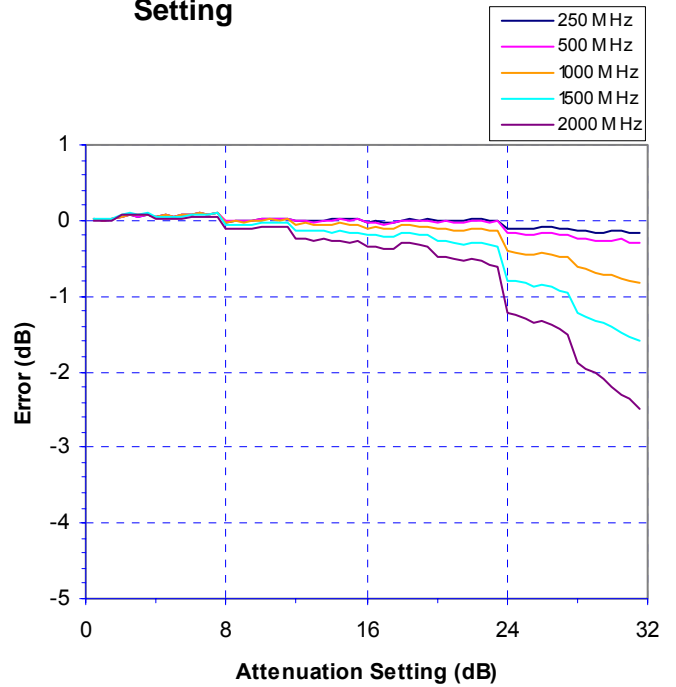
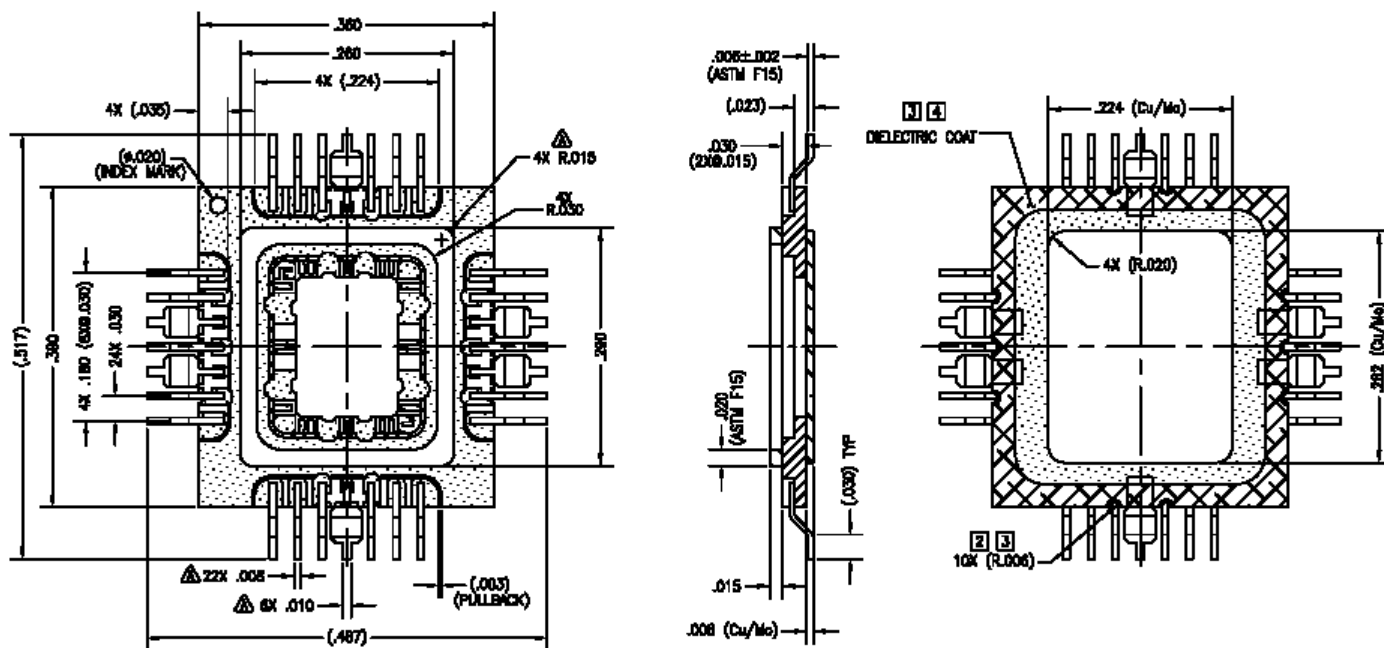


Figure 6. Package Drawing

28-lead CQFP



NOTES:

1. METALLIZATION/ PLATING: REFRACTORY METAL = Ni (75-350u") = Au (50u"MIN)
2. METALLIZED CASTELLATIONS.
3. DIELECTIC RUN INTO CASTELLATIONS SHALL BE ACCEPTABLE.
4. GOLD SPECKLES ON DIELECTRIC COAT SHALL BE ACCEPTABLE.
5. VISUAL ANOMALIES IN CASTELLATION METALLIZATION ACCEPTABLE.
6. TEXT AND ITS LOCATIONS ON LEAD FRAME ARE VENDOR'S OPTION.
7. SLIGHT PATTERN MISMATCH WITH DRAWING DUE TO DIELECTRIC COAT MISALIGNMENT SHALL BE ACCEPTABLE.
8. SEAL RING & HEAT SINK ARE CONNECTED TO GND.
9. LEAD INTEGRITY (ADHESION/ ALIGNMENT/ COPRANARITY), CASTELLATION QUALITY ARE BEST EFFORT BASIS.

Table 10. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|------------|--------------|--|------------------|-----------------|
| 94302-01 | 94302 | PE94302-28CQFP-50B Engineering Samples | 28-lead CQFP | 50 Count Trays |
| 94302-11 | 94302 | PE94302-28CQFP-50B Production Units | 28-lead CQFP | 50 Count Trays |
| 94302-00 | PE94302-EK | PE94302 Evaluation Kit | Evaluation Board | 1 / Box |

Sales Offices

The Americas

Peregrine Semiconductor Corp.

9450 Carroll Park Drive
San Diego, CA 92121
Tel 858-731-9400
Fax 858-731-9499

Europe

Peregrine Semiconductor Europe

Commercial Products:

Bâtiment Maine
13-15 rue des Quatre Vents
F- 92380 Garches, France
Tel: +33-1-47-41-91-73
Fax : +33-1-47-41-91-73

Space and Defense Products:

180 Rue Jean de Guiramand
13852 Aix-En-Provence cedex 3, France
Tel: +33(0) 4 4239 3361
Fax: +33(0) 4 4239 7227

North Asia Pacific

Peregrine Semiconductor K.K.

5A-5, 5F Imperial Tower
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: +81-3-3502-5211
Fax: +81-3-3502-5213

South Asia Pacific

Peregrine Semiconductor

28G, Times Square,
No. 500 Zhangyang Road,
Shanghai, 200122, P.R. China
Tel: +86-21-5836-8276
Fax: +86-21-5836-7652

For a list of representatives in your area, please refer to our Web site at: www.psemi.com

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The data sheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a DCN (Document Change Notice).

The information in this data sheet is believed to be reliable. However, Peregrine assumes no liability for the use of this information. Use shall be entirely at the user's own risk.

No patent rights or licenses to any circuits described in this data sheet are implied or granted to any third party.

Peregrine's products are not designed or intended for use in devices or systems intended for surgical implant, or in other applications intended to support or sustain life, or in any application in which the failure of the Peregrine product could create a situation in which personal injury or death might occur. Peregrine assumes no liability for damages, including consequential or incidental damages, arising out of the use of its products in such applications.

The Peregrine name, logo, and UTSi are registered trademarks and UltraCMOS is a trademark of Peregrine Semiconductor Corp.