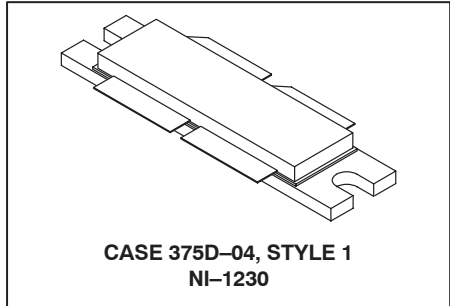


The RF Sub-Micron MOSFET Line
RF Power Field Effect Transistor
N-Channel Enhancement-Mode Lateral MOSFET



**2170 MHz, 52 W AVG.,
 2 x W-CDMA, 28 V
 LATERAL N-CHANNEL
 RF POWER MOSFET**



Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

- Typical 2-carrier W-CDMA Performance for $V_{DD} = 28$ Volts, $I_{DQ} = 2 \times 1100$ mA, $f_1 = 2135$ MHz, $f_2 = 2145$ MHz, Channel Bandwidth = 3.84 MHz, Adjacent Channels Measured over 3.84 MHz BW @ $f_1 - 5$ MHz and $f_2 + 5$ MHz. Distortion Products Measured over a 3.84 MHz BW @ $f_1 - 10$ MHz and $f_2 + 10$ MHz, Each Carrier Peak/Avg. = 8.5 dB @ 0.01% Probability on CCDF.
 - Output Power — 52 Watts Avg.
 - Power Gain — 13 dB
 - Efficiency — 24%
 - IM3 — -36 dBc
 - ACPR — -39 dBc
- Internally Matched, Controlled Q, for Ease of Use
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 5:1 VSWR, @ 28 Vdc, $f = 2140$ MHz, 180 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R6 Suffix = 150 Units per 56 mm, 13 inch Reel.

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-----------|-------------|------------------------------|
| Drain-Source Voltage | V_{DSS} | 65 | Vdc |
| Gate-Source Voltage | V_{GS} | -0.5, +15 | Vdc |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 500 2.86 | Watts W/ $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| Operating Junction Temperature | T_J | 200 | $^\circ\text{C}$ |
| CW Operation | CW | 180 | Watts |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------------|--------------|---------------------------|
| Thermal Resistance, Junction to Case Case Temperature 55°C , 180 W CW Case Temperature 45°C , 52 W CW | $R_{\theta JC}$ | 0.35 0.40 | $^\circ\text{C}/\text{W}$ |

NOTE – **CAUTION** – MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ESD PROTECTION CHARACTERISTICS

| Test Conditions | Class |
|---------------------|--------------|
| Human Body Model | 2 (Minimum) |
| Machine Model | M3 (Minimum) |
| Charge Device Model | C6 (Minimum) |

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS (1)

| | | | | | |
|--|------------------|---|---|----|------------------|
| Zero Gate Voltage Drain Leakage Current (V _{DS} = 65 Vdc, V _{GS} = 0 Vdc) | I _{DSS} | — | — | 10 | μA _{dc} |
| Zero Gate Voltage Drain Leakage Current (V _{DS} = 28 Vdc, V _{GS} = 0 Vdc) | I _{DSS} | — | — | 1 | μA _{dc} |
| Gate–Source Leakage Current (V _{GS} = 5 Vdc, V _{DS} = 0 Vdc) | I _{GSS} | — | — | 1 | μA _{dc} |

ON CHARACTERISTICS (1)

| | | | | | |
|---|---------------------|---|------|-----|-----|
| Gate Threshold Voltage (V _{DS} = 10 Vdc, I _D = 300 μA _{dc}) | V _{GS(th)} | 2 | 2.8 | 4 | Vdc |
| Gate Quiescent Voltage (V _{DS} = 28 Vdc, I _D = 1100 mA _{dc}) | V _{GS(Q)} | 3 | 3.8 | 5 | Vdc |
| Drain–Source On–Voltage (V _{GS} = 10 Vdc, I _D = 3 A _{dc}) | V _{DS(on)} | — | 0.26 | 0.3 | Vdc |
| Forward Transconductance (V _{DS} = 10 Vdc, I _D = 3 A _{dc}) | g _{fs} | — | 7.5 | — | S |

DYNAMIC CHARACTERISTICS (1)

| | | | | | |
|--|-----------------------------|---|------|---|----|
| Reverse Transfer Capacitance (V _{DS} = 28 Vdc, V _{GS} = 0, f = 1 MHz) | C _{r_{ss}} | — | 2.75 | — | pF |
|--|-----------------------------|---|------|---|----|

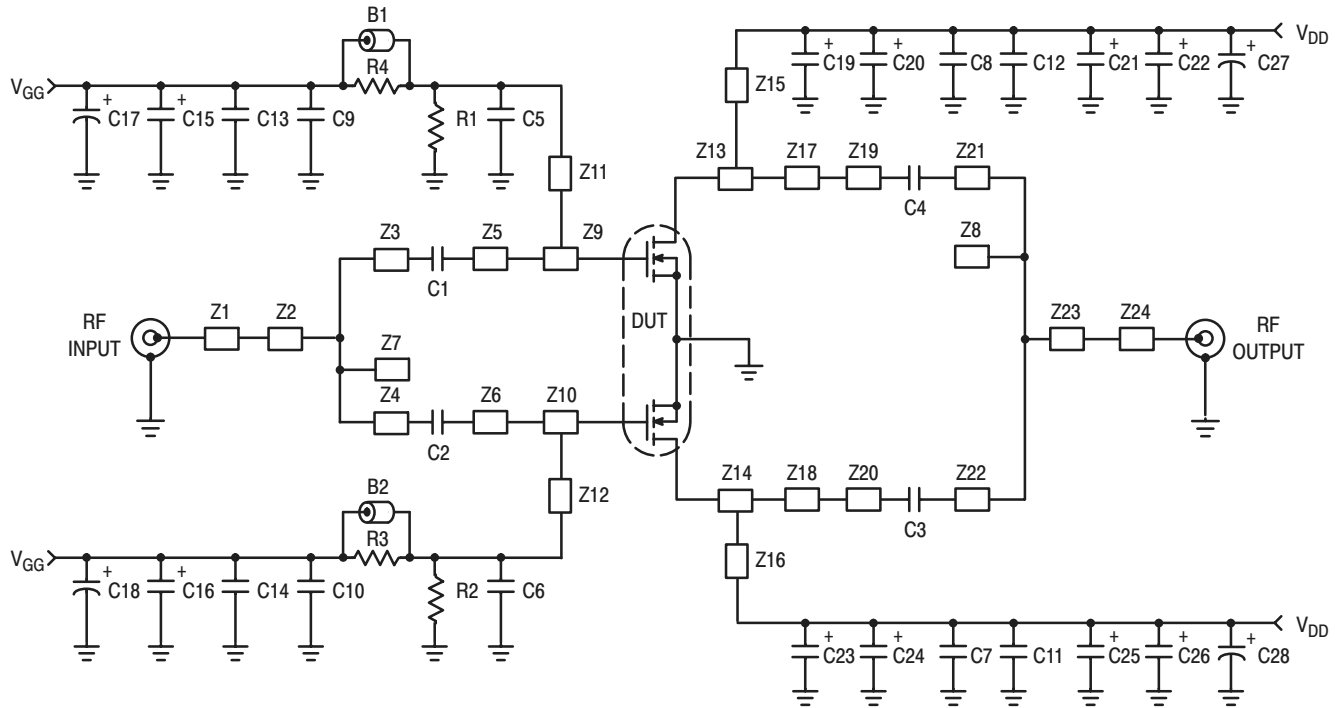
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system) (2)

2–Carrier W–CDMA, 3.84 MHz Channel Bandwidth Carriers. Each carrier has Peak/Avg. ratio = 8.5 dB @ 0.01% Probability on CCDF.

| | | | | | |
|--|-----------------|------|-----|-----|-----|
| Common–Source Amplifier Power Gain (V _{DD} = 28 Vdc, P _{out} = 52 W Avg., I _{DQ} = 2 x 1100 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz) | G _{ps} | 12 | 13 | — | dB |
| Drain Efficiency (V _{DD} = 28 Vdc, P _{out} = 52 W Avg., I _{DQ} = 2 x 1100 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz) | η | 22.5 | 24 | — | % |
| Third Order Intermodulation Distortion (V _{DD} = 28 Vdc, P _{out} = 52 W Avg., I _{DQ} = 2 x 1100 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; IM3 measured over 3.84 MHz BW @ f ₁ –10 MHz and f ₂ +10 MHz) | IM3 | — | –36 | –34 | dBc |
| Adjacent Channel Power Ratio (V _{DD} = 28 Vdc, P _{out} = 52 W Avg., I _{DQ} = 2 x 1100 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz; ACPR measured over 3.84 MHz BW @ f ₁ –5 MHz and f ₂ +5 MHz.) | ACPR | — | –39 | –37 | dBc |
| Input Return Loss (V _{DD} = 28 Vdc, P _{out} = 52 W Avg., I _{DQ} = 2 x 1100 mA, f ₁ = 2112.5 MHz, f ₂ = 2122.5 MHz and f ₁ = 2157.5 MHz, f ₂ = 2167.5 MHz) | IRL | — | –12 | –9 | dB |

(1) Each side of device measured separately. Part is internally matched both on input and output.

(2) Measurements made with device in push–pull configuration.



- | | | | |
|---------|----------------------------|----------|--|
| Z1 | 0.898" x 0.080" Microstrip | Z11, Z12 | 1.270" x 0.058" Microstrip |
| Z2, Z23 | 0.775" x 0.136" Microstrip | Z13, Z14 | 0.250" x 0.500" Microstrip |
| Z3, Z22 | 0.060" x 0.080" Microstrip | Z15, Z16 | 0.850" x 0.150" Microstrip |
| Z4, Z21 | 1.867" x 0.080" Microstrip | Z17, Z18 | 0.535" x 0.390" Microstrip |
| Z5, Z6 | 0.443" x 0.080" Microstrip | Z19, Z20 | 0.218" x 0.080" Microstrip |
| Z7, Z8 | 0.100" x 0.080" Microstrip | Z24 | 0.825" x 0.080" Microstrip |
| Z9, Z10 | 0.490" x 0.540" Microstrip | PCB | Arlon GX-0300-55-22, 0.030", $\epsilon_r = 2.55$ |

Figure 1. MRF5P21240R6 Test Circuit Schematic

Table 1. MRF5P21240R6 Test Circuit Component Designations and Values

| Part | Description | Value, P/N or DWG | Manufacturer |
|--|---------------------------------------|--------------------|--------------|
| B1, B2 | Short Ferrite Beads | 2743019447 | Fair Rite |
| C1, C2, C3, C4 | 18 pF Chip Capacitors | 100B180JCA500X | ATC |
| C5, C6, C7, C8 | 6.8 pF Chip Capacitors | 100B6R8JCA500X | ATC |
| C9, C10, C11, C12 | 0.1 μ F Chip Capacitors | CDR33BX104AKWS | Kemet |
| C13, C14 | 1000 pF Chip Capacitors | 100B102JCA500X | ATC |
| C15, C16 | 4.7 μ F Tantalum Capacitors | T491C475M050 | Kemet |
| C17, C18 | 10 μ F Electrolytic Capacitors | EEV-HB1H100P | Panasonic |
| C19, C20, C21, C22 C23, C24, C25, C26 | 22 μ F Tantalum Capacitors | T491X226K035AS4394 | Kemet |
| C27, C28 | 100 μ F Electrolytic Capacitors | 517D107M050BB6A | Sprague |
| R1, R2 | 1.0 k Ω , 1/8 W Chip Resistors | | |
| R3, R4 | 10 Ω , 1/8 W Chip Resistors | | |

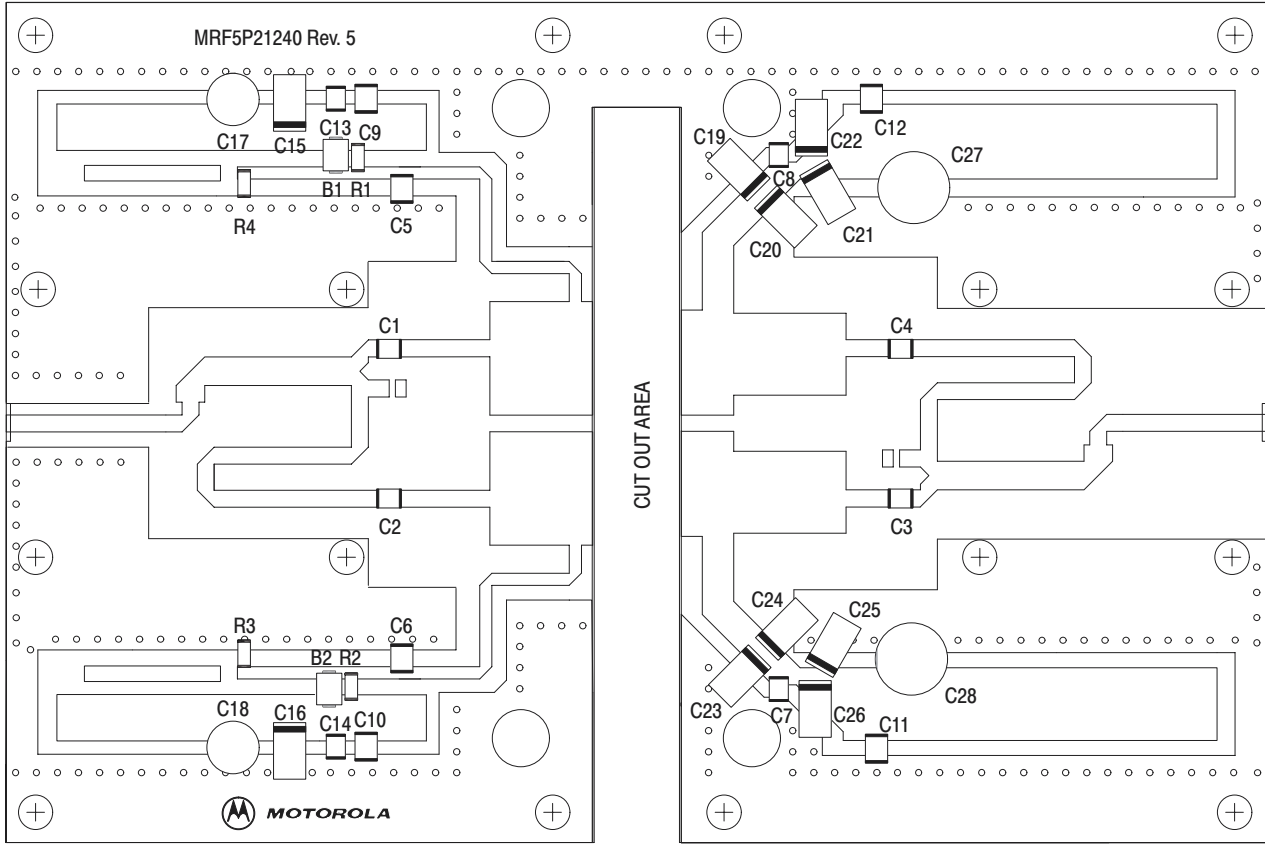


Figure 2. MRF5P21240R6 Test Circuit Component Layout

Freescale Semiconductor, Inc.

TYPICAL CHARACTERISTICS

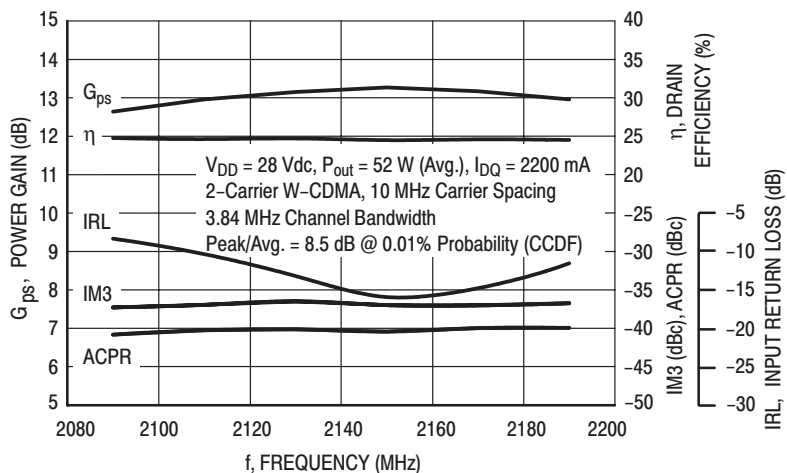


Figure 3. 2-Carrier W-CDMA Broadband Performance

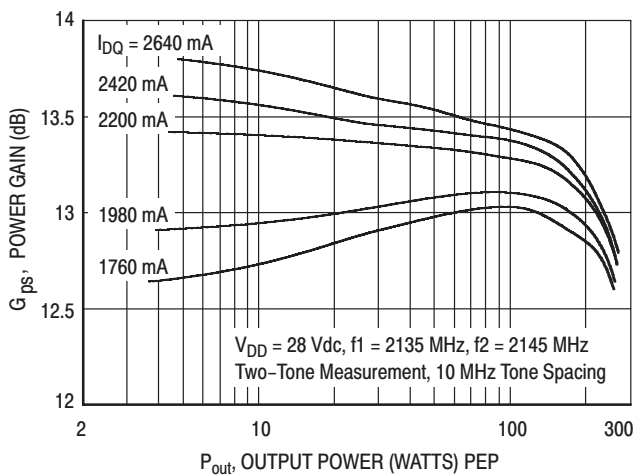


Figure 4. Two-Tone Power Gain versus Output Power

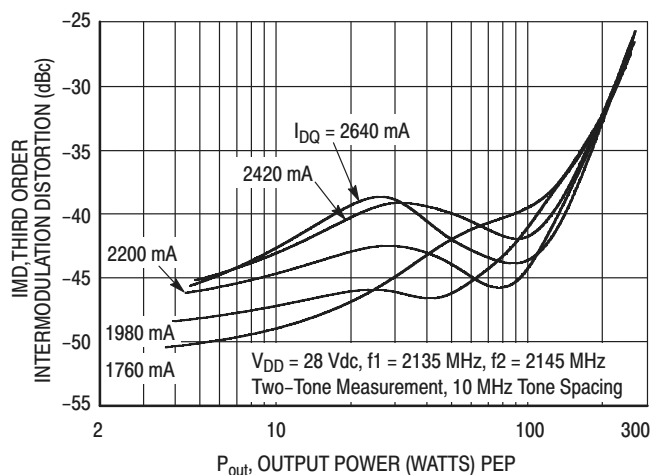


Figure 5. Third Order Intermodulation Distortion versus Output Power

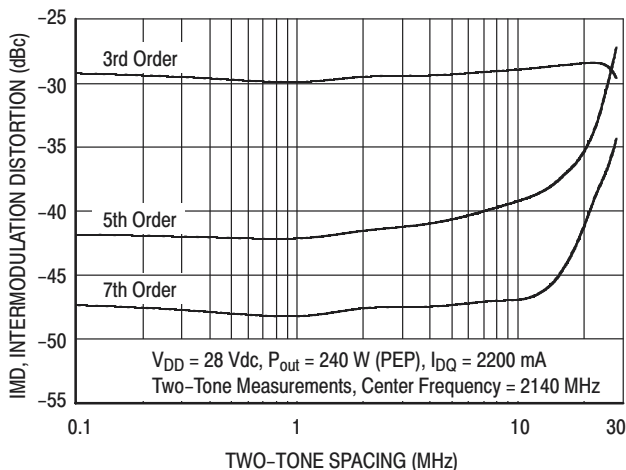


Figure 6. Intermodulation Distortion Products versus Tone Spacing

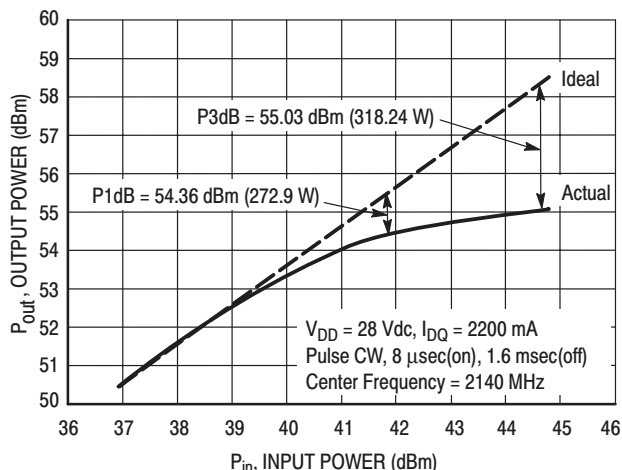


Figure 7. Pulse CW Output Power versus Input Power

TYPICAL CHARACTERISTICS

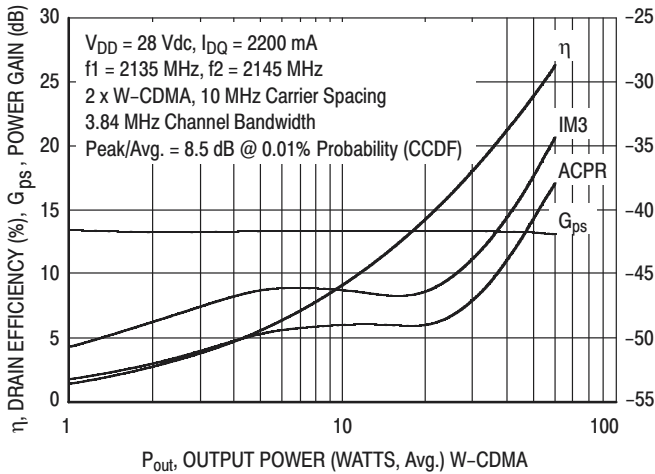


Figure 8. 2-Carrier W-CDMA ACPR, IM3, Power Gain and Drain Efficiency versus Output Power

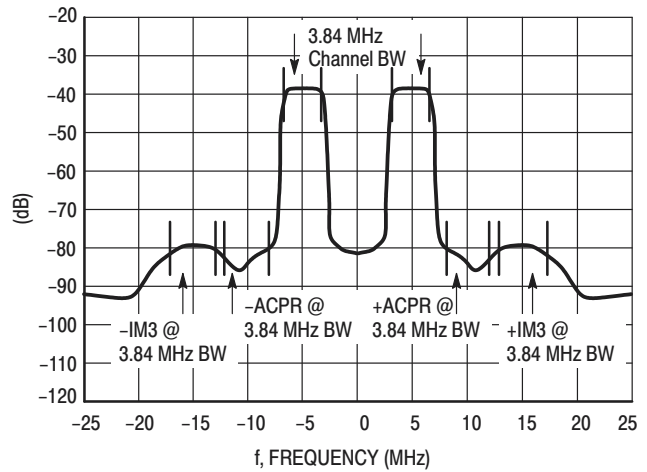


Figure 9. 2-Carrier W-CDMA Spectrum

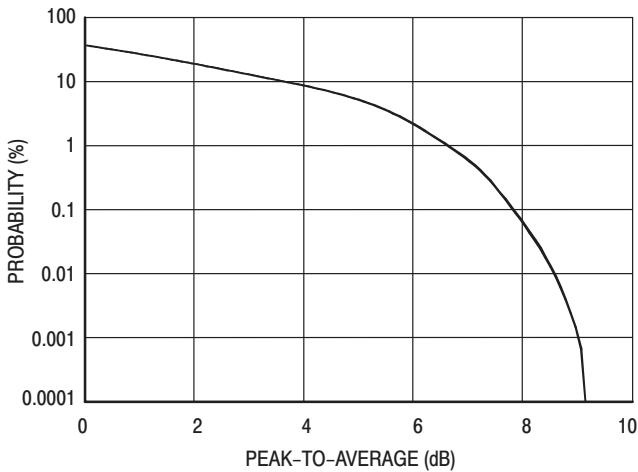
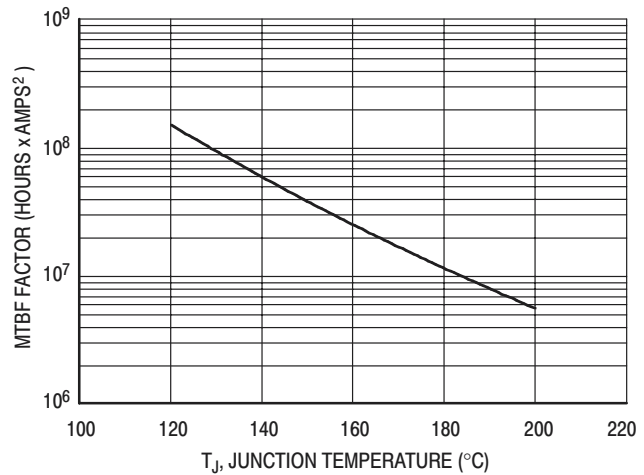
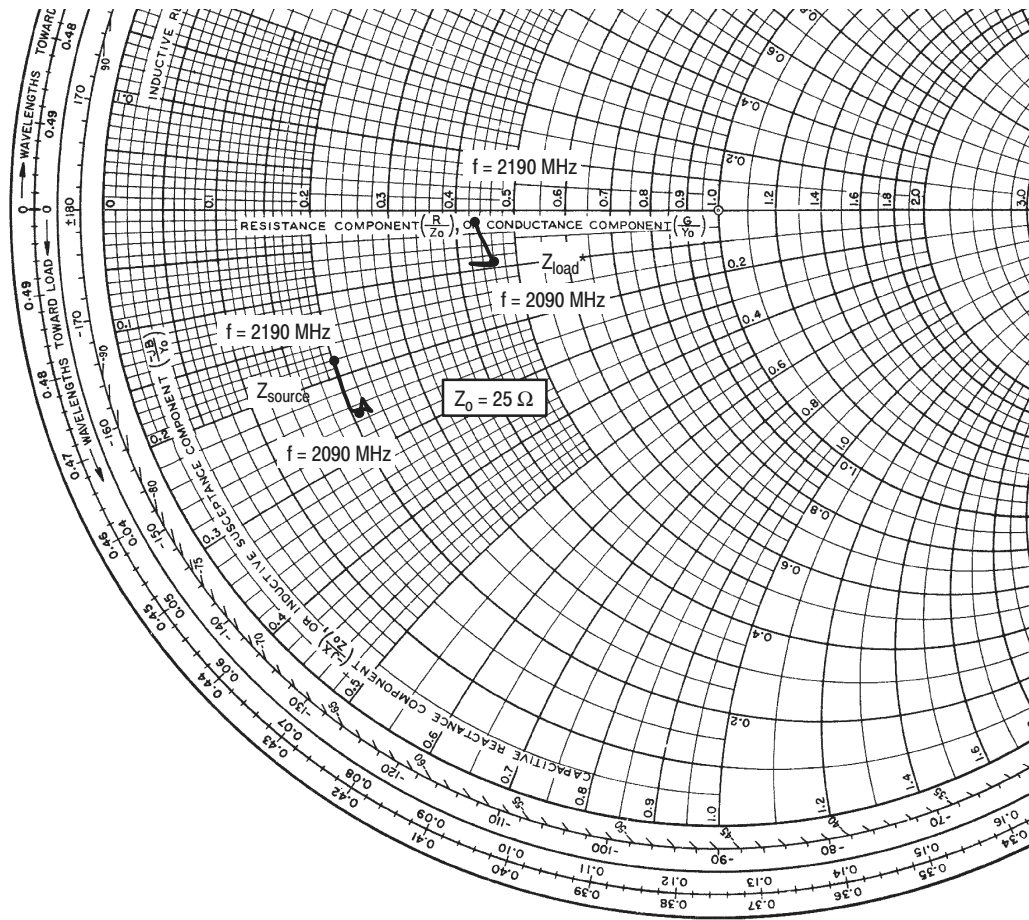


Figure 10. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 67% Clipping, Single Carrier Test Signal



This above graph displays calculated MTBF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTBF factor by I_D^2 for MTBF in a particular application.

Figure 11. MTBF Factor versus Junction Temperature



$V_{DD} = 28\text{ V}$, $I_{DQ} = 2 \times 1100\text{ mA}$, $P_{out} = 52\text{ W Avg.}$

| f MHz | Z_{source} Ω | Z_{load} Ω |
|----------|--------------------------|------------------------|
| 2090 | $5.33 - j6.21$ | $11.42 - j2.25$ |
| 2110 | $5.44 - j5.88$ | $10.45 - j2.16$ |
| 2130 | $5.40 - j6.16$ | $11.28 - j2.14$ |
| 2150 | $5.12 - j6.06$ | $11.38 - j2.14$ |
| 2170 | $4.96 - j5.25$ | $11.04 - j1.25$ |
| 2190 | $4.98 - j4.47$ | $10.73 - j0.40$ |

Z_{source} = Test circuit impedance as measured from gate to gate, balanced configuration.

Z_{load} = Test circuit impedance as measured from drain to drain, balanced configuration.

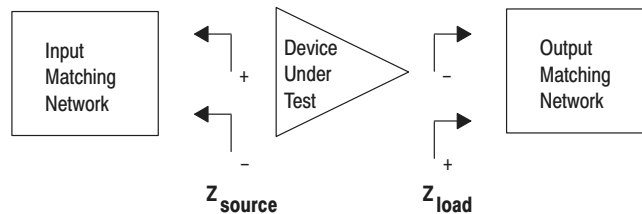
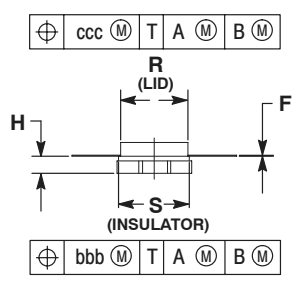
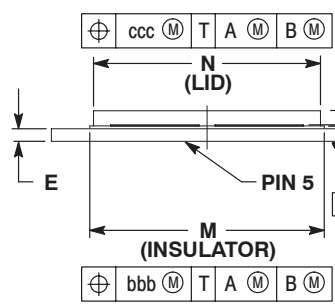
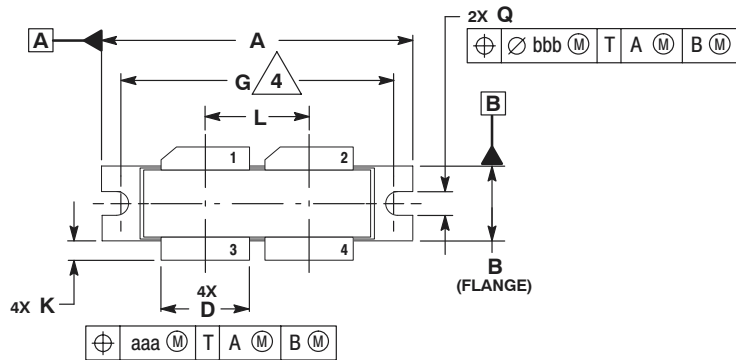


Figure 12. Series Equivalent Source and Load Impedance

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PACKAGE DIMENSIONS



- NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
 4. RECOMMENDED BOLT CENTER DIMENSION OF 1.52 (38.61) BASED ON M3 SCREW.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.615 | 1.625 | 41.02 | 41.28 |
| B | 0.395 | 0.405 | 10.03 | 10.29 |
| C | 0.150 | 0.200 | 3.81 | 5.08 |
| D | 0.455 | 0.465 | 11.56 | 11.81 |
| E | 0.062 | 0.066 | 1.57 | 1.68 |
| F | 0.004 | 0.007 | 0.10 | 0.18 |
| G | 1.400 BSC | | 35.56 BSC | |
| H | 0.079 | 0.089 | 2.01 | 2.26 |
| K | 0.117 | 0.137 | 2.97 | 3.48 |
| L | 0.540 BSC | | 13.72 BSC | |
| M | 1.219 | 1.241 | 30.96 | 31.52 |
| N | 1.218 | 1.242 | 30.94 | 31.55 |
| Q | 0.120 | 0.130 | 3.05 | 3.30 |
| R | 0.355 | 0.365 | 9.01 | 9.27 |
| S | 0.365 | 0.375 | 9.27 | 9.53 |
| aaa | 0.013 REF | | 0.33 REF | |
| bbb | 0.010 REF | | 0.25 REF | |
| ccc | 0.020 REF | | 0.51 REF | |

- STYLE 1:
1. PIN 1. DRAIN
 2. DRAIN
 3. GATE
 4. GATE
 5. SOURCE

**CASE 375D-04
ISSUE C
NI-1230**

Freescale Semiconductor, Inc.

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USA/EUROPE/LOCATIONS NOT LISTED:
 Motorola Literature Distribution
 P.O. Box 5405, Denver, Colorado 80217
 1-800-521-6274 or 480-768-2130

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center,
 3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573, Japan
 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong
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