

512KB and 1MB Synchronous Fast Static RAM Module

The MCM72F6A (512KB) is configured as 64K x 72 bits and the MCM72F7A (1MB) is configured as 128K x 72 bits. Both are packaged in a 168-pin dual-in-line memory module DIMM. Each module uses Motorola's 3.3 V 64K x 18 bit flow-through BurstRAMs.

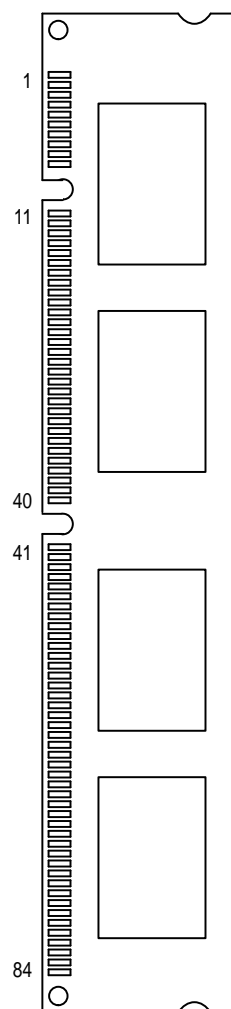
Address (A), data inputs (DQ, DP), and all control signals except output enable (G) are clock (K) controlled through positive-edge-triggered noninverting registers.

Write cycles are internally self-timed and initiated by the rising edge of the clock (K) input. This feature provides increased timing flexibility for incoming signals. Synchronous byte write (W) allows writes to either individual bytes or to both bytes.

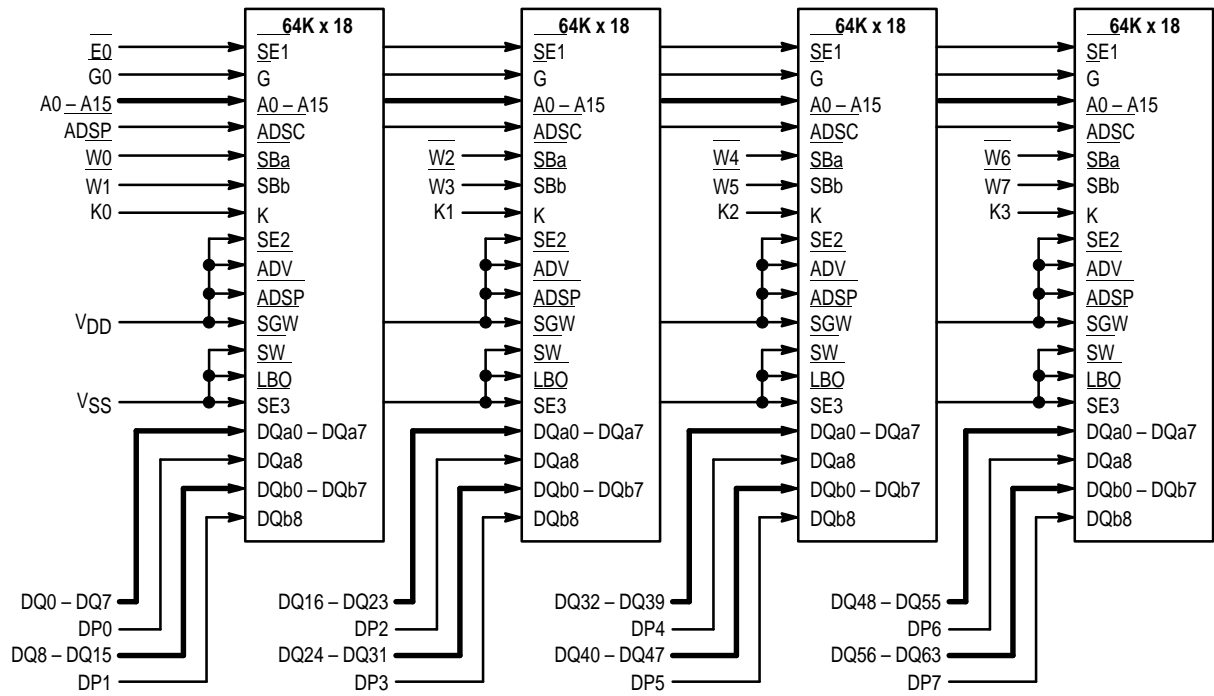
- Single 3.3 V + 10%, - 5% Power Supply
- Plug and Pin Compatibility with 2MB and 4MB
- Multiple Clock Pins for Reduced Loading
- All Inputs and Outputs are LVTTTL Compatible
- Byte Write Capability
- Fast SRAM Access Times: 9/10/12 ns
- Decoupling Capacitors for Each Fast Static RAM
- High Quality Multi-Layer FR4 PWB With Separate Power and Ground Planes
- Amp Connector, Part Number: 390064-4
- 5 V Tolerant on All Pins (Inputs and I/Os)
- 168-Pin DIMM Module

MCM72F6A
MCM72F7A

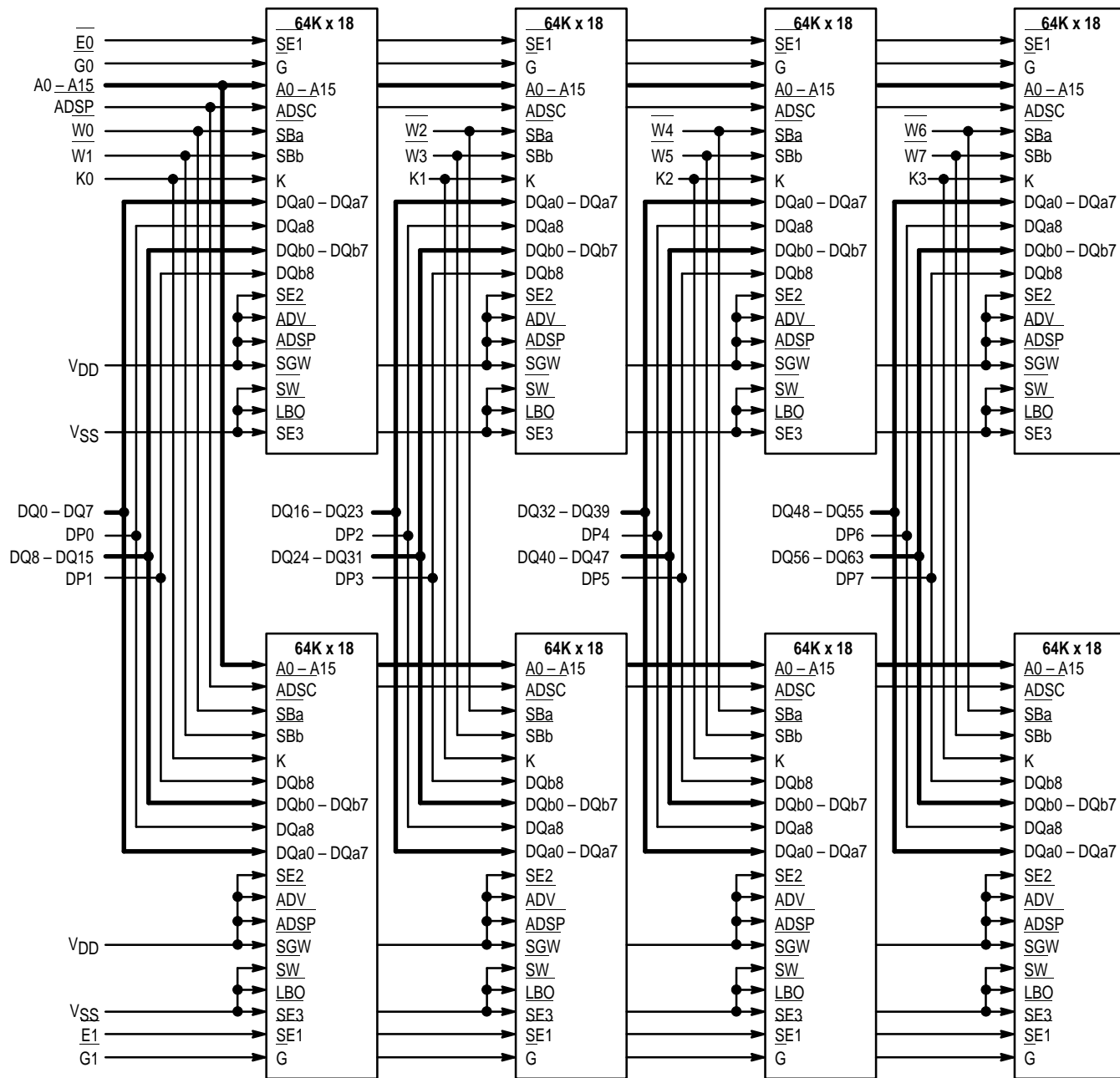
168-LEAD DIMM
CASE 1115J-01
TOP VIEW



MCM72F6A BLOCK DIAGRAM



MCM72F7A BLOCK DIAGRAM



PIN ASSIGNMENT
168-LEAD DIMM
TOP VIEW

VSS	1	85	VSS
DQ63	2	86	DP7
DQ62	3	87	DQ61
VDD	4	88	VSS
DQ60	5	89	DQ59
DQ58	6	90	DQ57
VSS	7	91	VSS
DQ56	8	92	DP6
DQ55	9	93	DQ54
VSS	10	94	VDD
DQ53	11	95	DQ52
DQ51	12	96	DQ50
VSS	13	97	VSS
DQ49	14	98	DQ48
DP5	15	99	DQ47
VDD	16	100	VSS
DQ46	17	101	DQ45
DQ44	18	102	DQ43
VSS	19	103	VSS
DQ42	20	104	DQ41
DQ40	21	105	DP4
VSS	22	106	VDD
DQ39	23	107	DQ38
DQ37	24	108	DQ36
VSS	25	109	VSS
DQ35	26	110	DQ34
DQ33	27	111	DQ32
VSS	28	112	VSS
K3	29	113	K2
VSS	30	114	VSS
DP3	31	115	DQ31
DQ30	32	116	DQ29
VDD	33	117	VSS
DQ28	34	118	DQ27
DQ26	35	119	DQ25
VSS	36	120	VSS
DQ24	37	121	DP2
DQ23	38	122	DQ22
VSS	39	123	VDD
DQ21	40	124	DQ20

DQ19	41	125	DQ18
VSS	42	126	VSS
DQ17	43	127	DQ16
DP1	44	128	DQ15
VDD	45	129	VSS
DQ14	46	130	DQ13
DQ12	47	131	DQ11
VSS	48	132	VSS
DQ10	49	133	DQ9
DQ8	50	134	DP0
VSS	51	135	VDD
DQ7	52	136	DQ6
DQ5	53	137	DQ4
VSS	54	138	VSS
DQ3	55	139	DQ2
DQ1	56	140	DQ0
VDD	57	141	VSS
NC	58	142	NC
NC	59	143	NC
VSS	60	144	VSS
NC	61	145	A15
A14	62	146	A13
VSS	63	147	VDD
A12	64	148	A11
A10	65	149	A9
VSS	66	150	VSS
A8	67	151	A7
A6	68	152	A5
VDD	69	153	VSS
A4	70	154	A3
A2	71	155	A1
A0	72	156	ADSP
VSS	73	157	VSS
K1	74	158	K0
VSS	75	159	VSS
W7	76	160	W6
W5	77	161	W4
VSS	78	162	VSS
W3	79	163	W2
W1	80	164	W0
VSS	81	165	VDD
G1	82	166	G0
E1	83	167	E0
VSS	84	168	VSS

PIN DESCRIPTIONS

Pin Locations	Symbol	Type	Description
72, 155, 71, 154, 70, 152, 68, 151, 67, 149, 65, 148, 64, 146, 62, 145	A0 – A15	Input	Synchronous Address Inputs: These inputs are registered and must meet setup and hold times.
156	ADSP	Input	Synchronous Address Status Controller: Initiates read, write, or chip deselect cycle.
134, 44, 121, 31, 105, 15, 92, 86	DP0 – DP7		Synchronous Parity Data Inputs/Outputs.
140, 56, 139, 55, 137, 53, 136, 52, 50, 133, 49, 131, 47, 130, 46, 128, 127, 43, 125, 41, 124, 40, 122, 38, 37, 119, 35, 118, 34, 116, 32, 115, 111, 27, 110, 26, 108, 24, 107, 23, 21, 104, 20, 102, 18, 101, 17, 99, 98, 14, 96, 12, 95, 11, 93, 9, 8, 90, 6, 89, 5, 87, 3, 2	DQ0 – DQ63	I/O	Synchronous Data Inputs/Outputs.
167, 83	E0, E1	Input	Synchronous Chip Enable: Active low to enable chip. Negated high — deselects chip when ADSP is asserted. E1 is only used on 1MB module.
166, 82	G0, G1	Input	Asynchronous Output Enable Input: Low — enables output buffer. High — DQx pins are high impedance. G1 is only used on 1MB module.
158, 74, 113, 29	K0 – K3	Input	Clock: This signal registers the address, data in, and all control signals except G0 and G1.
164, 80, 163, 79, 161, 77, 160, 76	W0 – W7	Input	Synchronous Byte Write Inputs.
4, 16, 33, 45, 57, 69, 94, 106, 123, 135, 147, 165	VDD	Supply	Power Supply: 3.3 V + 10%, – 5%. Must be connected on all modules.
1, 7, 10, 13, 19, 22, 25, 28, 30, 36, 39, 42, 48, 51, 54, 60, 63, 66, 73, 75, 78, 81, 84, 85, 88, 91, 97, 100, 103, 109, 112, 114, 117, 120, 126, 129, 132, 138, 141, 144, 150, 153, 157, 159, 162, 168	VSS	Supply	Ground.
58, 59, 61, 142, 143	NC		No Connection: There is no connection to the chip.

DATA RAM MCM69F618A SYNCHRONOUS TRUTH TABLE (See Notes 1, 2, 3, and 4)

Next Cycle	Address Used	Ex	ADSP	Gx	DQx	WRITE
Deselect	None	1	0	X	High-Z	X
Begin Read	External Address	0	0	0	DQ	Read
Read	Current	X	1	1	High-Z	Read
Read	Current	X	1	0	DQ	Read
Begin Write	External	0	0	X	High-Z	Write
Write	Current	X	1	X	High-Z	Write

NOTES:

1. X = don't care, 1 = logic high, 0 = logic low.
2. Write is defined as any Wx low.
3. G is an asynchronous signal and is not sampled by the clock K. G drives the bus immediately (t_{GLQX}) following G going low.
4. On write cycles that follow read cycles, G must be negated prior to the start of the write cycle to ensure proper write data setup times. G must also remain negated at the completion of the write cycle to ensure proper write data hold times.

ABSOLUTE MAXIMUM RATINGS (Voltages Referenced to $V_{SS} = 0$ V)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{DD}	- 0.5 to + 4.6	V
Voltage Relative to V_{SS}	V_{in}, V_{out}	- 0.5 to + 6.0	V
Output Current (per I/O)	I_{out}	± 20	mA
Power Dissipation	MCM72F6A MCM72F7A	P_D 4.6 9.2	W
Temperature Under Bias	T_{bias}	- 10 to + 85	$^{\circ}C$
Storage Temperature	T_{stg}	- 55 to + 125	$^{\circ}C$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established.

This device contains circuitry that will ensure the output devices are in High-Z at power up.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{DD} = 3.3$ V + 10%, - 5%, $T_A = 0$ to $70^{\circ}C$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (Voltages Referenced to $V_{SS} = 0$ V)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{DD}	3.135	3.6	V
Input High Voltage	V_{IH}	2.0	5.5**	V
Input Low Voltage	V_{IL}	- 0.5*	0.8	V

* $V_{IL} \geq -2.0$ V for $t \leq t_{KHKH}/2$.

** $V_{IH} \leq 6$ V for $t_{KHKH}/2$.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (0 V $\leq V_{in} \leq V_{DD}$)	$I_{kg}(I)$	—	± 1.0	μA
Output Leakage Current (0 V $\leq V_{in} \leq V_{DD}$)	$I_{kg}(O)$	—	± 1.0	μA
Output Low Voltage ($I_{OL} = + 8.0$ mA)	V_{OL}	—	0.4	V
Output High Voltage ($I_{OH} = - 4.0$ mA)	V_{OH}	2.4	—	V

POWER SUPPLY CURRENTS

Parameter	Symbol	Min	Max	Unit
AC Supply Current (Device Selected, All Outputs Open, Cycle Time $\geq t_{KHKH}$ min)	I_{DDA}	—	900 860 840 1800 1720 1680	mA
CMOS Standby Supply Current (Deselected, Clock (K) Cycle Time $\geq t_{KHKH}$, All Other Inputs CMOS Levels $V_{in} \leq V_{SS} + 0.2$ V or $\geq V_{DD} - 0.2$ V)	I_{SB1}	—	440 400 380 880 800 760	mA
Clock Running Supply Current (Deselected, Clock (K) Cycle Time $\geq t_{KHKH}$, All Other Inputs Held to Static CMOS Levels $V_{in} \leq V_{SS} + 0.2$ V or $\geq V_{DD} - 0.2$ V)	I_{SB2}	—	160 140 320 280	mA

MCM72F6A CAPACITANCE ($f = 1.0$ MHz, $dV = 3.0$ V, $T_A = 0$ to $70^{\circ}C$, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	C_{in}	—	16 36	pF
I/O Capacitance	$C_{I/O}$	—	19	pF

MCM72F7A CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 0 to 70 °C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance	W, K	—	22	pF
	E, G	—	36	
	Other Inputs	—	60	
I/O Capacitance	C _{I/O}	—	28	pF

MASS (Periodically Sampled Rather Than 100% Tested)

Parameter	Max	Unit
MCM72F6A	16	g
MCM72F7A	20	g

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{DD} = 3.3 V + 10%, - 5%, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level 1.5 V Output Timing Reference Level 1.5 V
 Input Pulse Levels 0 to 3.0 V Output Load See Figure 1 Unless Otherwise Noted
 Input Rise/Fall Time 1 V/ns (20 to 80%)

DATA RAMs READ/WRITE CYCLE TIMING (See Notes 1, 2, 3, and 4)

Parameter	Symbol	MCM72F6A-9 MCM72F7A-9		MCM72F6A-10 MCM72F7A-10		MCM72F6A-12 MCM72F7A-12		Unit	Notes	
		Min	Max	Min	Max	Min	Max			
Cycle Time	t _{KHKH}	12	—	15	—	16.6	—	ns		
Clock High Pulse Width	t _{KHKL}	4	—	5	—	6	—	ns		
Clock Low Pulse Width	t _{KLKH}	4	—	5	—	6	—	ns		
Clock Access Time	t _{KHQV}	—	9	—	10	—	12	ns		
Output Enable to Output Valid	t _{GLQV}	—	5	—	5	—	6	ns		
Clock High to Output Active	t _{KHQX1}	0	—	0	—	0	—	ns	5	
Clock High to Output Change	t _{KHQX2}	3	—	3	—	3	—	ns	5	
Output Enable to Output Active	t _{GLQX}	0	—	0	—	0	—	ns	5	
Output Disable to Q-High-Z	t _{GHQZ}	—	5	—	5	—	6	ns	5, 6	
Clock High to Q-High-Z	t _{KHQZ}	3	5	3	5	3	6	ns	5, 6	
Setup Times	Address	t _{AVKH}	2.5	—	2.5	—	2.5	—	ns	
	ADSP	t _{ADKH}								
	Data In	t _{DVKH}								
	Write	t _{WVKH}								
Chip Enable	t _{EVKH}									
Hold Times:	Address	t _{KHAX}	0.5	—	0.5	—	0.5	—	ns	
	ADSP, ADSC, ADV	t _{KHADX}								
	Data In	t _{KHDX}								
	Write	t _{KHWX}								
	Chip Enable	t _{KHEX}								

NOTES:

1. In setup and hold times, write refers to any Wx low.
2. Chip Enable is defined as Ex low, whenever ADSP is asserted.
3. All read and write cycle timings are referenced from K or G.
4. G is a don't care after write cycle begins. To prevent bus contention, G should be negated prior to start of write cycle.
5. This parameter is sampled and not 100% tested.
6. Measured at ± 200 mV from steady state.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

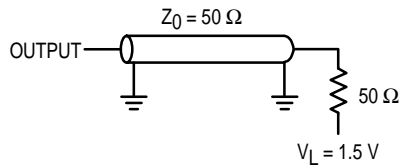
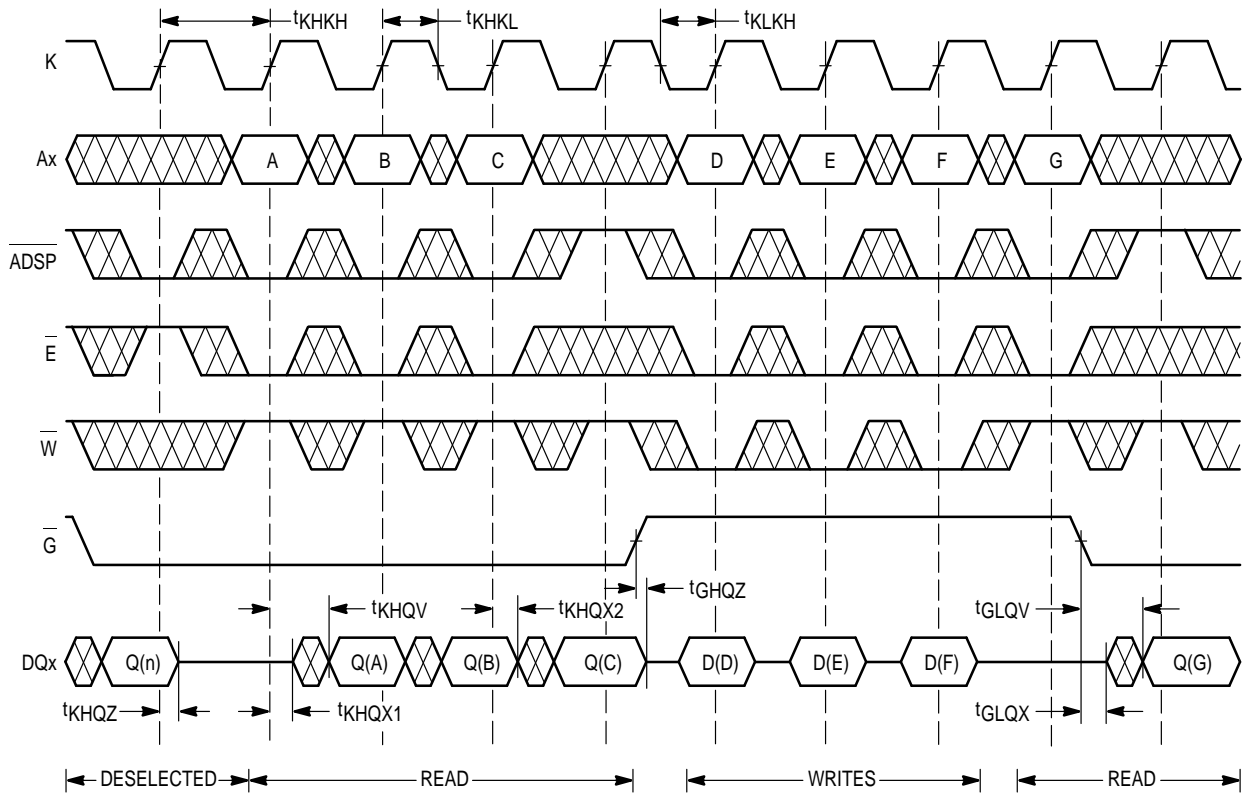
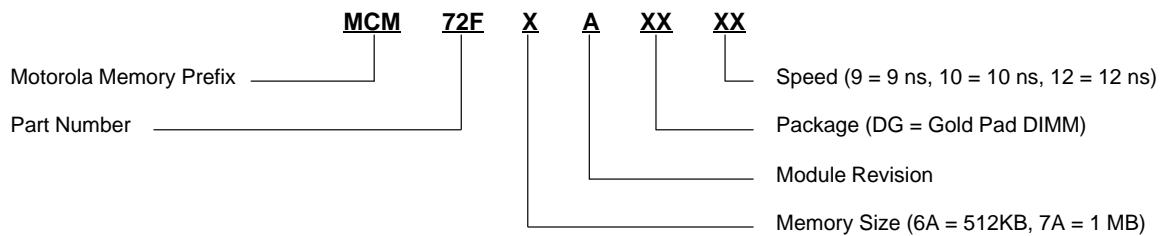


Figure 1. AC Test Load

READ/WRITE CYCLES



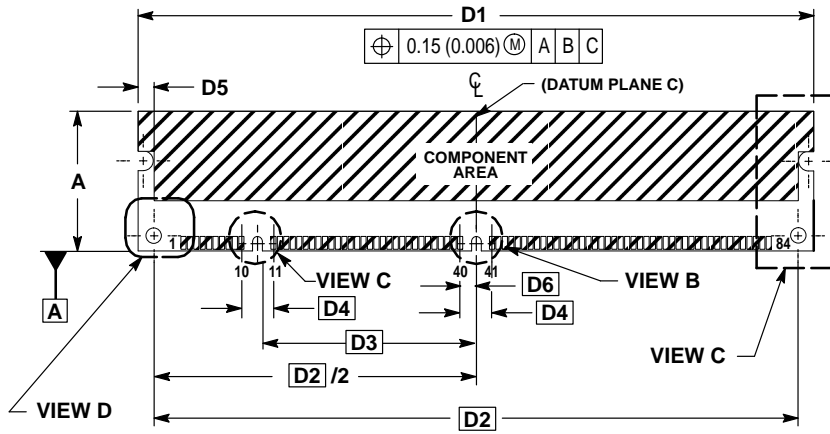
ORDERING INFORMATION (Order by Full Part Number)



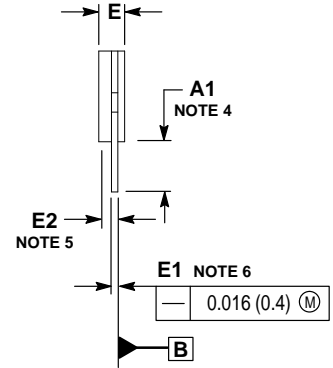
Full Part Numbers — MCM72F6ADG9 MCM72F6ADG10 MCM72F6ADG12
MCM72F7ADG9 MCM72F7ADG10 MCM72F7ADG12

PACKAGE DIMENSIONS

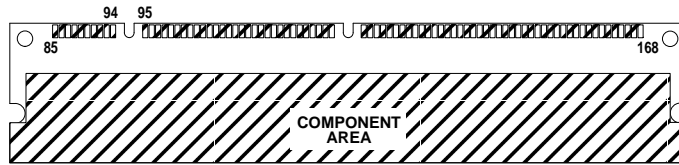
168-LEAD DIMM
CASE 1115J-01



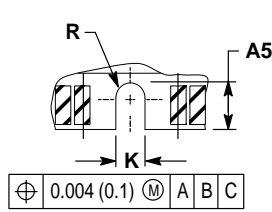
FRONT VIEW



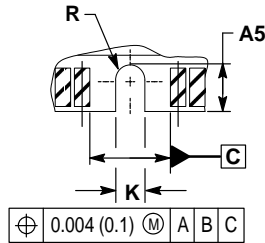
SIDE VIEW



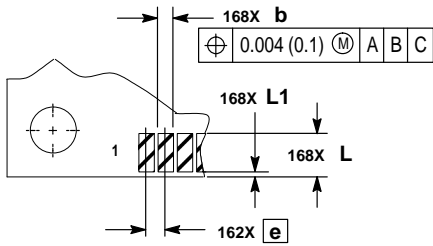
BACK VIEW



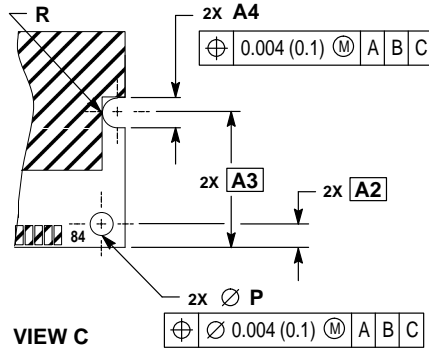
VIEW A



VIEW B



VIEW D




VIEW C

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. CARD THICKNESS APPLIES ACROSS TABS AND INCLUDES PLATING AND/OR METALLIZATION.
4. DIMENSIONS E AND A1 DEFINE A DOUBLE-SIDED MODULE.
5. DIMENSION E2 DEFINES OPTIONAL SINGLE-SIDED MODULE.
6. STRAIGHTNESS CALLOUT APPLIES TO TAB AREA ONLY.
7. D5 DIMENSION DEFINES SLOT END AND EDGE OF COMPONENT AREA.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.095	1.105	27.81	28.07
A1	0.390	—	9.90	—
A2	0.118 BSC	—	3.00 BSC	—
A3	0.700 BSC	—	17.78 BSC	—
A4	0.154	0.161	3.90	4.10
A5	0.118	0.128	3.00	3.25
b	0.037	0.041	0.95	1.05
D1	5.245	5.255	133.22	133.48
D2	5.014 BSC	—	127.35 BSC	—
D3	1.700 BSC	—	43.18 BSC	—
D4	0.250 BSC	—	6.35 BSC	—
D5	0.118	—	3.00	—
D6	0.125 BSC	—	3.175 BSC	—
e	0.050 BSC	—	1.27 BSC	—
E	—	0.200	—	4.00
E1	0.046	0.054	1.17	1.37
E2	—	0.148	—	2.70
K	0.075	0.083	1.90	2.10
L	0.100	—	2.54	—
L1	—	0.010	—	0.25
P	0.114	0.122	2.90	3.10

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