MOTOROLA

IEEE 802.3 10BASE-T Transceiver

MC34055

10BASE–T TRANSCEIVER

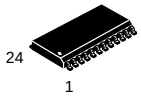
SEMICONDUCTOR TECHNICAL DATA

The Motorola 10BASE–T transceiver, designed to comply with the ISO 8802–3 [IEEE 802.3] 10BASE–T specification, will support a Medium Dependent Interface (MDI) in an embedded Media Attachment Unit (MAU)*. The interface supporting the Data Terminal Equipment (DTE) is TTL, CMOS, and raised ECL compatible, and the interface to the Twisted Pair (TP) media is supported through standard 10BASE–T filters and transformers. Differential data intended for the TP media is provided a 50 ns pre–emphasis and data at the TP receiver is screened by Smart Squelch circuitry for specific threshold, pulse width, and sequence requirements.

Other features of the MC34055 include: Collision and Jabber detection status outputs, select mode pins for forcing Loop Back and Full–Duplex operation, a Signal Quality Error pin for testing the collision detect circuitry without affecting the TP output, and a LED driver for Link Integrity status. An on–chip oscillator, capable of receiving a clock input or operating under crystal control, is also provided for internal timing and driving a buffered clock output.

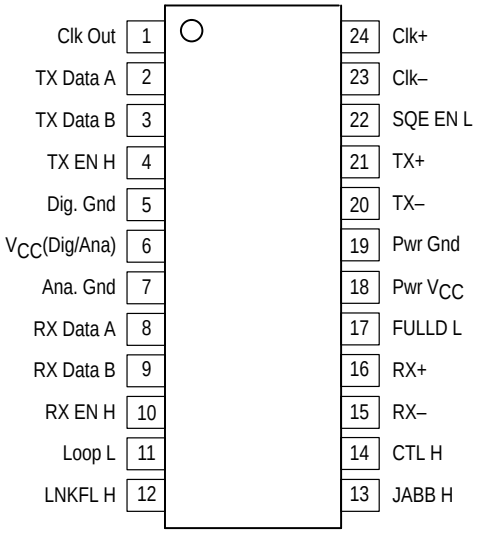
The MC34055 is manufactured on a BiCMOS process and is packaged in a 24 pin SOIC.

- BiCMOS Technology for Low Power Operation
- Standard 5.0 V, ± 5% Voltage Supply
- Smart Squelch Enforcement of Threshold, Pulse Width, and Sequence Requirements
- Driver Pre–Emphasis for Output Data
- TTL, CMOS and Raised ECL Compatible
- Interfaces to TP Media with Standard 10BASE–T Filters and Transformers
- LED Capable Status Outputs for Collision, Jabber Detection, and Link Integrity
- Directly Driven or Crystal Controlled Clock Oscillator
- Selectable Full–Duplex Operation
- Signal Quality Error Test Pin
- Selectable Loop Back



DW SUFFIX
PLASTIC PACKAGE
CASE 751E
(SO–24L)

PIN CONNECTIONS



MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted.)

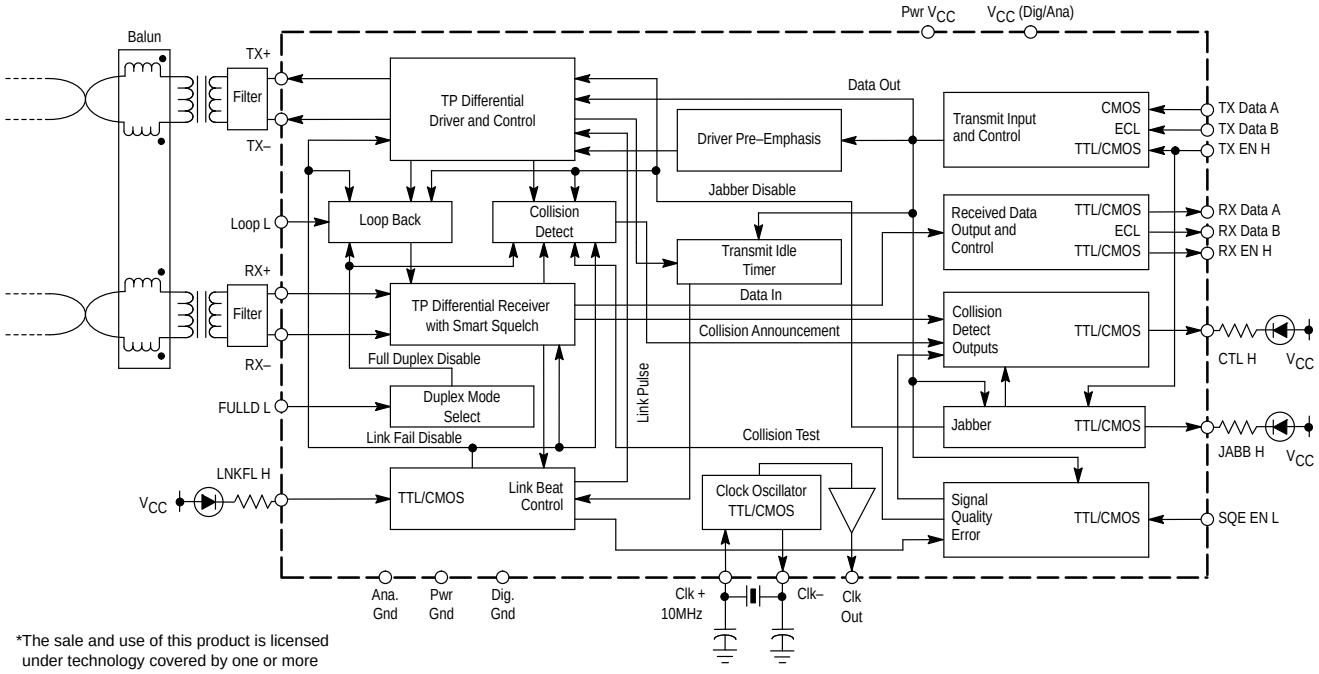
Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to 7.0	Vdc
Differential Voltage at RX+/RX–	V_{ID}	– 5.25 to 5.25	Vdc
Voltage Applied to Logic and Mode/Test Select Inputs		– 0.5 to 5.5	Vdc
Voltage Applied to Logic Outputs and Output Status Pins		– 0.5 to 7.0	Vdc
Ambient Operating Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J	– 65 to 150	°C

NOTE: Devices should not be operated at these limits. The "Recommended Operating Conditions" table provides for actual device operation.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC34055DW	T_A = 0° to +70°C	SO–24L

Simplified Block Diagram



*The sale and use of this product is licensed under technology covered by one or more Digital Equipment Corporation patents.

This device contains 9,875 active transistors.

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Voltage Applied to Logic Inputs and Status Pins	–	0	–	5.25	Vdc
Differential Input Voltage	–	0.59	–	2.8	Vpp
Operating Ambient Temperature	T_A	0	–	70	°C

NOTE: All limits are not necessarily functional concurrently.

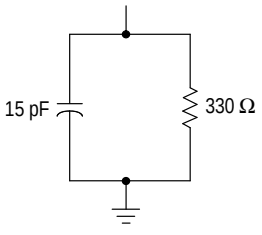
ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC} = 5.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current (4.75 V ≤ V_{CC} ≤ 5.25 V)	I_{CC}	–	60	180	mA
Reset Circuit Threshold	–	4.0	–	4.4	Vdc
TWISTED PAIR TRANSMITTER					
Output Differential Voltage (See Load Circuits: Differential Load Circuit) Output Differential Voltage with Pre–Emphasis Output Differential Voltage	V_O	 2.2 1.56	 2.53 1.72	 2.8 1.98	Vpp
Common Mode Driver Impedance	Z_{OCM}	6.0	8.5	14	Ω
Transmitter Differential Output Impedance	Z_{OD}	8.0	15.5	29	Ω
TX DATA A					
Input High Voltage (I_{IH} = + 20 μA) Input Low Voltage (I_{IL} = –150 μA)	V_{IH} V_{IL}	3.15 0	– –	5.25 0.8	Vdc
TX DATA B					
Input Voltage (See Load Circuits: ECL Load Circuit)					Vdc
High: @ 0°C	V_{IH}	0.984 V_{CC} – 0.923		0.984 V_{CC} – 0.763	
@ 25°C		0.984 V_{CC} – 0.877		0.984 V_{CC} – 0.727	
@ 70°C		0.984 V_{CC} – 0.825		0.984 V_{CC} – 0.644	
Low: @ 0°C	V_{IL}	0.750 V_{CC} – 0.568		0.750 V_{CC} – 0.361	
@ 25°C		0.750 V_{CC} – 0.550		0.750 V_{CC} – 0.350	
@ 70°C		0.750 V_{CC} – 0.531		0.750 V_{CC} – 0.324	

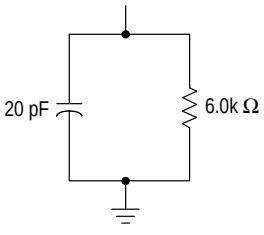
ELECTRICAL CHARACTERISTICS ($0°C \le T_A \le 70°C$, V_{CC} = 5.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TX EN H					
Input High Voltage (I_{IH} = 200 μA)	V_{IH}	2.0	–	5.0	Vdc
Input Low Voltage (I_{IL} = – 20 μA)	V_{IL}	0	–	0.8	
RX DATA A/RX EN H/JABB H/CTL H					
Output Voltage (See Load Circuits: CMOS Load Circuit)					Vdc
High (I_{OH} = –12 mA)	V_{OH}	3.7	–	–	
Low (I_{OL} = +16 mA)	V_{OL}	–	–	0.5	
RX DATA B					
Output Voltage (See Load Circuits: ECL Load Circuit)					Vdc
High: @ 0°C	V_{OH}	0.984 V_{CC} – 0.923		0.984 V_{CC} – 0.763	
@ 25°C		0.984 V_{CC} – 0.877		0.984 V_{CC} – 0.727	
@ 70°C		0.984 V_{CC} – 0.825		0.984 V_{CC} – 0.644	
Low: @ 0°C	V_{OL}	0.750 V_{CC} – 0.568		0.750 V_{CC} – 0.361	
@ 25°C		0.750 V_{CC} – 0.550		0.750 V_{CC} – 0.350	
@ 70°C		0.750 V_{CC} – 0.531		0.750 V_{CC} – 0.324	
SIGNAL QUALITY ERROR TEST ENABLE CONTROL (SQE EN L)					
Test Control Voltage					Vdc
Test Disabled (Input High Voltage)(I_{IH} = + 20 μA Max.)	V_{IH}	2.0	–	5.0	
Test Enabled (Input Low Voltage)(– 50 μA < I_{IL} < –150 μA)	V_{IL}	0	–	0.8	
FULL DUPLEX MODE SELECT (FULLD L)					
Mode Select Control Voltage					Vdc
Normal Operation (Input High)(I_{IH} = + 20 μA)	V_{IH}	2.0	–	5.0	
Full Duplex (Input Low)(– 50 μA < I_{IH} < –150 μA)	V_{IL}	0	–	0.8	
LOOPBACK TEST MODE FUNCTION (LOOP L)					
Test Control Voltage					Vdc
Test Disabled (Input High)(I_{IH} = + 20 μA)	V_{IH}	2.0	–	5.0	
Test Enabled (Input Low)(I_{IL} = – 200 μA)	V_{IL}	0	–	0.8	
LINK FAIL STATUS (LINKFL H)					
Status Output Voltage (See Load Circuits: CMOS Load Circuit)					
Maximum Voltage for Output Low Condition (I_{OL} = 20 mA)	V_{OH}	–	–	0.5	Vdc
Output Low Sink Current	V_{OL}	–	–	20	mA
CLOCK OSCILLATOR					
Clk+ Input Logic Threshold					
High Level Input Voltage (I_{IH} = +100 μA Max.)	V_{IH}	2.0	–	5.0	Vdc
Logic Low Input Voltage (I_{IL} = –100 μA Max.)	V_{IL}	–	–	0.8	μA
Clk Out Output Voltage (See Load Circuits: CMOS Load Circuit)					Vdc
Logic High (I_{OH} = –12 mA)	V_{OH}	3.7	3.9	–	
Logic Low (I_{out} = +16 μA)	V_{OL}	–	0.25	0.5	

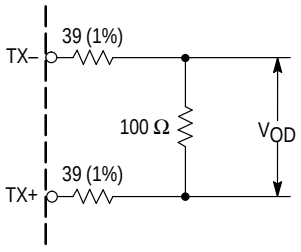
Output Load Circuits



ECL Load Circuit



TTL/CMOS Load Circuit



Differential Load Circuit

TIMING CHARACTERISTICS ($0°C \le T_A \le 70°C$)

Characteristic	Symbol	Min	Typ	Max	Unit
TRANSMIT START TIMING					
TX EN H to TX+/TX– Enable Time	t_{TXEN}	–	–	75	ns
TX Data A/B to TX+/TX– Enable Time	t_{FDXD}	–	–	75	ns
Steady State Propagation Delay of TX Data A/B to TX+/TX– Output	t_{TXSS}	–	–	75	ns
Pre–Emphasis Pulse Width	t_{PRCM}	45	–	55	ns
Transmitter Caused Edge Skew Between TX+ and TX–	$t_{Skew\ T}$	–	–	2.0	ns
Transmitter Added Edge Jitter to TX+/TX– from TX Data A/B	$t_{Jitter\ T}$	–	–	4.0	ns
Steady–State Delay between the TX Data A/B Input to the RX Data A/B Outputs for Normal Operation	t_{TXRX}	–	–	50	ns
TX EN H Assert to RX EN H Assert Under Normal Operation	t_{DREL}	–	–	50	ns
TRANSMIT STOP TIMING					
Delay between TX EN H Low and TX+/TX– High	t_{TXDH}	–	–	75	ns
TX EN H Assert/De–assert Delay from TX EN H to RX EN H Assert/De–assert	t_{XTRE}	–	–	400	ns
End of Packet Hold Time from Last TX Data A/B Edge or TX EN H De–assert	t_{TDDC}	250	–	–	ns
LINK BEAT PULSES					
Output Link Test Pulse Width	t_{LKPW}	80	–	120	ns
Minimum Link Beat Pulse Duration on RX+/RX–	t_{LDCY_A}	80	–	192	ns
LOOP BACK MODE TIMING					
Delay from Loop L Deassertion to RX EN H Driven from TX EN H Status	t_{LTRA}	–	–	30	ns
TX EN H Assert/De–assert to RX EN H, Assert/De–assert when in Loop–Back Mode and Receiver Inactive	t_{LTRX}	–	–	50	ns
Steady–State TX Data A/B to RX Data A/B when in Loop–Back Mode	t_{LTRD}	–	–	50	ns
SMART SQUELCH					
Interval Unit Squelch Deactivation	t_{SQ}	–	–	5.0	Bit Times
RECEIVE START TIMING					
Receiver–Added Edge Skew to RX Data A/B Signal	$t_{Skew\ R}$	–	–	1.5	ns
Receiver–Added Edge Jitter to RX Data A/B Signal	$t_{Jitter\ R}$	–	–	1.5	ns
Start–Up Delay from RX+/RX– to RX Data A/B	t_{RXNE}	–	–	50	ns
Delay from RX EN H Assertion Until RX Data A/B Valid	t_{RARE}	–10	–	+10	ns
Steady–State Propagation Delay from RX+/RX– Data A/B	t_{RXSS}	–	–	50	ns
RECEIVE SHUTDOWN TIMING					
Last received Data Edge until the RX EN H Output forces low	t_{RXDE}	155	–	250	ns

Figure 1. Start Up and Steady State Transmit Timing

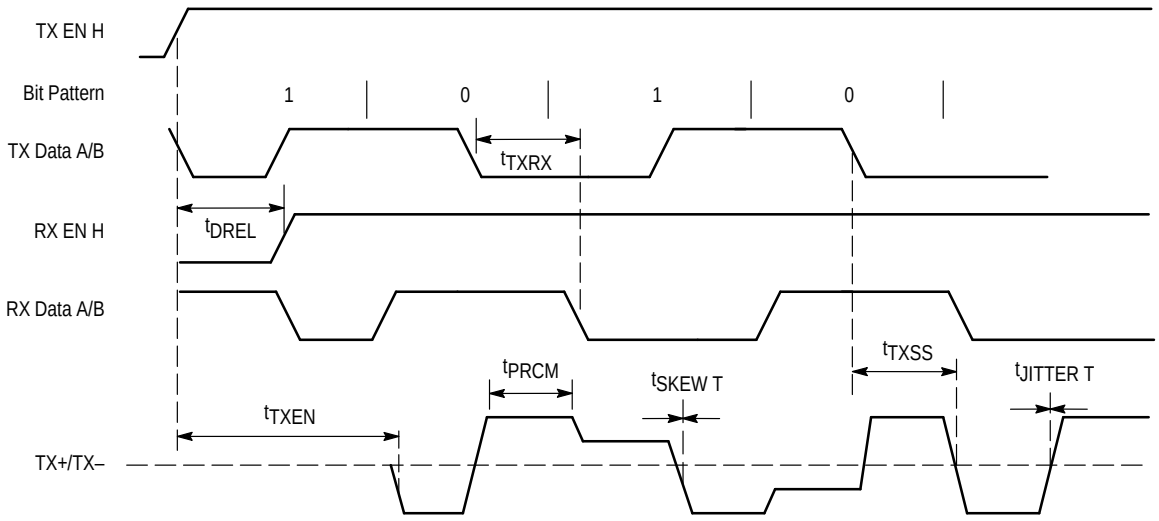


Figure 2. Driver Shutdown Timing

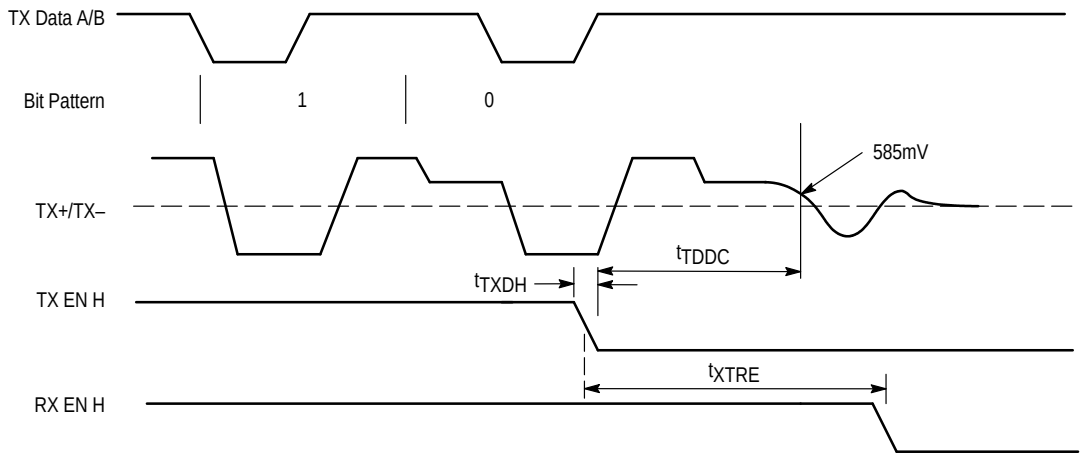


Figure 3. Link Pulse Timing

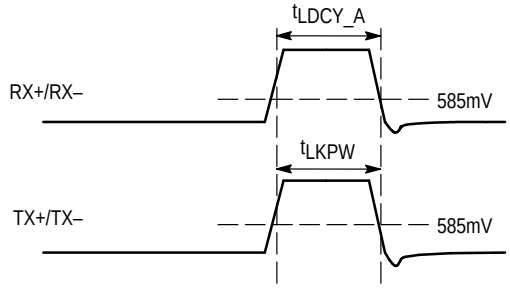


Figure 4. Loop Back Timing

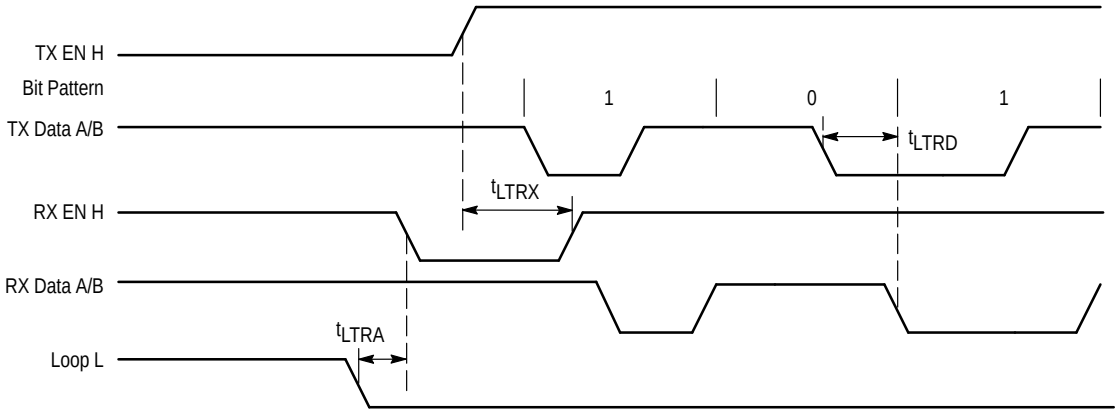


Figure 5. Receive Startup Timing

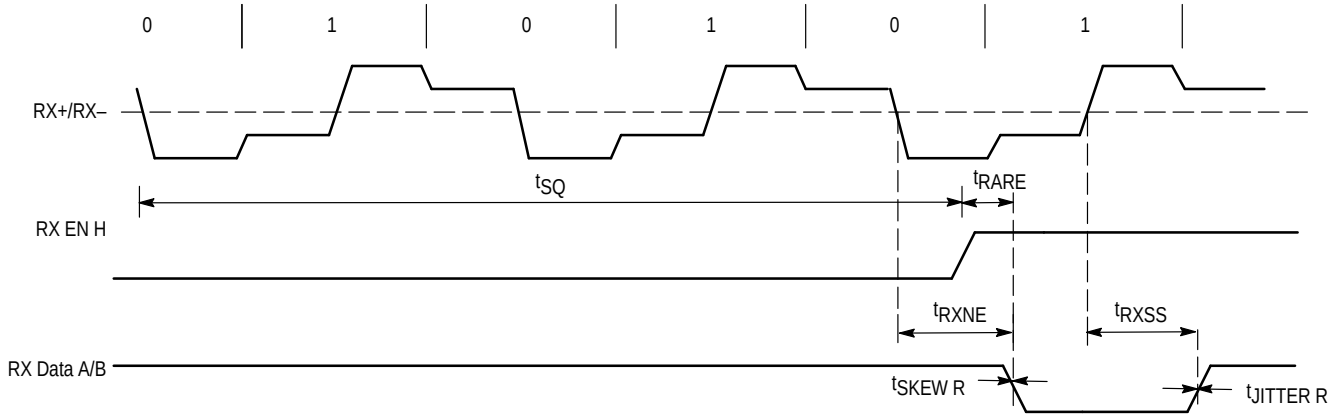
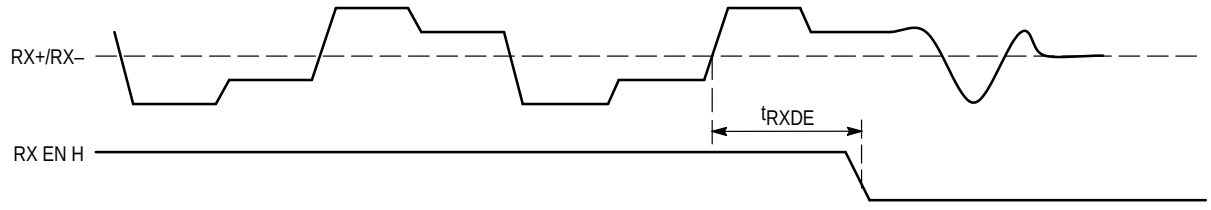


Figure 6. Receive Shutdown Timing



PIN FUNCTION DESCRIPTION

Pin	Symbol	Description
1	Clk Out	TTL/CMOS buffered 10 MHz clock output. This pin will source 400 μA and sink 16 mA.
2	TX Data A	CMOS transmit input pin. Data input at this pin is output to the TP media. The input will source less than 175 μA and sink less than 20 μA.
3	TX Data B	Raised ECL transmit input pin. Data input at this pin is output to the TP media. The input can source 40 μA for a high level input or 70 μA for a low level input.
4	TX EN H	TTL/CMOS transmit enable pin. Transmit is enabled when asserted high. The input will source less than 175 μA and sink less than 20 μA.
5	Dig. Gnd	Digital ground
6	V_{CC}(Dig/Ana)	Digital and analog V_{CC}. With the current consumed at this pin and Pin 18, the device will consume less than 180 mA at 5.0 Vdc.
7	Ana. Gnd	Analog ground
8	RX Data A	TTL/CMOS received data output pin. Data from the TP media is output at this pin. The output will source 12 mA and sink 16 mA.
9	RX Data B	Raised ECL received data output pin. Data from the TP media is output at this pin.
10	RX EN H	TTL/CMOS received data output enable pin. This pin is asserted after the Smart Squelch circuitry determines that there is valid data at the TP input pins and also when internal loop–back is occurring. The output will source 12 mA and sink 16 mA. The receive data outputs are forced high when this pin is low.
11	Loop L	TTL/CMOS Loopback test select. Asserting this pin causes the transmit data to be looped to the receive circuit while the TP transmit driver sends a link pulse. The input will source less than 175 μA and sink less than 20 μA.
12	LNKFL H	This pin is driven high to indicate a link fail state. When low, the pin will sink 20 mA to light an LED. An usquelched condition due to valid data on the receive circuit will cause the pin to transition high and low in 100 ms intervals.
13	JABB H	TTL/CMOS Jabber status pin. This pin is asserted when a Jabber condition is detected and will source 12 mA and sink 16 mA.
14	CTL H	TTL/CMOS status pin. This pin pulled high when Jabber or Collision conditions are detected. Also high for a time interval when a Signal Quality Error test is being performed. The pin will source 12 mA and sink 16 mA.
15	RX–	The inverting terminal of the TP differential receiver.
16	RX+	The noninverting terminal of the TP differential receiver.
17	FULLD L	TTL/CMOS duplex mode select. When low, this pin forces the device to operate in full–duplex mode. The input will source less than 175 μA and sink less than 20 μA.
18	Pwr V_{CC}	Power supply pin. With the current consumed at this pin and Pin 6, the device will consume less than 180 mA at 5.0 Vdc.
19	Pwr Gnd	Power ground pin.
20	TX–	The inverting terminal of the TP differential driver.
21	TX+	The noninverting terminal of the TP differential driver.
22	SQE EN L	TTL/CMOS Signal Quality Error test enable pin. Pulling this pin low allows test of the collision detect circuitry without affecting the twisted pair channel. The input will source less than 175 μA and sink less than 20 μA.
23	Clk–	TTL/CMOS clock oscillator pin. See Pin 24.
24	Clk+	TTL/CMOS clock oscillator pin. This pin is used with Pin 23 if the internal oscillator is to be free run with a crystal. The oscillator can also be directly driven with a TTL/CMOS clock signal at this pin. The oscillator frequency should be 10 MHz with a duty cycle of 50 ± 20%.

FUNCTIONAL DESCRIPTION

Introduction

The Motorola 10BASE–T transceiver, designed to comply with the ISO 8802–3[IEEE 802.3] 10BASE–T specification, will support one Medium Dependent Interface (MDI) through standard 10BASE–T filters and transformers. Although the device is capable of being used in embedded or external Medium Attachment Units (MAU), it was primarily designed for use in repeater or hub applications. For this reason a digital interface is provided rather than an AUI interface. This interface is TTL, CMOS, and raised ECL compatible and allows for easy connection in hub applications.

Other features of the MC34055 include: select mode pins of forcing Loop–Back and Full–Duplex operation; a Signal Quality Error pin for testing the collision detect circuitry without affecting the twisted pair output; and LED drivers for Link Integrity status; Collision detection; and Jabber detection. An on chip oscillator, capable of receiving a clock input or operating under crystal control, is also provided for internal timing and driving a buffered clock output.

Data Transmission

For data intended for the twisted pair, the MC34055 has two data inputs, TX Data A and TX Data B. TX Data A is CMOS compatible and TX Data B is raised ECL compatible. The inputs were not intended to be used simultaneously in a single application and are internally logically combined. The unused input should be disabled by connection to V_{CC}.

When data transmission is intended, the MC34055 detects the first falling edge of the Manchester encoded frame at the input being used, synchronizes the on chip oscillator (Pins 23 and 24) and asserts the twisted pair driver output to full differential amplitude within 25 ns if the driver enable pin (TX EN H) is previously asserted. Also, since twisted pair attenuates a 10 MHz signal more than a 5.0 MHz signal the 10BASE–T standard requires that data applied to the twisted pair receive pre–equalization. To fulfill this requirement the MC34055 provides an additional 730 mV for approximately 50 ns to output data. This is accomplished over the single pair of differential driver pins. TX+ and TX–, and effectively equalizes the power of all data components at the receiver. Figure 7A shows a 10 MHz waveform. Figure 7B shows the effect of pre–emphasis on a 5.0 MHz waveform. Manchester encoded data with the pattern shown in Figure 7A would represent a repeating pattern of zeros (000000...). Figure 7B would represent an alternating pattern of ones and zeros (0101010...).

Figure 7A. 10 MHz Waveform on Differential Outputs

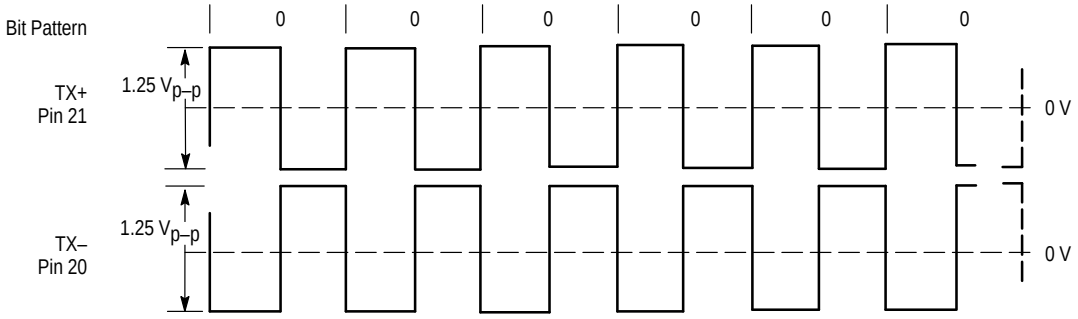
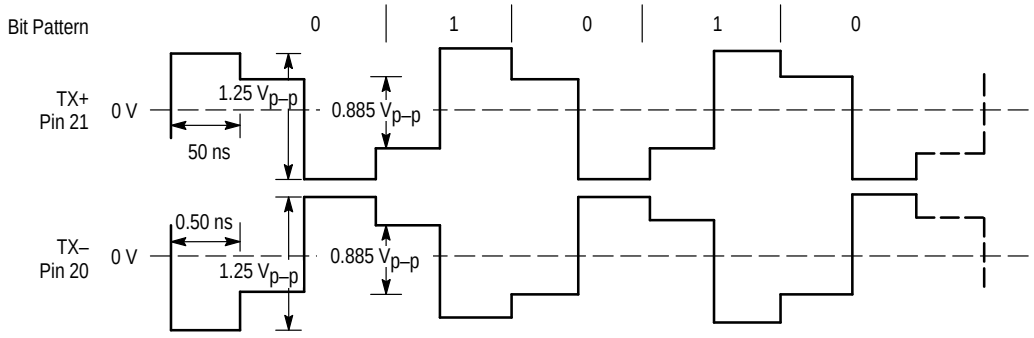


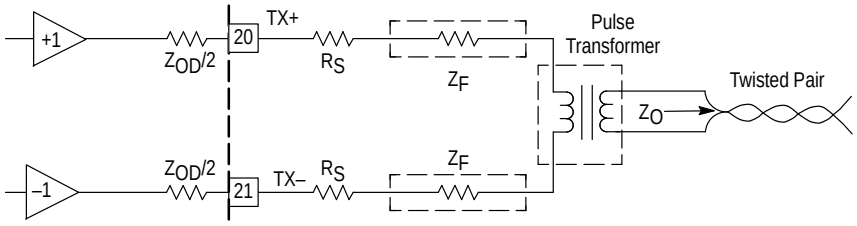
Figure 7B. 5.0 MHz Waveform on Differential Outputs



The figures show the voltage waveforms on the differential driver output pins. To actually meet the 10BASE–T specification requires bandpass filtering and a pulse transformer.

The output voltage waveform specifications of the IEEE 802.3 standard require that voltages impressed on the twisted pair meet a voltage template. The MC34055 can meet the voltage template for all the 10BASE–T applications by choosing the appropriate low pass filter and external components in the driver output circuitry. When the differential transmit driver output pins are configured to drive the bandpass filters and pulse transformer as shown in Figure 8, the resultant waveform is capable of meeting the voltage template.

Figure 8. Differential Driver Media Interface Circuitry



Where: Z_{OD} is the transmitters differential output impedance (~20 Ω),
R_S is a 1% series resistor,
Z_F is the filters impedance, and Z_O is the characteristic impedance of the twisted pair (100 Ω).

Following the end–of–frame activity, an internal pull–up resistor pulls TX Data A/B high and causes the differential driver to maintain full differential output voltage for approximately 250 ns. The differential driver interprets the lack of transition activity as an end of frame and starts an idle timer. Should another frame intended for the twisted pair arrive before the idle timer expires(~250 ns), the idle timer will be reset, if not, the transmit driver function will begin the decay to idle process. During idle periods the differential driver must force the media to a minimal differential voltage unless a link beat is being produced. The transition to minimal voltage is subject to performance requirements in the IEEE specification and is met by the MC34055 when the appropriate filters and transformers are used to interface to the media.

The MC34055 differential driver generates link pulses (beats) during idle periods. The link pulses produced are singular positive (TX+ positive with respect to TX–) pulses applied to the media at 16 ms intervals and last approximately 100 ns. The link pulses allow the receiver at the other end of the link to verify the validity of the segment. There is the possibility, due to the two asynchronous sources, that one of the two input pins (TX Data A or TX Data B) will receive frame activity immediately after a link pulse is initiated. In this event, the transmit differential driver will remain active for the entire frame interval and the link pulse will not affect more than one bit interval.

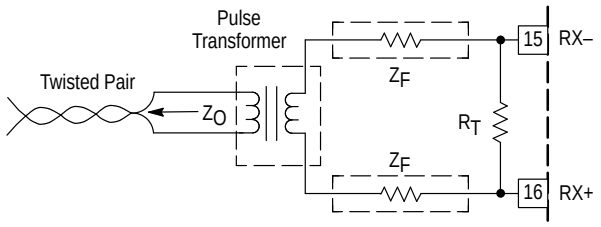
The MC34055 also has Jabber circuitry to detect and disable the twisted pair driver in the event that a serial controller fails constantly transmitting. Should any data source try to transmit longer than 20 ms minimum, the Jabber function will disable the differential driver outputs, the collision presence detector and the internal loopback function. Also, two status indicator pins, CTL H and JABB H are asserted. The MC34055 will remain in the jabber state until the TX EN H pin is pulled low or the jabbering input ceases to toggle for a minimum of 500 ms. The status indicator pins, CTL H and JABB H will also sink up to 20 mA and can therefore support external LEDs.

The driver also works with the receiver to provide loop–back. Under normal operating conditions (Loop L= “1”), the data applied to the TX Data A/B pins is looped back internally to the RX Data A/B pins. This function is disabled when there is a collision condition or FULLD L is low.

Data Reception

Data intended for the DTE proceeds from the twisted pair to the isolation transformer and bandpass filters before reaching the differential receiver terminals. Figure 9 shows the configuration of the external media receive circuitry. Once transitions at the receiver terminals (RX+ and RX–) are detected, the on–chip oscillator is synchronized and the received data is screened by smart squelch circuitry for validity. This qualification requires incoming data to meet amplitude and sequence requirements. If the data meets the Smart Squelch requirements, the receiver enters the unsquelch state and the data is forwarded to the RX Data A/B output pins provided Loop L is not low. Two data outputs are provided to increase design flexibility, RX Data A and RX Data B. RX Data A is CMOS/TTL compatible and RX Data B is raised ECL compatible.

Figure 9. Differential Receiver Media Interface Circuitry



Where: R_T is a terminating resistor (100 Ω),
Z_F is the filters impedance, and Z_O is the characteristic impedance of the twisted pair (100 Ω).

The MC34055 powers up in a squelched and “link OK” state, after which minimum and maximum link test and maximum link fail timers are started. If valid data or a link pulse is received after the link test minimum timer but before the link fail maximum timer times out, the timers are reset and begin counting again. In the event of missing or incorrect link pulses, the MC34055 enters the link fail state whereby the LNKFL H status pin is asserted until valid data or link pulse activity appears at the receiver terminals.

Powering up in the squelched state assures that the data path to the data output pin (RX Data A/B) is disabled, and prevents noise at the receiver terminals (RX+/RX–), from being interpreted as valid input data. Once transitions appear at the receiver terminals, the smart squelch circuitry checks for the smart squelch requirements to unsquelch; an alternating sequence (1010... or 0101...) of pulses with amplitude of at least 525 mV. This requirement is met by the preamble of an IEEE 802.3 frame with good signal to noise ratio.

After a pulse is received and checked for proper polarity and amplitude, the pulse width is checked for proper duration. If the duration is to short or too long the smart squelch circuitry resets and begins to look again for a proper sequence. By requiring the differential pulses to meet amplitude and sequence requirements, it is unlikely that pulses due to crosstalk from coresident twisted pairs are capable of causing the receiver to unsquelch. If a positive pulse is received first and the differential driver is not transmitting, the receiver should unsquelch after three alternating pulses. If a negative pulse is received first, one additional pulse is required before unsquelch. If the differential driver is transmitting, three additional pulses are required to unsquelch.

After meeting the smart squelch requirements, the MC34055 will pull high the RX EN H pin and enable the path to the receive data pin (RX Data A/B) provided the MC34055 is not in the loop back test mode (Loop L low). If the receiver unsquelches, the receive enable pin remains high and the data path to the receive data pin remains enabled until transitions cease to exist at the receiver terminals. Valid data reception is also indicated by high/low transitions of the LNKFL H pin at 100 ms intervals. When transitions at the differential terminals cease, marking the end of frame activity, the receiver re–enters the squelch state, pulls low on the RX EN H pin, and begins accepting valid link pulses until the start of the next 802.3 frame.

If the MC34055 is requested to begin transmitting (TX EN H is asserted), and the receiver unsquelches simultaneously, there is a collision. Also, if the MC34055 driver enable pin is previously asserted and the receiver detects valid transition activity, the receiver Smart Squelch circuitry verifies the possibility of collision by requiring three extra transitions at the differential receiver before the unsquelch condition is reached. If unsquelch occurs, a collision condition exists. During all collision conditions the MC34055 asserts the CTL H status pin for the duration of the condition and for a time after the end of collision.

During a collision condition the receive and transmit paths are still both enabled allowing transparency to the media. Either the presence of simultaneous transmit and receive activity or the condition of the CTL H status pin can be used by the communications controller to acknowledge and react to the collision. In applications where a 10 MHz collision signal is required by an SIA, the combination of this status pin and the clock oscillator output can be logically combined to provide a 10 MHz output. If the DTE reacts to the collision and ceases transmitting, the MC34055 will decay to idle until a re–transmit is attempted.

Crystal Oscillator

The MC34055 has an on–chip clock oscillator used to provide a reliable and accurate time reference to all the internal timers. The oscillator can be run with a crystal or driven at Pin 24 from an external clock source. Also provided is a buffered clock output which is useful if the MC34055 is to be used in a repeater or concentrator application.

Table 1. The crystal used in the oscillator is subject to the following specifications.

Crystal Operating Mode	Fundamental
Crystal Cut Type	AT
Crystal External Shunt Capacitance	7.0 pF Max
Crystal Resonant Mode	Series
Crystal Accuracy	± 0.01% @ 25°C
Crystal Temperature Variance	0.005% from 0° to 70°C
Crystal Series Resistance	25 Ω Max, 17 Ω Typical
Crystal Operating Temperature Range	0° to 70°C

LOOP L Test Mode

If the Loop L pin is low, the MC34055 is in a test mode whereby the data at the input pin (TX Data A/B) is being looped back internally to the receive data pin(RX Data A/B). In this mode the data path from the differential receiver terminals to the receive data output pins (RX Data A/B) is disconnected while the Smart Squelch functionality of the differential receiver is still operational. This test mode allows the DTE to test the MC34055 internal loop back circuitry since the data is looped back to the receive circuitry as close to the twisted pair interface as possible.

Signal Quality Error Test

The MC34055 also provides the ability to test the collision detect circuitry without disabling either of the data paths. By pulling the SQE EN L pin low, a collision test is provided to the collision detect circuitry immediately following the last edge of a transmitted 802.3 frame. The test verifies the operability of the collision detect circuitry, operability is announced by the assertion of the CTL H pin for a period following a valid data transmission.

Jabber Detection

The transmit circuitry of the MC34055 has the ability to monitor and shut down the differential driver in the event of a jabber condition. If transmission activity ever exceeds 20 ms minimum, the differential driver, the collision detect, and internal loop back circuits are disabled. To announce the presence of a jabber condition, both the CTL H and the JABB H status output pins are asserted. In order to end the jabber condition, the TX Data A/B input must stop toggling, or the TX EN H pin must be pulled low for a minimum of 500 ms. The status output pins have the ability to drive an external led and were added to facilitize network manageability. The jabber status outputs will not assert during power up or power down.

Full Duplex Mode

The MC34055 can be operated in a full–duplex mode if required. When the FULLD L pin is pulled low the device will enter the full duplex mode. This mode allows the transmitter and driver to operate independently. Collision will not be announced and the internal loop back operation is disabled. The Signal Quality Error test, however, is still operational if enabled.

Status Pins

The MC34055 has three status indicator pins capable of sourcing or sinking enough current to support an external LED. Status pin levels (“1” or “0”) report the condition of the transceiver. Table 2 shows the combinations and significance.

Table 2

Status Pin			Condition
JABB H	CTL H	LNKFL H	
“0”	“1”	X	Collision condition or Signal Quality Error test.
“1”	“1”	X	Jabber condition
X	X	“0”	Link Failure. Incorrect or nonexistent link pulses, or lack of data at the receiver terminals.
X	X	“1”	Link “OK”. Receiving link pulses.
X	X	“0101…”	Link “OK”. Receiving valid data.

Test Select Pins

The MC34055 has three operation mode test select pins, Loop L, SQE EN L and FULLD L. The level of the pin determines the mode of operation. Table 3 shows the levels and corresponding conditions of the status pins.

Table 3

Pin	Status	Condition
Loop L	“1”	Normal operating mode. Loop back occurs when the transmitter initiates and the receiver is receiving link pulses. The RX EN H pin follows the TX EN H pin and the transmit data appears on the RX Data A/B output pin being used.
	“0”	Loop back test mode. The transmit circuit is looped back internally as close to the differential receive circuit as possible. In this mode the RX EN H pin follows the TX EN H pin and the transmit data appears on the RX Data A/B output pin being used. Any received data other than link pulses are ignored and the receiver will not unsquelch or announce collision.
SQE EN L	“0”	Normal operating mode. Concurrent transmit and receive activity results in a collision condition.
	“1”	Test enabled. An internal test is run on the collision circuitry and the CTL H pin is asserted for a time window following the last positive packet edge. Data transmission and reception is undisturbed.
FULLD L	“1”	Normal operating mode. Internal loop–back is operable and collision is announced.
	“0”	Internal loop–back is disabled and collision will not be announced. Signal Quality Error test is still operable.

APPLICATIONS INFORMATION

The MC34055 implements the physical layer of a 10BASE–T application of IEEE 802.3. It provides the physical connection to the media (twisted pair) and the services required by the MAC sublayer of the Data Link Layer. Two interfaces are defined in the IEEE 802.3 specification of the physical layer; one is the MDI providing connection to the twisted pair; and the other is the AUI providing connection to the encoder/decoder function of the Data Link Layer. While the MC34055 provides the connection to the twisted pair, a CMOS and raised ECL interface is provided instead of an AUI.

The MC34055 implements the twisted pair interface of the physical layer in a 802.3 10BASE–T application but circuitry must be added if an AUI is desired, (see Figure 10 for suggested schematic). For example, an external MAU application requires the AUI and a twisted pair interface. A chip capable of realizing the AUI interface is the Texas Instruments SN75ALS085. This IC has an AUI interface and another interface which is compatible with the MC34055. The differential input of the 75ALS085 can be used for the TX+/TX– terminals of the AUI. The differential drivers of the 75ASL085 can be used as the RX+/RX– and the COL+/COL– terminals of the AUI. The other interface of the 75ALS085 then will interface to the MC34055 by three paths shown in the application suggestion. The application accounts for all the inputs/outputs of an external MAU.

Embedded applications do not require a full AUI and a MC10116 can be used to interface between the raised ECL interfaces of the MC34055 and the AUI of existing encoder/decoder chips. The MC10116 is a MECL 10k Triple Line Receiver with typical propagation delay and rise and fall times (20% to 80%) of 2.0 ns. Figure 11 shows the use of the MC10116 with the MC34055 and the AMD 7992 SIA.

In a multi–port repeater, or hub, a port is required for each DTE connected to the IEEE 802.3 network. This port consists of two connections, one for the TX+/TX– pair and another for the RX+/RX– pair. The repeater unit then multiplexes these lines so that all of the stations are capable of transmitting to or receiving from all the other stations on the network. This establishes the need for a transceiver without an AUI interface. If an AUI is present with each 10BASE–T transceiver, chip count is increased because there is a requirement to convert from balanced to unbalanced lines before multiplexing.

An application suggestion for the use of the MC34055 used in a multiport repeater is shown in Figure 6. Here the receive and transmit lines for the 10BASE–T transceivers are multiplexed by the hub hardware.

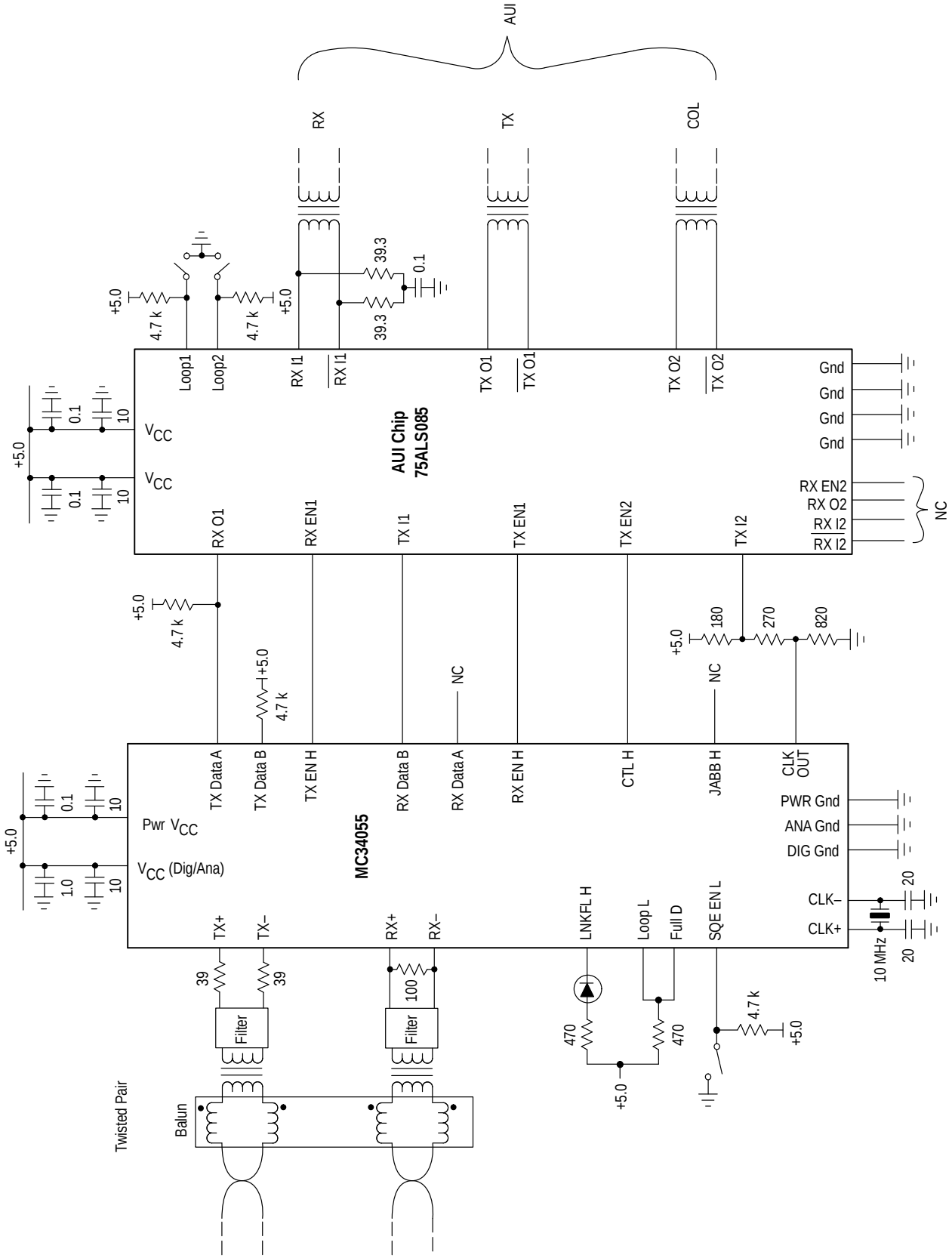


Figure 10. External MAU Application

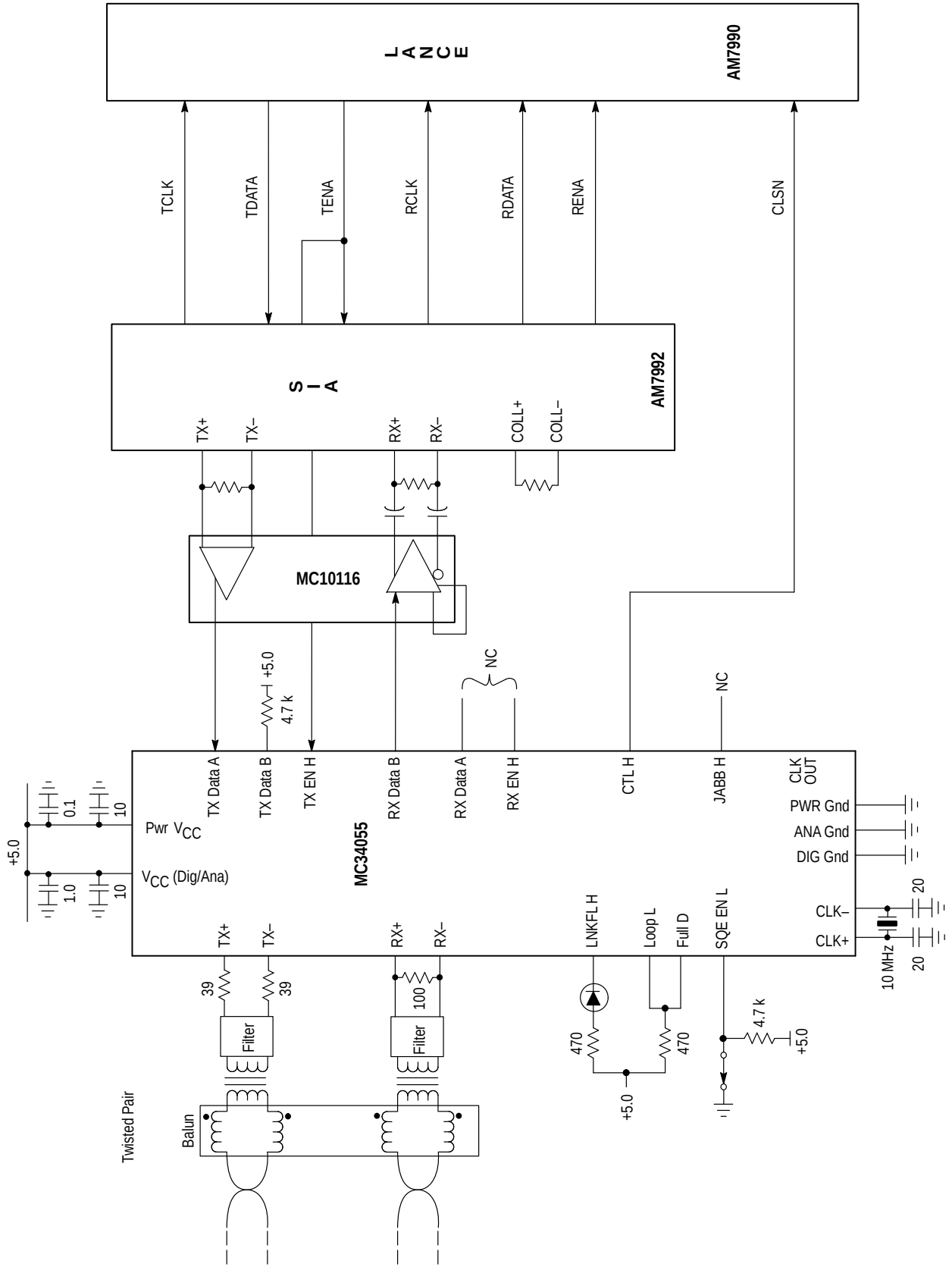


Figure 11. Internal MAU Application

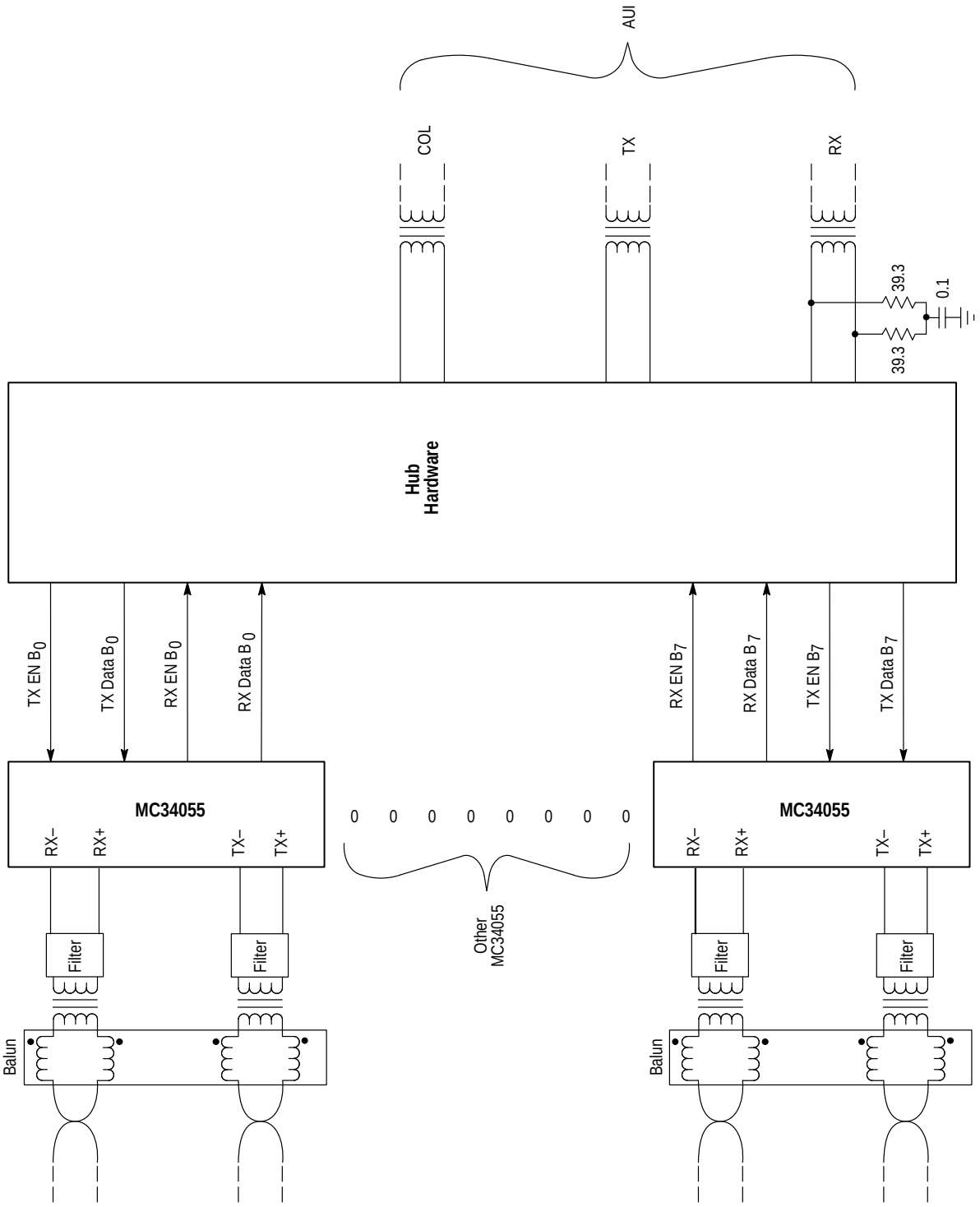
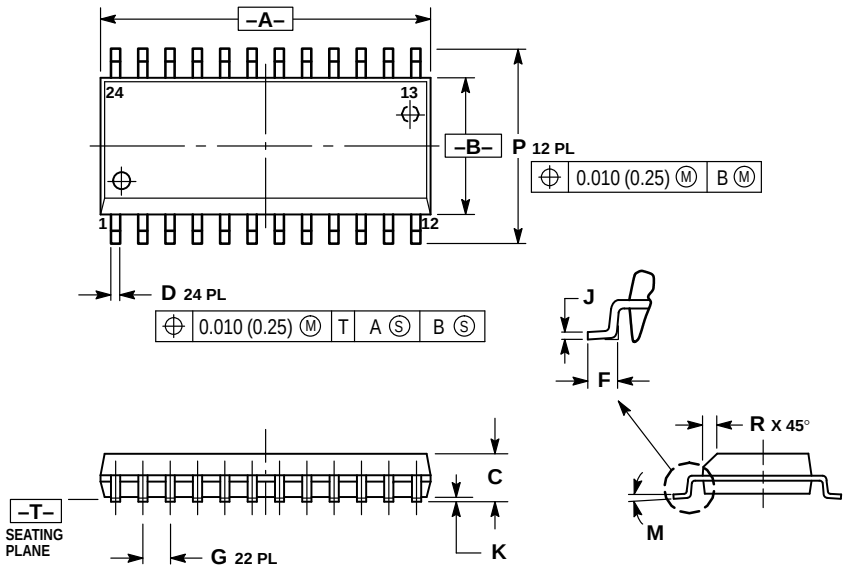


Figure 12. 10BASE–T Connecentrator Application

OUTLINE DIMENSIONS

DW SUFFIX
PLASTIC PACKAGE
CASE 751E–04
(SO–24L)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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