

# Dual 10-bit bus interface latch (3-State)

# MB2841

## FEATURES

- High speed parallel latches
- Live insertion/extraction permitted
- Extra data width for wide address/data paths or buses carrying parity
- Power-up 3-State
- Power-up reset
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors

- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The MB2841 Bus interface register is designed to provide extra data width for wider data/address paths of buses carrying parity.

The MB2841 consists of two sets of ten D-type latches with 3-State outputs. The flip-flops appear transparent to the data when Latch Enable (nLE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the nLE High-to-Low transition, the data that meets the setup and hold time is latched.

Data appears on the bus when the Output Enable (nOE) is Low. When nOE is High the output is in the High-impedance state.

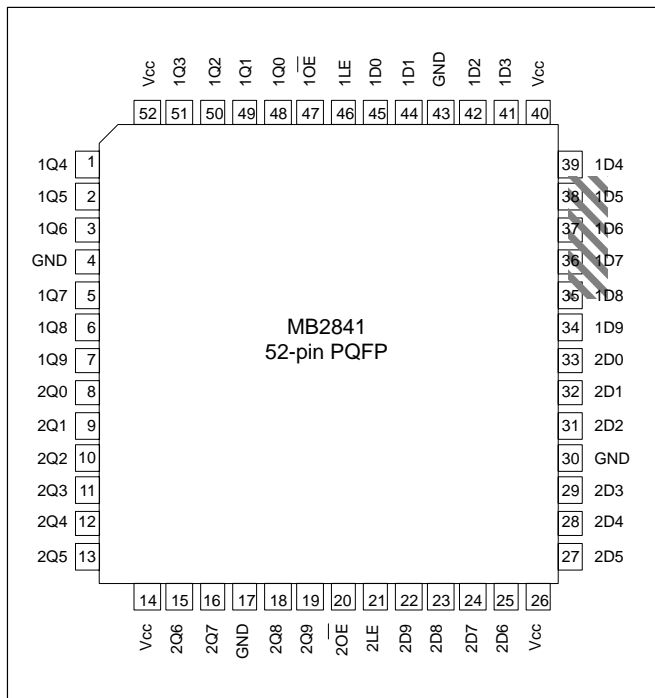
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T <sub>amb</sub> = 25°C; GND = 0V	TYPICAL	UNIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nDx to nQx	C <sub>L</sub> = 50pF; V <sub>CC</sub> = 5V	3.5	ns
C <sub>IN</sub>	Input capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	4	pF
C <sub>OUT</sub>	Output capacitance	V <sub>O</sub> = 0V or V <sub>CC</sub> ; 3-State	7	pF
I <sub>CCZ</sub>	Total supply current	Outputs disabled; V <sub>CC</sub> = 5.5V	120	μA

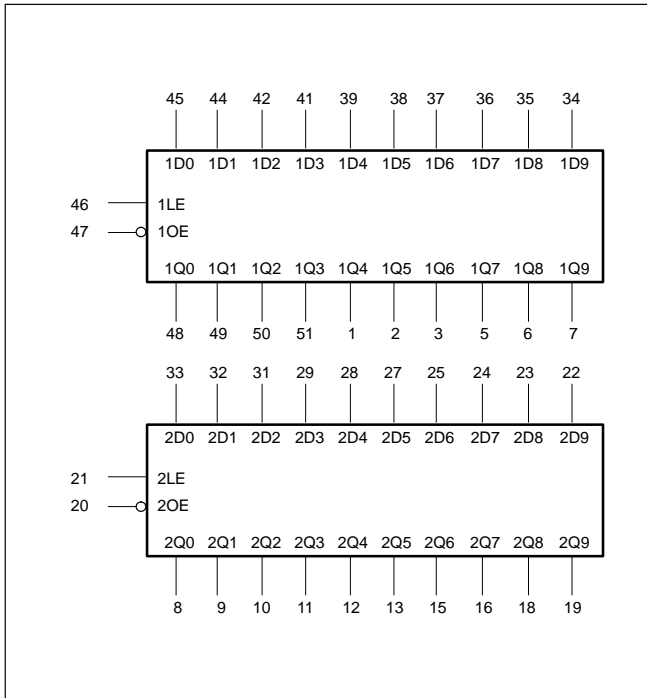
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DRAWING NUMBER
52-pin Plastic Quad Flat Pack (PQFP)	-40°C to +85°C	MB2841BB	1418B

## PIN CONFIGURATION



## LOGIC SYMBOL



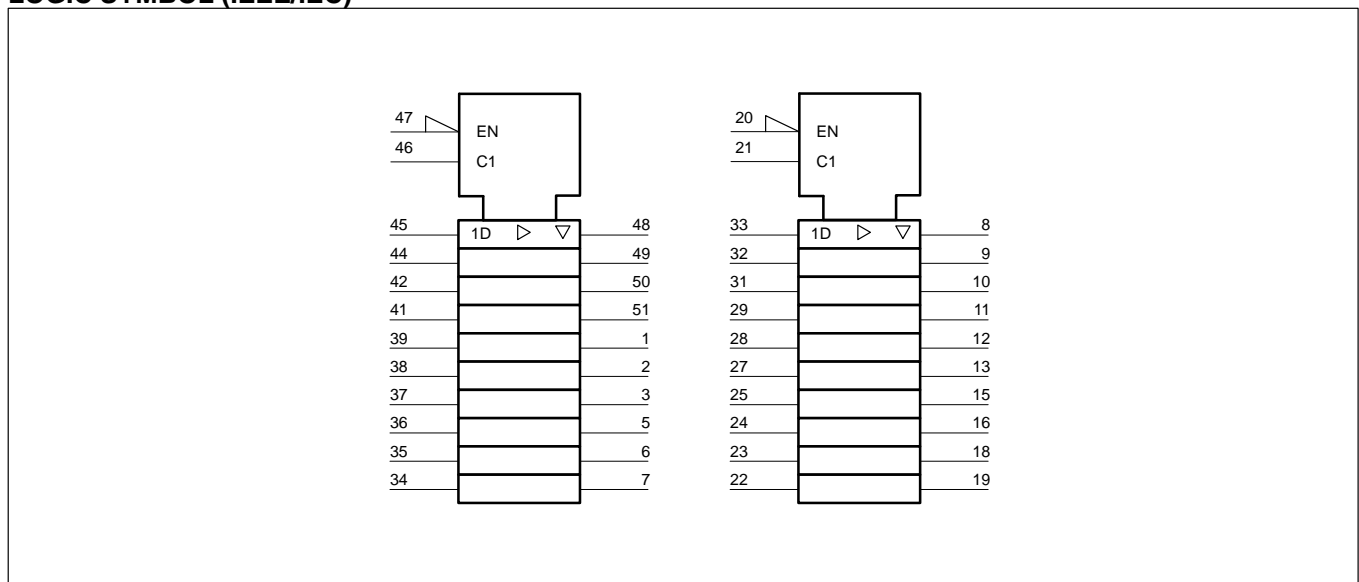
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## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
45, 44, 42, 41, 39, 38, 37, 36, 35, 34, 33, 32, 31, 29, 28, 27, 25, 24, 23, 22	1D0 – 1D9 2D0 – 2D9	Data inputs
48, 49, 50, 51, 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15, 16, 18, 19	1Q0 – 1Q9 2Q0 – 2Q9	Data outputs
47, 20	1 $\overline{OE}$ , 2 $\overline{OE}$	Output enable inputs (active-Low)
46, 21	1LE, 2LE	Latch enable inputs (active rising edge)
4, 17, 30, 43	GND	Ground (0V)
14, 26, 40, 52	V <sub>CC</sub>	Positive supply voltage

## LOGIC SYMBOL (IEEE/IEC)



## FUNCTION TABLE

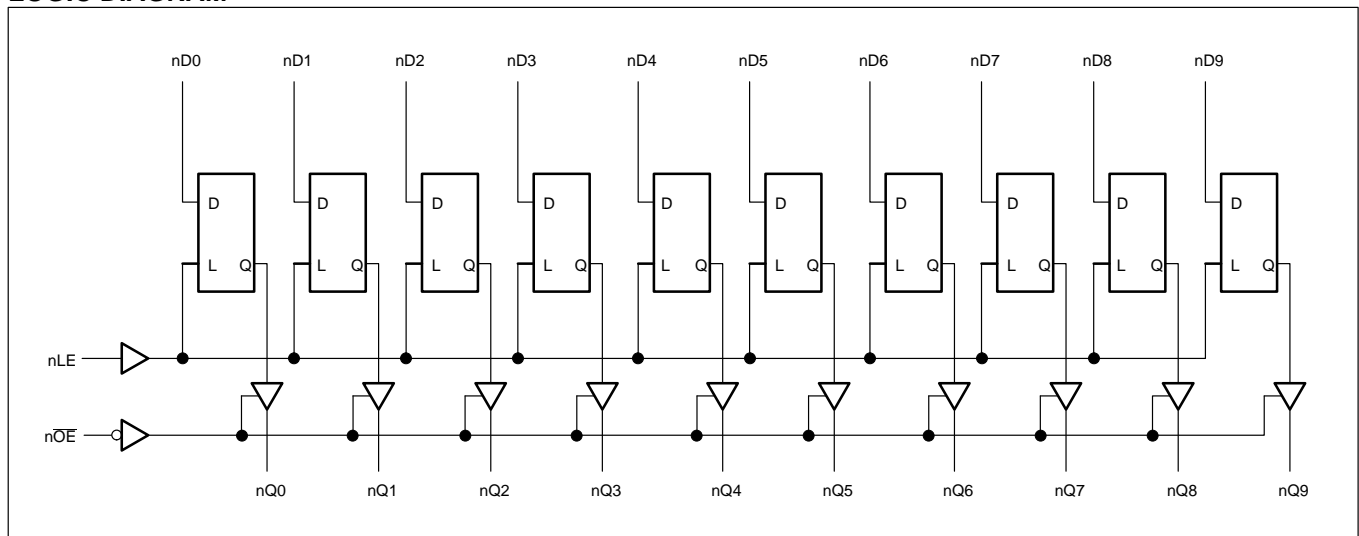
INPUTS			OUTPUTS	OPERATING MODE
n $\overline{OE}$	nLE	nDx	nQ0 – nQ9	
L	H	L	L	Transparent
L	H	H	H	
L	↓	l	L	Latched
L	↓	h	H	
H	X	X	Z	High impedance
L	L	X	NC	Hold

H = High voltage level  
 h = High voltage level one set-up time prior to the High-to-Low LE transition  
 L = Low voltage level  
 l = Low voltage level one set-up time prior to the High-to-Low LE transition  
 ↓ = High-to-Low LE transition  
 NC= No change  
 X = Don't care  
 Z = High impedance "off" state

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## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$	-18	mA
$V_I$	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	output in Low state	128	mA
$T_{stg}$	Storage temperature range		-65 to 150	°C

### NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level Input voltage		0.8	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			MIN	TYP	MAX	MIN	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.4		3.0		V
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4		2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.42	0.55		0.55	V
V <sub>RST</sub>	Power-up output voltage <sup>NO TAG</sup>	V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.13	0.55		0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±0.01	±1.0		±1.0	µA
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5V		±5.0	±100		±100	µA
I <sub>PU/PD</sub>	Power-up/down 3-State output current <sup>4</sup>	V <sub>CC</sub> = 2.1V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = Don't care		±5.0	±50		±50	µA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		5.0	50		50	µA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-5.0	-50		-50	µA
I <sub>CEx</sub>	Output High leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		5.0	50		50	µA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	-50	-70	-180	-50	-180	mA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		120	250		250	µA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>		56	76		76	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>		120	250		250	µA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5V; one input at 3.4V, other inputs at V <sub>CC</sub> or GND		0.5	1.5		1.5	mA

**NOTES:**

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. For valid test results, data must not be loaded into the flip-flops (or latches) after applying the power.
4. This parameter is valid for any V<sub>CC</sub> between 0V and 2.1V with a transition time of up to 10msec. From V<sub>CC</sub> = 2.1V to V<sub>CC</sub> = 5V ± 10% a transition time of up to 100µsec is permitted.

## AC CHARACTERISTICS

GND = 0V, t<sub>R</sub> = t<sub>F</sub> = 2.5ns, C<sub>L</sub> = 50pF, R<sub>L</sub> = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V			T <sub>amb</sub> = -40 to +85°C V <sub>CC</sub> = +5.0V ±0.5V		
			MIN	TYP	MAX	MIN	MAX	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nDx to nQx	2	1.5 1.7	3.1 3.5	4.4 4.7	1.5 1.7	5.0 5.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay nLE to nQx	1	2.4 2.9	4.2 4.6	5.7 6.0	2.4 2.9	6.5 6.7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output enable time to High and Low level	4 5	1.3 2.3	3.1 4.0	4.2 5.2	1.3 2.3	4.9 5.9	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output disable time from High and Low level	4 5	1.0 1.5	3.3 3.2	4.6 4.5	1.0 1.5	5.1 5.0	ns

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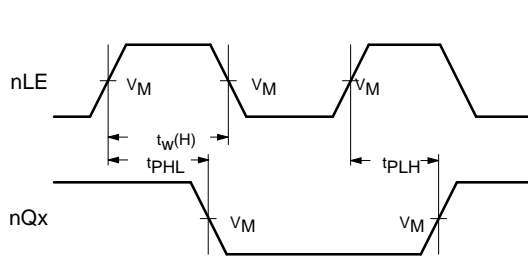
## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

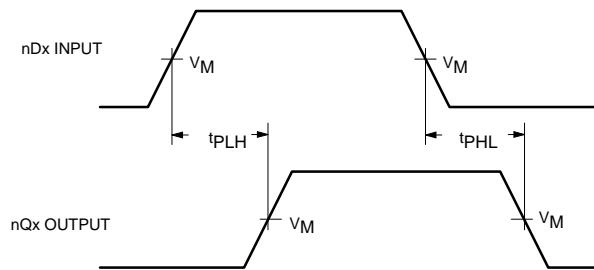
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40 \text{ to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low nDx to nLE	3	2.0 1.5	0.8 0.4		2.0 1.5		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low nDx to nLE	3	0.5 0.5	-0.3 -0.7		0.5 0.5		ns
$t_w(\text{H})$	nLE pulse width High	1	2.9	1.9		2.9		ns

## AC WAVEFORMS

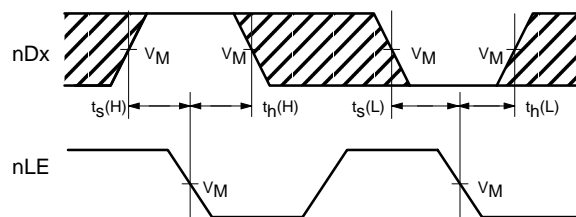
$V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



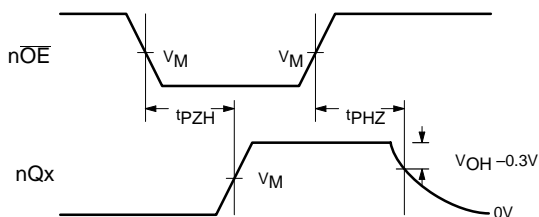
Waveform 1. Propagation Delay, Latch Enable Input to Output, and Enable Pulse Width



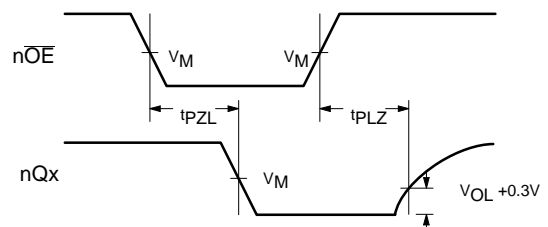
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times



Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



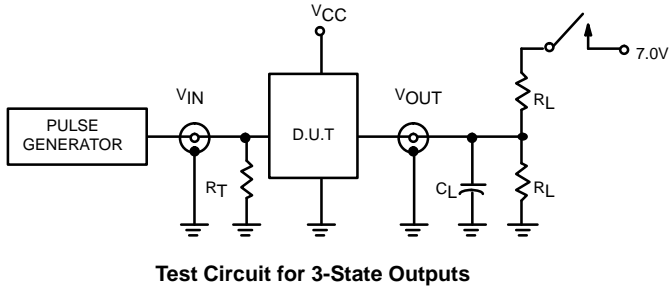
Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

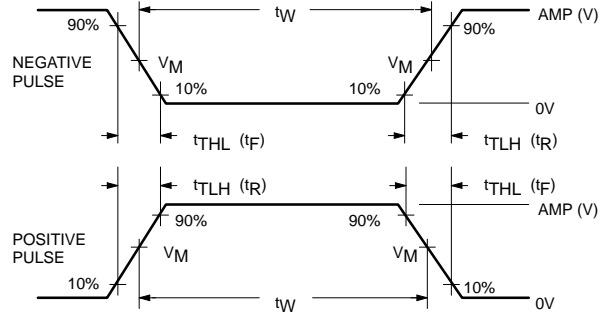
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## TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V<sub>M</sub> = 1.5V  
Input Pulse Definition

### SWITCH POSITION

TEST	SWITCH
t <sub>PLZ</sub>	closed
t <sub>pZL</sub>	closed
All other	open

### DEFINITIONS

R<sub>L</sub> = Load resistor; see AC CHARACTERISTICS for value.

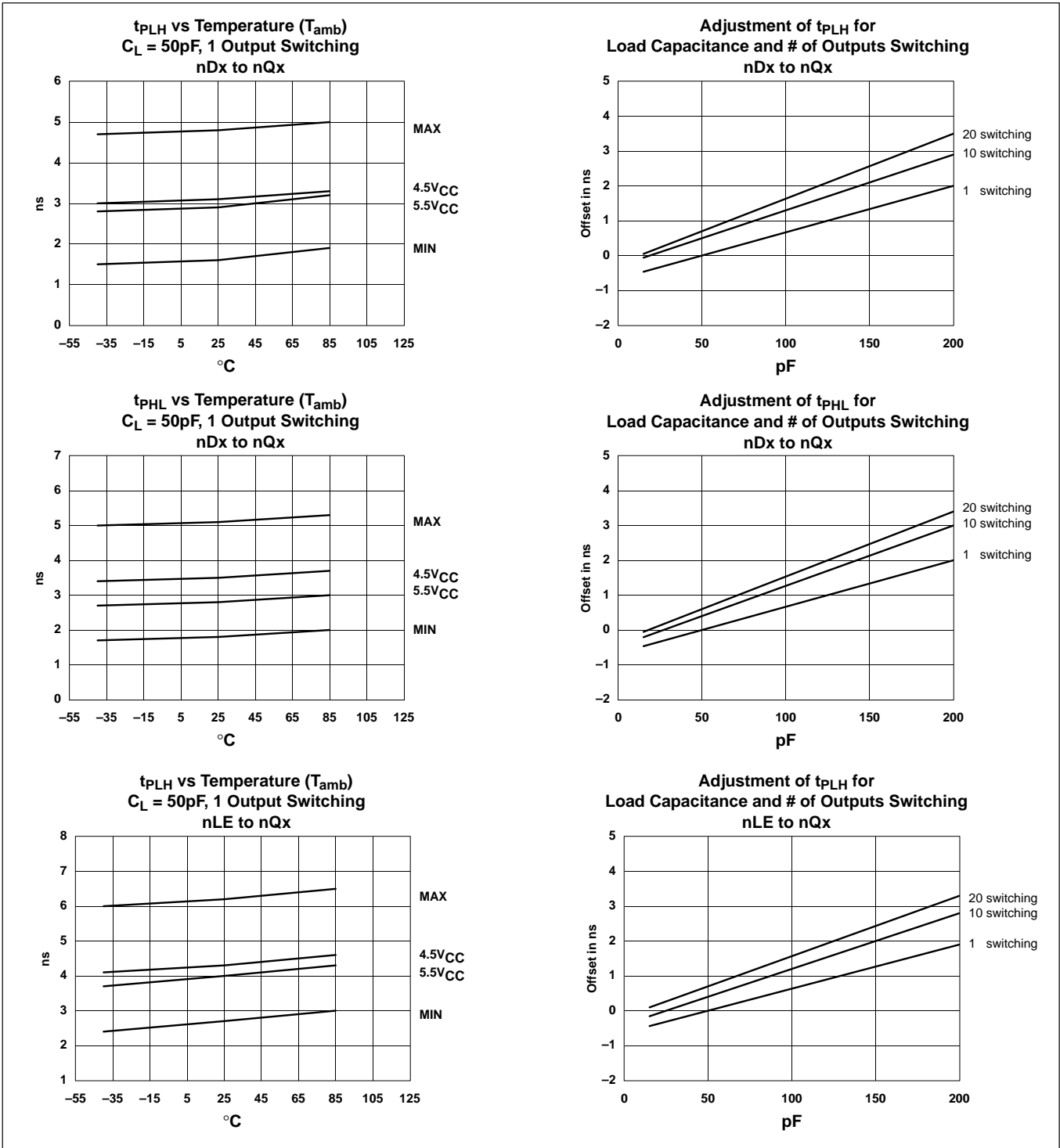
C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t <sub>W</sub>	t <sub>R</sub>	t <sub>F</sub>
MB	3.0V	1MHz	500ns	2.5ns	2.5ns

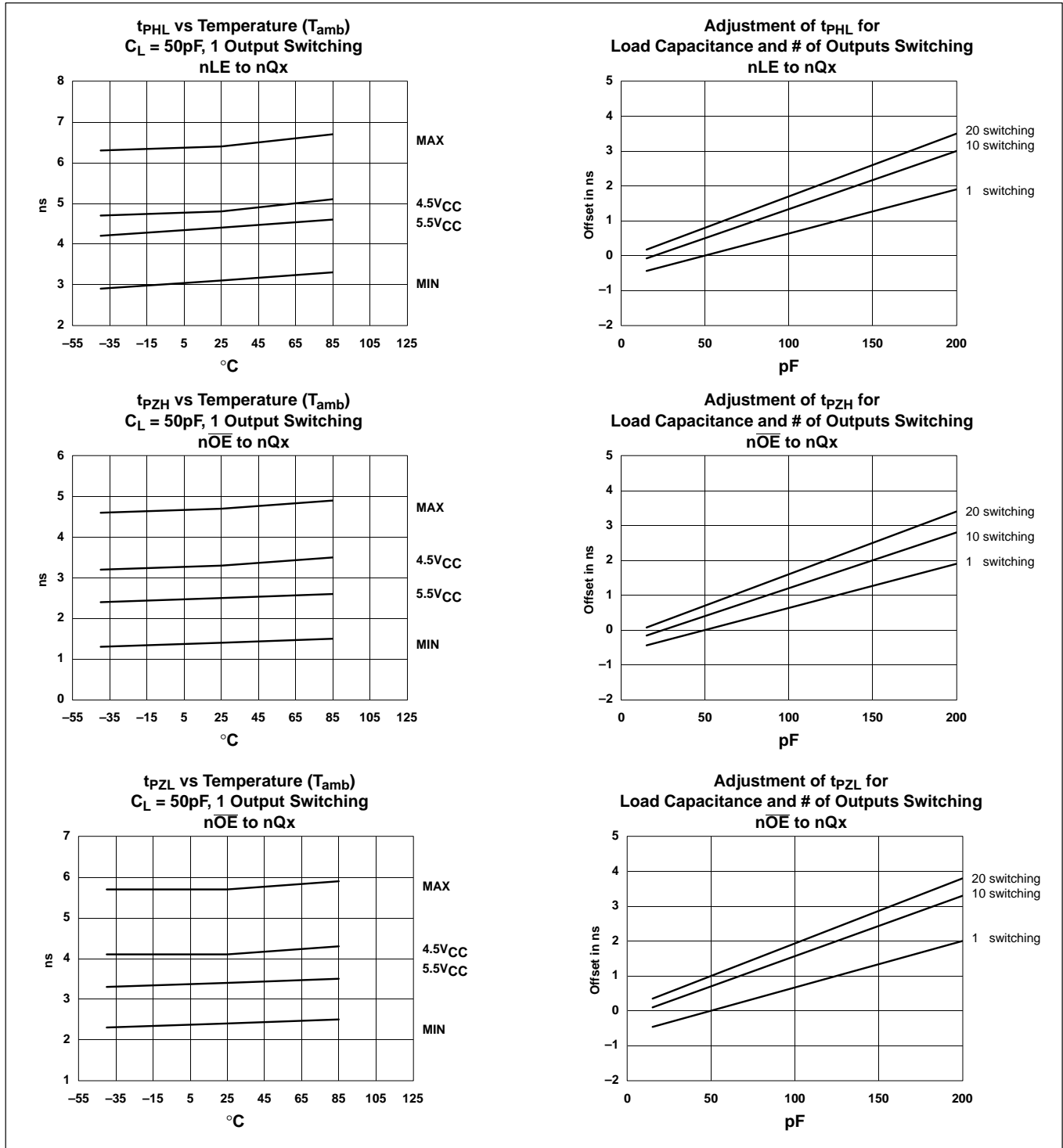
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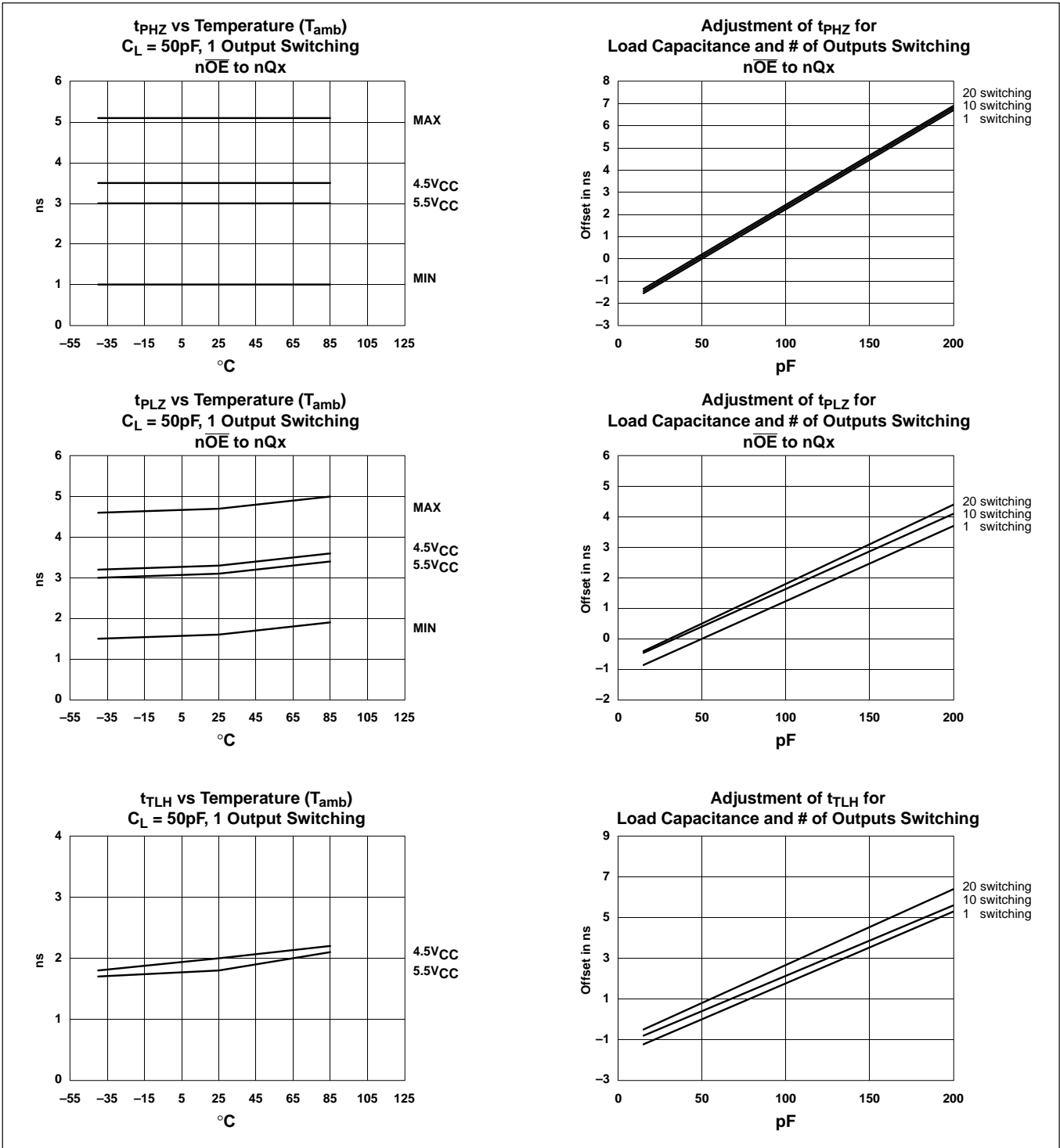
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