M39P0R9070E0

512 Mbit (x16, Multiple Bank, Multi-Level, Burst) Flash Memory 128 Mbit Low Power SDRAM, 1.8V Supply, Multi-Chip Package

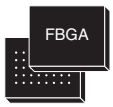
PRELIMINARY DATA

Features summary

- Multi-chip package
  - 1die of 512 Mbit (32Mb x 16, Multiple Bank, Multi-Level, Burst) Flash memory
  - 1 die of 128 Mbit (4 Banks of 2Mb x16) Low Power Synchronous Dynamic RAM
- Supply voltage
  - $V_{DDF} = V_{CCP} = V_{DDQ} = 1.7$ to 1.95V
  - $V_{PPF} = 9V$ for fast program (12V tolerant)
- Electronic signature
  - Manufacturer Code: 20h
  - Device Code: 8819
- Package
  - ECOPACK® (RoHS compliant)

Flash memory

- Synchronous / asynchronous read
  - Synchronous Burst Read mode: 108MHz, 66MHz
  - Asynchronous Page Read mode
  - Random Access: 93ns
- Programming time
  - 4µs typical Word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple Bank Memory Array: 64 Mbit Banks
  - Four Extended Flash Array (EFA) Blocks of 64 Kbits
- Dual operations
  - program/erase in one Bank while read in others
  - No delay between read and write operations
- Security
  - 64-bit unique device number
  - 2112-bit user programmable OTP Cells



TFBGA105 (ZAD)
9 x 11mm

- 100,000 program/erase cycles per block
- Block locking
  - All Blocks locked at power-up
  - Any combination of Blocks can be locked with zero latency
  - $\overline{WP}_F$ for Block Lock-Down
  - Absolute Write Protection with $V_{PPF} = V_{SS}$
- Common Flash Interface (CFI)

LPSDRAM

- 128Mbit synchronous dynamic RAM
  - Organized as 4 Banks of 2 MWords, each 16 bits wide
- Synchronous burst read and write
  - Fixed Burst Lengths: 1, 2, 4, 8 words or Full Page
  - Burst Types: Sequential and Interleaved.
  - Maximum Clock Frequency: 104MHz
  - $\overline{CAS}$ Latency 2, 3
- Automatic precharge
- Low power features:
  - PASR (Partial Array Self Refresh),
  - Automatic TCSR (Temperature Compensated Self Refresh)
  - Driver Strength (DS)
  - Deep Power-Down Mode
- Auto Refresh and Self Refresh

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1 Summary description

The M39P0R9070E0 combines two memory devices in one Multi-Chip Package:

- 512-Mbit Multiple Bank Flash memory (the M58PR512J)
- 128-Mbit Low Power Synchronous DRAM (the M65KA128AL)

This datasheet should be read in conjunction with the M58PR512J and M65KA128AL datasheets, available from *www.st.com*.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA105 package. It is supplied with all the bits erased (set to '1').

Figure 1. Logic Diagram

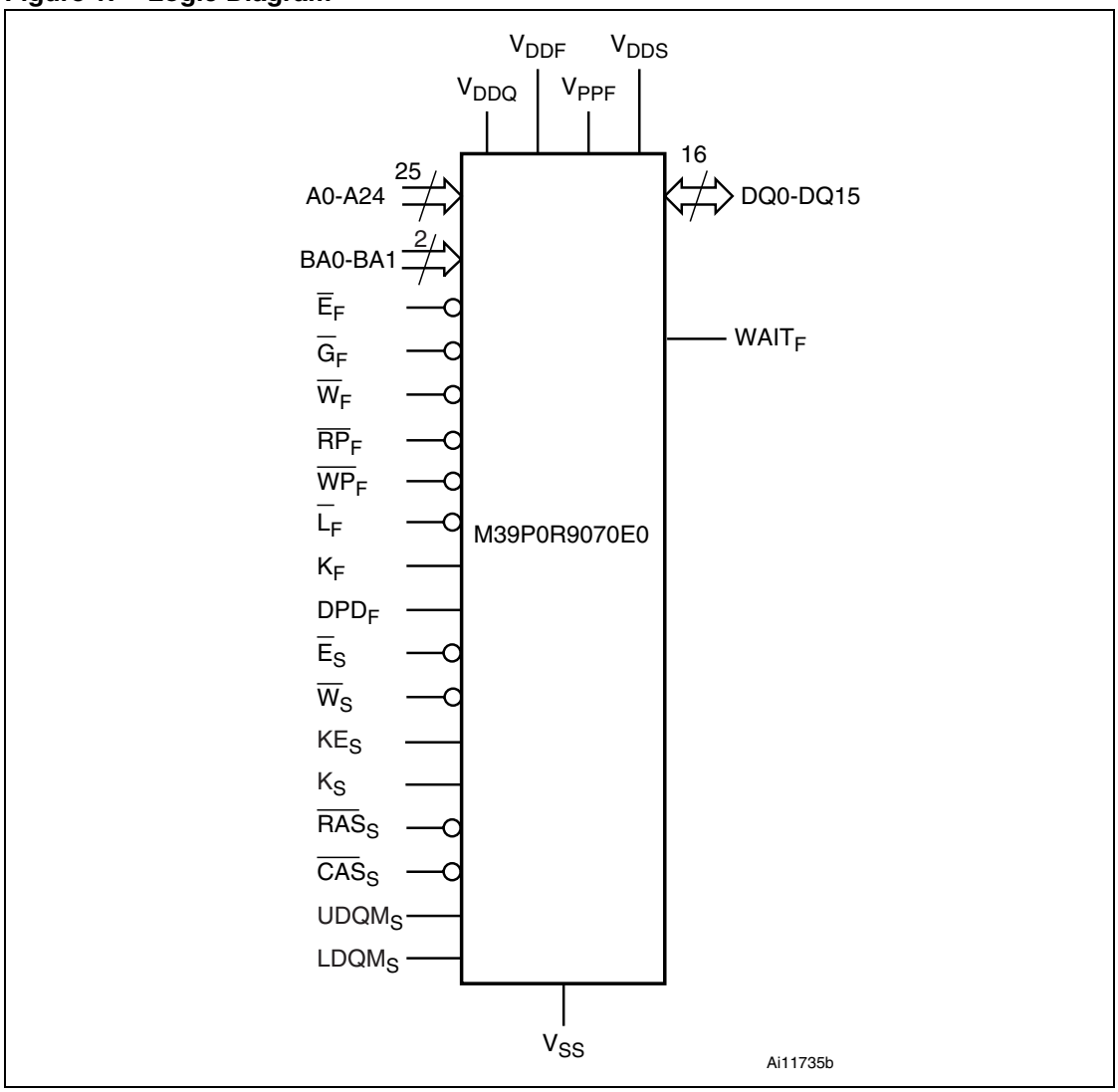
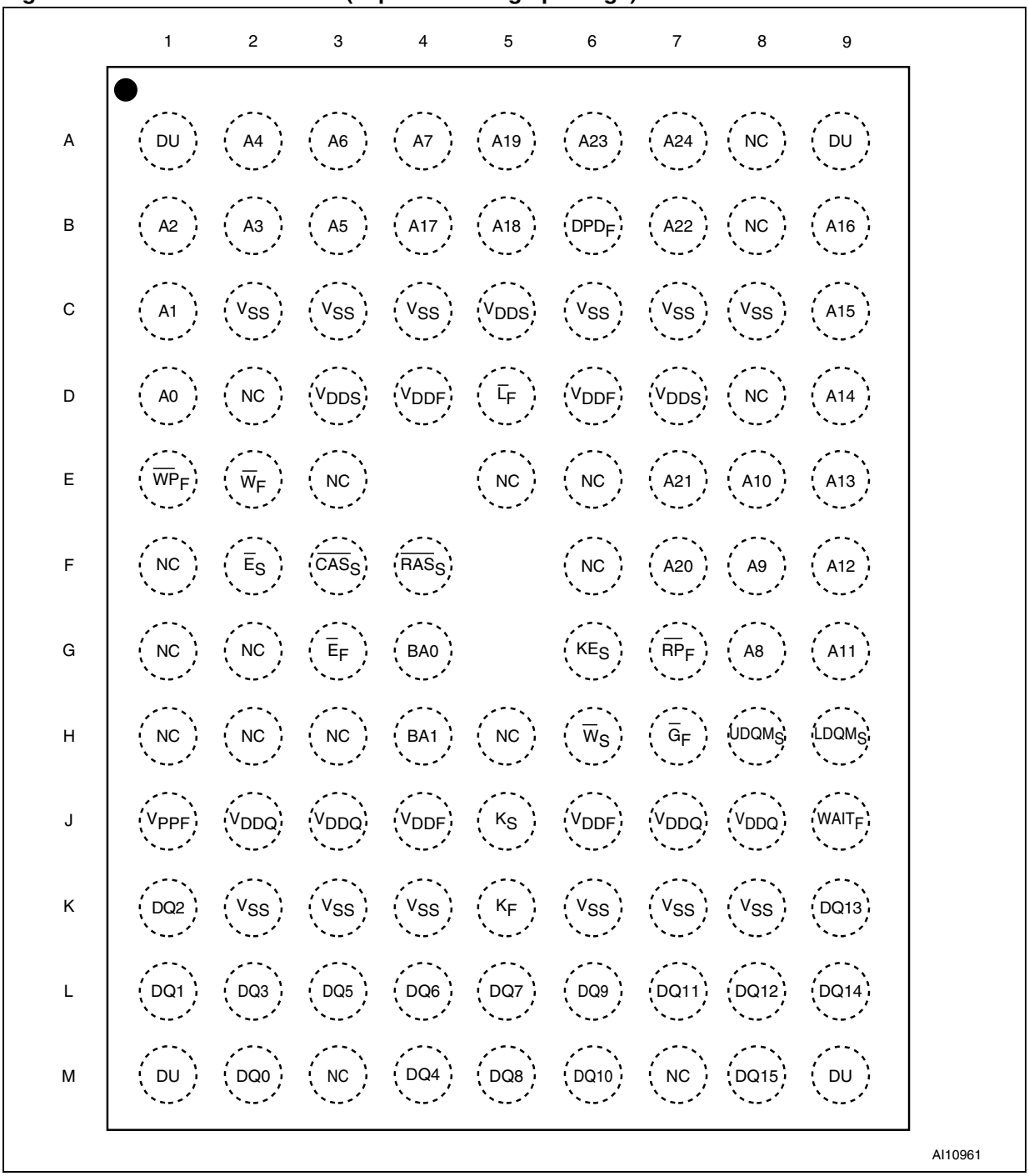


Table 1. Signal Names

A0-A24[1]	Address Inputs
DQ0-DQ15	Common Data Input/Output
V_{DDQ}	Common Flash and LPSDRAM Power Supply for I/O Buffers
V_{PPF}	Flash Memory Optional Supply Voltage for Fast Program & Erase
V_{DDF}	Flash Memory Power Supply
V_{DDS}	LPSDRAM Power Supply
V_{SS}	Ground
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash Memory	
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable Input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
$\overline{L}_F$	Latch Enable input
K_F	Burst Clock
$WAIT_F$	Wait Output
DPD_F	Deep Power-Down
Low Power SDRAM	
$\overline{E}_S$	Chip Enable Input
$\overline{W}_S$	Write Enable input
K_S	LPSDRAM Clock input
KE_S	LPSDRAM Clock Enable input
$\overline{CAS}_S$	Column Address Strobe Input
$\overline{RAS}_S$	Row Address Strobe Input
BA0, BA1	Bank Select Inputs
$UDQM_S$	Upper Data Input/Output Mask
$LDQM_S$	Lower Data Input/Output Mask

Note: 1 A12-A24 are Address Inputs for the Flash memory component only.

Figure 2. TFBGA Connections (Top view through package)



2 Signal descriptions

See *Figure 1., Logic Diagram* and *Table 1., Signal Names*, for a brief overview of the signals connect-ed to this device.

2.1 Address inputs (A0-A24)

A0-A11 are common to the Flash memory and LPSDRAM components. A12-A24 are Address Inputs for the Flash memory component only. In the Flash memory, the Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller. In the LPSDRAM, the A0-A11 Address Inputs are used to select the row or column to be made active. If a row is selected, all A0-A11 Address Inputs are used. If a column is selected, only the nine least significant Address Inputs, A0-A8, are used. In this latter case, A10 determines whether Auto Precharge is used. If A10 is High (set to '1') during Read or Write, the Read or Write operation includes an Auto Precharge cycle. If A10 is Low (set to '0') during Read or Write, the Read or Write cycle does not include an Auto Precharge cycle.

2.2 LPSDRAM Bank Select Address Inputs (BA0-BA1)

The BA0 and BA1 Bank Select Address Inputs are used by the LPSDRAM to select the bank to be made active. The LPSDRAM must be enabled, the Row Address Strobe, RAS_S, must be Low, V_{IL}, the Column Address Strobe, CAS_S, and W must be High, V_{IH}, when selecting the addresses. The address inputs are latched on the rising edge of the clock signal, K_S.

2.3 Data Inputs/Outputs (DQ0-DQ15)

In the Flash memory, the Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation. In the LPSDRAM, the Data Inputs/Outputs are common to all memory components. They output the data stored at the selected address during a Read operation, or are used to input the data during a write operation.

2.4 Flash Memory Chip Enable Input ($\overline{E}_F$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level. It is not allowed to have E_F and E_S all at V_{IL} at the same time, only one memory component should be enabled at a time.

2.5 Flash Memory Output Enable ($\overline{G}_F$)

The Output Enable input controls data outputs during the Bus Read operation of the memory.

2.6 Flash Memory Write Enable ($\overline{W}_F$)

The Write Enable input controls the Bus Write operation of the Flash memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.7 Flash Memory Write Protect Input ($\overline{WP}_F$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at V_{IH}, the Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See M58PR512J datasheet for details).

2.8 Flash Memory Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the memory. When

Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current

I_{DD2}. Refer to *Table 6., Flash Memory DC Characteristics - Currents*, for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs. The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to *Table 7., Flash Memory DC Characteristics - Voltages*).

2.9 Deep Power-Down (DPD_F)

The Deep Power-Down input is used to put the Flash memory in Deep Power-Down mode.

When the Flash memory is in Standby mode and the Enhanced Configuration Register bit ECR15 is set, asserting the Deep Power-Down input will cause the memory to enter the Deep Power-Down mode.

When the device is in the Deep Power-Down mode, the memory cannot be modified and the data is protected.

The polarity of the DPD_F pin is determined by ECR14. The Deep Power-Down input is active Low by default.

2.10 Flash Memory Latch Enable ($\overline{L}_F$)

The Latch Enable input latches the address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH}. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

2.11 Flash Memory Clock (K_F)

The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is ignored during asynchronous read and in write operations.

2.12 Flash Memory Wait ($WAIT_F$)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH}, Output Enable is at V_{IH}, or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one data cycle in advance.

2.13 LPSDRAM Chip Select ($\overline{E}_S$)

The Chip Select input Es activates the LPSDRAM state machine, address buffers and decoders when driven Low, V_{IL}. When High, V_{IH}, the device is not selected.

2.14 LPSDRAM Column Address Strobe ($\overline{CAS}_S$)

The Column Address Strobe, CAS_S, is used in conjunction with Address Inputs A8-A0 and BA1-BA0, to select the starting column location prior to a Read or Write.

2.15 LPSDRAM Row Address Strobe ($\overline{RAS}_S$)

The Row Address Strobe, RAS_S, is used in conjunction with Address Inputs A11-A0 and BA1-BA0, to select the starting address location prior to a Read or Write.

2.16 LPSDRAM Write Enable ($\overline{W}_S$)

The Write Enable input, $\overline{W}_S$, controls writing to the LPSDRAM.

2.17 LPSDRAM Clock Input (K_S)

The Clock signal, K_S, is used to clock the Read and Write cycles. During normal operation, the Clock Enable pin, KEs, is High, V_{IH}. The clock signal K_S can be suspended to switch the device to the Self Refresh, Power-Down or Deep Power-Down mode by driving KE_S Low, V_{IL}.

2.18 LPSDRAM Clock Enable (KE_S)

The Clock Enable, KE_S, pin is used to control the synchronizing of the signals to Clock signal K_S. The signals are clocked when KE_S is High, V_{IH} When KE_S is Low, V_{IL}, the signals are no longer clocked and data Read and Write cycles are extended. KE_S is also involved in switching the device to the Self Refresh, Power-Down and Deep Power-Down modes.

2.19 LPSDRAM Lower/Upper Data Input/Output Mask ($LDQM_S$/ $UDQM_S$)

Lower Data Input/Output Mask and Upper Data Input/Output Mask pins are input signals used to mask the Read or Write data.

2.20 Flash Memory V_{DDF} Supply Voltage

V_{DDF} provides the power supply to the internal core of the Flash memory component. It is the main power supply for all operations (Read, Program and Erase).

2.21 LPSDRAM V_{DDS} Supply Voltage

V_{DDS} provides the power supply to the internal core of the LPSDRAM component. It is the main power supply for all operations (Read and Write).

2.22 V_{DDQ} Supply Voltage

V_{DDQ} is common to the Flash memory and LPSDRAM memory components. It provides the power supply to the I/O pins and enables all Outputs to be powered independently of V_{DDF} for the Flash memory, or V_{DDS} for the LPSDRAM. V_{DDQ} can be tied to V_{DDF} or V_{DDS}, or can use a separate supply.

2.23 Flash Memory V_{PPF} Program Supply Voltage

V_{PPF} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin. If V_{PP} is kept in a low voltage range (0V to V_{DDQ}) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PP} > V_{PP1}$ enables these functions (see Tables 6 and 7, DC Characteristics for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue. If V_{PP} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed.

2.24 V_{SS} Ground

V_{SS} ground is common to the LPSDRAM and Flash memory components. It is the reference for the core supply. It must be connected to the system ground.

Note: Each device in a system should have V_{DDF} V_{DDS}, V_{DDQ} and V_{PPH} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 5., AC Measurement Load Circuit The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The LPSDRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for Flash and $\overline{E}_S$ for the LPSDRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is a simultaneous read operations on the Flash memory and the LPSDRAM which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 3. Functional Block Diagram

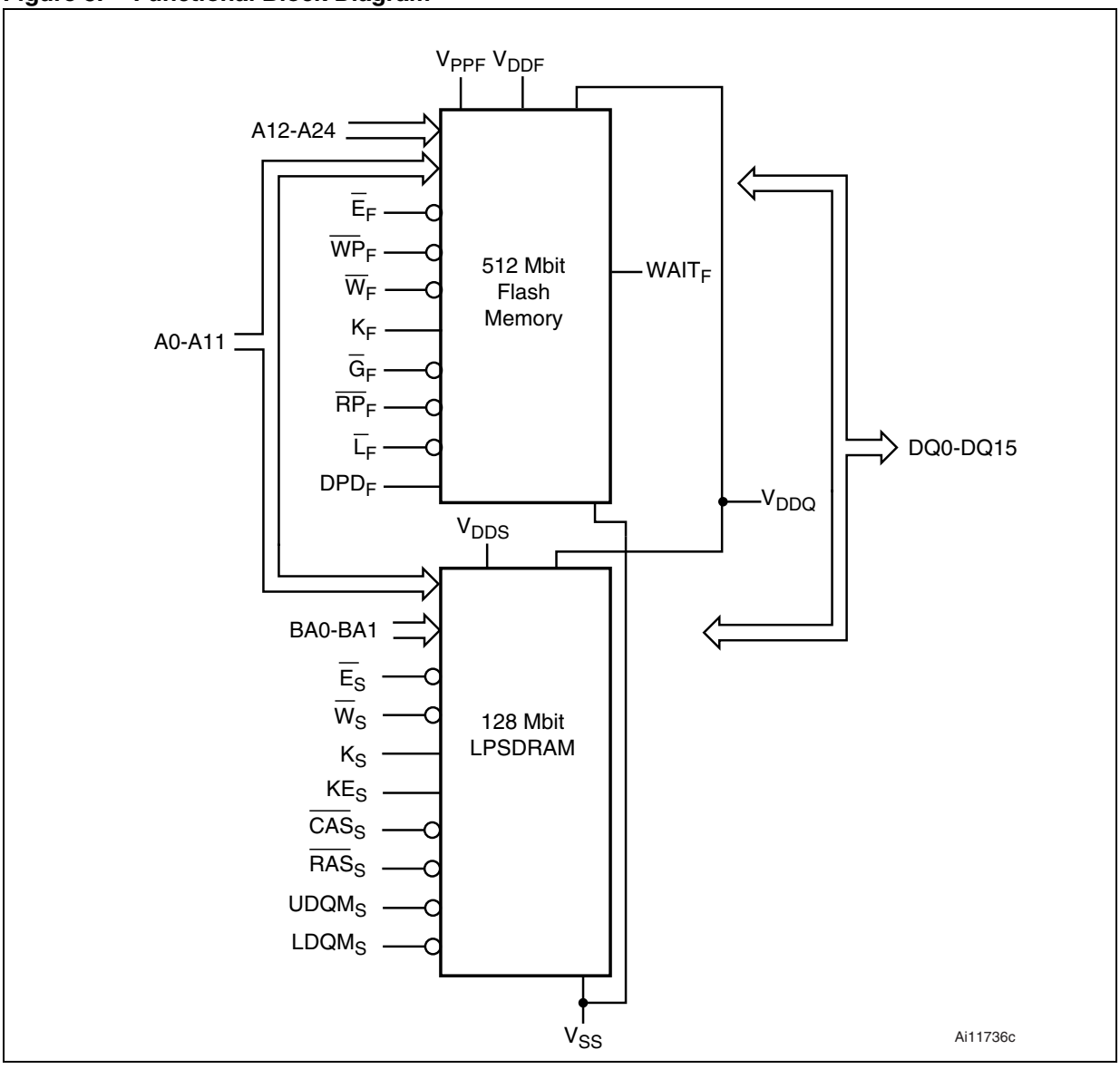


Table 2. Bus Operations

	Operation[1]	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{L}_F$	$\overline{RP}_F$	$WAIT_F$[2]	KE_Sn-1	KE_Sn	$\overline{E}_S$	$\overline{RAS}_S$	$\overline{CAS}_S$	$\overline{W}_S$	A10	A9, A11	A0-A7	BA0-BA1	DQ15-DQ0
Flash memory[3]	Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IL} (4)	V_{IH}				The SDRAM must be disabled.								Data Output
	Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IL} (4)	V_{IH}												Data Input
	Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}												Data Output or Hi-Z (5)
	Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	Hi-Z			Any SDRAM operation mode is allowed.								Hi-Z
	Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z											Hi-Z
	Reset	X	X	X	X	V_{IL}	Hi-Z											Hi-Z
	Deep Power-Down	V_{IH}	X	X	X	V_{IH}	Hi-Z											Hi-Z
LPSDRAM[3]	Burst Read	The Flash memory must be disabled.						V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V	SCA (6)	BS (7)	Data Output
	Burst Write							V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V	SCA (6)	BS (7)	Data Input
	Self Refresh							V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X			X	–
	Auto Refresh							V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	X			X	–
	Power-Up							V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X			X	–
	Power-Down	Any Flash memory operation mode is allowed.						V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X			X	–
										V_{IH}	X	X	X					
	Deep Power-Down							V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X			X	–
	Device Deselect							V_{IH}	X	V_{IH}	X	X	X	X			X	–
	No Operation							V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X			X	–

1. **X = Don't care, V = Valid.**
2. **$WAIT_F$ signal polarity is configured using the Set Configuration Register command.**
3. For further details, refer to the M58PR512J and M65KA128AL datasheets.
4. $\overline{L}_F$ can be tied to V_{IH} if the valid address has been previously latched.
5. Depends on $\overline{G}_F$
6. SCA = Start Column Address.
7. BS = Bank Select.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–25	85	°C
T_J	SDRAM Junction Temperature	–25	90	°C
T_{BIAS}	Temperature Under Bias	–25	85	°C
T_{STG}	Storage Temperature	–55	125	°C
V_{IO}	Input or Output Voltage	–0.5	2.6	V
V_{DDF}	Supply Voltage	–1.0	3.0	V
V_{DDS}	LPSDRAM Supply Voltage	–0.5	2.6	V
V_{DDQ}	Input/Output Supply Voltage	–0.5	2.6	V
V_{PPF}	Program Voltage	–1.0	12.6	V
I_O	Output Short Circuit Current		100	mA
t_{VPPH}	Time for V_{PP} at V_{PPH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 4., Operating and AC Measurement Conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter[1][2]	Flash memory		LPSDRAM			Unit
	Min	Max	Min	Typ	Max	
V_{DDF} Supply Voltage	1.7	1.95	–	–	–	V
V_{DDS} Supply Voltage	–	–	1.7	1.8	1.95	V
V_{DDQ} Supply Voltage[3]	1.7	1.95	1.7	1.8	1.95	V
V_{PPF} Supply Voltage (Factory environment)	8.5	9.5	–	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQ}+0.4	–	–	–	V
Ambient Operating Temperature	–25	85	–25	–	85	°C
Load Capacitance (C_L)	30		30			pF
Impedance Output (Z_0)	50					Ω
Output Circuit Protection Resistance (R)	50					Ω
Input Rise and Fall Times		3	1			ns
Input Pulse Voltages	0 to V_{DDQ}		–			V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		$V_{DDQ}/2$			V

1. All voltages are referenced to V_{SS} = 0V.
2. T_J = –25 to 90°C, f = 1MHz
3. V_{DDQ} must not exceed the level of V_{DDS}.

Figure 4. AC Measurement I/O Waveform

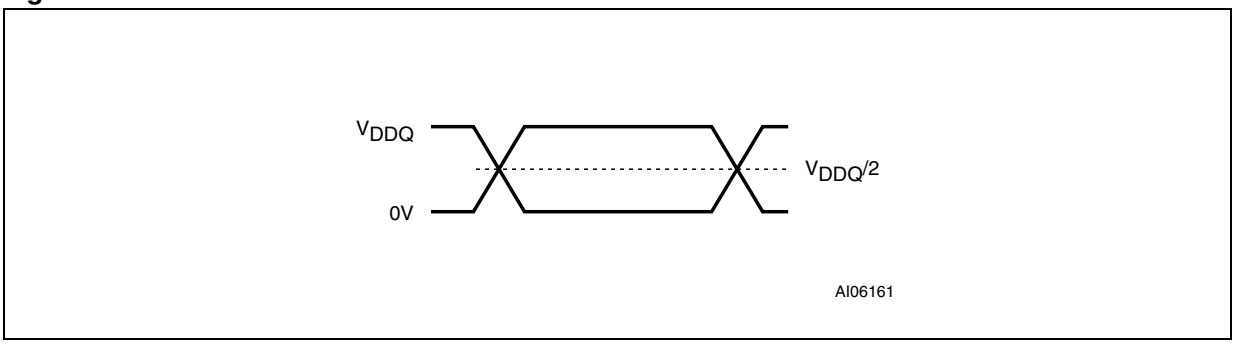


Figure 5. AC Measurement Load Circuit

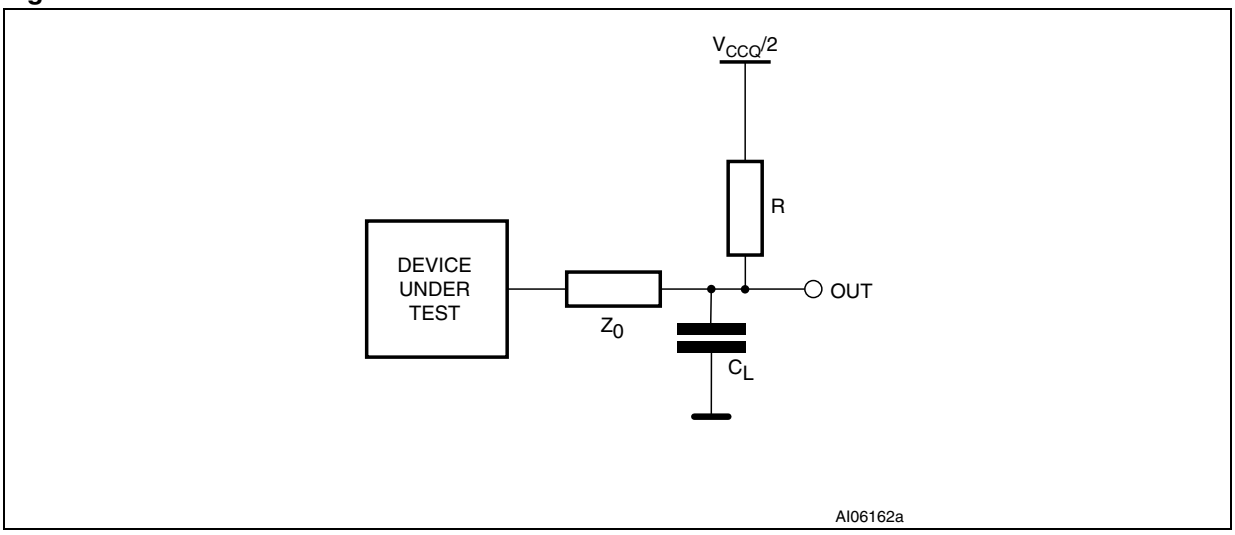


Table 5. Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	–	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	–	15	pF

1. Sampled only, not 100% tested.

Table 6. Flash Memory DC Characteristics - Currents

Symbol	Parameter	Test Condition		Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±1	µA
I_{DD1}	Supply Current Asynchronous Read (f=5MHz)	$\overline{E}_F = V_{IL}$, $\overline{G}_F = V_{IH}$		25	30	mA
	Supply Current Page Read (f=13MHz)			11	15	mA
	Supply Current Synchronous Read (f=66MHz)	8 Word		22	32	mA
		16 Word		19	26	mA
		Continuous		25	34	mA
	Supply Current Synchronous Read (f = 108MHz)	8 Word		26	36	mA
		16 Word		23	30	mA
		Continuous		30	42	mA
I_{DD2}	Supply Current (Reset)	$\overline{RP}_F = V_{SS} \pm 0.2V$	512 Mbit	50	120	µA
I_{DD3}	Supply Current (Standby)	$\overline{E}_F = V_{DDF} \pm 0.2V$	512 Mbit	50	120	µA
I_{DD4}	Supply Current (Automatic Standby)	$\overline{E}_F = V_{IL}$, $\overline{G}_F = V_{IH}$	512 Mbit	50	120	µA
I_{DD5} (1)	Supply Current (Deep Power Down)			2	30	µA
I_{DD6} (2)	Supply Current (Program)	$V_{PPF} = V_{PPH}$		35	50	mA
		$V_{PPF} = V_{DDF}$		35	50	mA
	Supply Current (Erase)	$V_{PPF} = V_{PPH}$		35	50	mA
		$V_{PPF} = V_{DDF}$		35	50	mA
	Supply Current (Blank Check)	$V_{PPF} = V_{PPH}$		35	50	mA
		$V_{PPF} = V_{DDF}$		35	50	mA
I_{DD7} (2)(3)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank		60	80	mA
		Program/Erase in one Bank, Synchronous Read (Continuous f=66MHz) in another Bank		65	92	mA
I_{DD8} (2)	Supply Current Program/ Erase Suspended (Standby)	$\overline{E}_F = V_{DDF} \pm 0.2V$	512 Mbit	50	120	µA
I_{PP1} (2)	V_{PPF} Supply Current (Program)	$V_{PPF} = V_{PPH}$		8	22	mA
		$V_{PPF} = V_{DDF}$		0.05	0.1	µA
	V_{PPF} Supply Current (Erase)	$V_{PPF} = V_{PPH}$		8	22	mA
		$V_{PPF} = V_{DD}$		0.05	0.1	µA
I_{PP2}	V_{PPF} Supply Current (Read)	$V_{PP} \le V_{DDF}$		2	15	µA
I_{PP3} (2)	V_{PPF} Supply Current (Standby, Program/Erase Suspend)	$V_{PP} \le V_{DDF}$		0.2	5	µA
I_{PP4}	V_{PPF} Supply Current (Blank Check)	$V_{PPF} = V_{PPH}$		0.05	0.1	mA
		$V_{PPF} = V_{PP1}$		0.05	0.1	mA

1. The DPD current is measured 40µs after entering the Deep Power Down mode.
2. Sampled only, not 100% tested.
3. V_{DDF} Dual Operation current is the sum of read and program or erase currents.

Table 7. Flash Memory DC Characteristics - Voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		0		0.4	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.1			V
V_{PP1}	V_{PPF} Program Voltage-Logic	Program, Erase	1.1	1.8	3.3	V
V_{PPH}	V_{PPF} Program Voltage Factory	Program, Erase	8.5	9.0	9.5	V
V_{PPLK}	Program or Erase Lockout				0.4	V
V_{LKO}	V_{DDF} Lock Voltage		1			V
V_{RPH}	$\overline{RP}_F$ pin Extended High Voltage				3.3	V
V_{LKOQ}	V_{DDQ} Lock Voltage		0.9			V

Table 8. LPSDRAM DC Characteristics 1

Symbol	Parameter	Test Condition(1)	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le 1.8V$	–1	1	µA
I_{LO}(2)	Output Leakage Current	$0V \le V_{OUT} \le 1.8V$	–1.5	1.5	µA
V_{IL}(3)	Input Low Voltage	V_{IN} = 0V	–0.3(4)	0.3	V
V_{IH}(3)	Input High Voltage	V_{IN} = 0V	$0.8V_{DDQ}$	V_{DDQ} + 0.3(5)	V
V_{OL}	Output Low Voltage	I_{OUT} = 100µA, V_{IN} = 0V		0.2	V
V_{OH}	Output High Voltage	I_{OUT} = –100µA, V_{IN} = 0V	V_{DDQ} –0.2		V

1. T_J = –25 to 90°C.
2. Data outputs are disabled.
3. V_{DDQ} must not exceed the level of V_{DDS}.
4. V_{IL} may undershoot to -1.0V for less that 5ns.
5. V_{IH} may overshoot to 2.6V for less that 5ns.

Table 9. LPSDRAM DC Characteristics 2

Symbol	Parameter	Test Condition(1)	Typ	Unit
I_{DD1}(2)	Operating Current	Burst length = 1, one bank active $t_{RC} \geq t_{RC}(min)$, I_{OL} = 0mA	36	mA
I_{DD2P}	Standby Current in Power-Down Mode	$KE_S \leq V_{IL}(max)$, t_{CK} = 15ns	0.6	mA
I_{DD2PS}		$KE_S \leq V_{IL}(max)$, $t_{CK} = \infty$ Input signal stable	0.5	
I_{DD2N}	Standby Current in Non Power-Down Mode	$KE_S \geq V_{IH}$ (min), $\overline{E}_S \geq V_{IH}$ (min), t_{CK} = 15ns Input signals are changed once in 30ns	3	mA
I_{DD2NS}		$KE_S \geq V_{IH}$ (min), $t_{CK} = \infty$ Input signals are stable	1	
I_{DD3P}	Active Standby Current in Power-Down Mode	$KE_S \leq V_{IL}(max)$, t_{CK} = 15ns	1	mA
I_{DD3PS}		$KE_S \leq V_{IL}(max)$, $t_{CK} = \infty$	0.8	
I_{DD3N}	Active Standby Current in Non Power-Down Mode	$KE_S \geq V_{IH}$ (min), $\overline{E}_S \geq V_{IH}$ (min), t_{CK} = 15ns Input signals are changed once in 30ns	15	mA
I_{DD3NS}		$KE_S \geq V_{IH}$ (min), $t_{CK} = \infty$ Input signals are stable	5	
I_{DD4}(2)	Burst Mode Current, CL=2	$t_{CK} \geq t_{CK}$ (min), I_{OL} = 0mA All banks active	35	mA
	Burst Mode Current, CL=3		52	mA
I_{DD5}(3), (4)	Auto Refresh Current, CL=2	$t_{RC1} \geq t_{RC1}(min)$	65	mA
	Auto Refresh Current, CL=3			
I_{DD6}	Self Refresh Current	$KE_S \leq 0.2V$	See M65KA128AL datasheet	µA
I_{DD7}	Standby Current in Deep Power-down Mode	See Deep Power-Down Entry AC Waveforms, and Deep Power-Down Exit AC Waveforms Figures in M65KA128AL datasheet.	10	µA

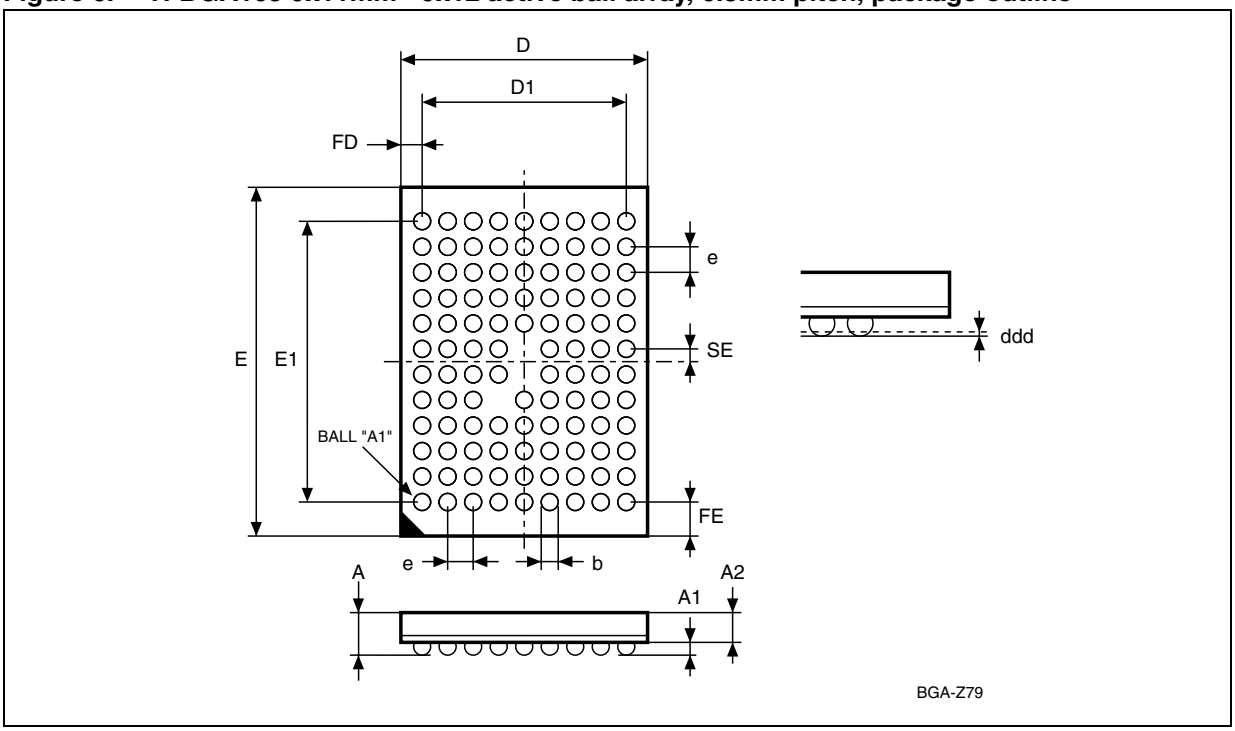
1. T_J = –25 to 90°C.
2. I_{DD1} and I_{DD4} depend on the output loading and cycle rates. All measurements are made with the output open and on condition that the addresses are changed only once during t_{CK} (min.).
3. The minimum value of t_{RC} ($\overline{RAS}_S$ cycle time for Refresh operation) is shown in the Asynchronous AC Characteristics Table in M65KA128AL datasheet.
4. I_{DD5} is measured on condition that the addresses are changed only once during t_{CK} (min.).

6 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 6. TFBGA105 9x11mm - 9x12 active ball array, 0.8mm pitch, package outline



Drawing is not to scale.

Table 10. TFBGA105 9x11mm - 9x12 active ball array, 0.8mm pitch, mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.20			0.008	
A2	0.80			0.031		
b	0.35	0.30	0.40	0.014	0.012	0.016
D	9.00	8.90	9.10	0.354	0.350	0.358
D1	6.40			0.252		
ddd			0.10			0.004
E	11.00	10.90	11.10	0.433	0.429	0.437
E1	8.80			0.346		
e	0.80	–	–	0.031	–	–
FD	1.30			0.051		
FE	1.10			0.043		
SE	0.40			0.016		

7 Part numbering

Table 11. Ordering Information Scheme

Example: M39 P 0 R 9 0 7 0 E 0 ZAD E

Device Type

M39 = Multi-Chip Package (Flash + LPSDRAM)

Flash 1 Architecture

P = Multi-Level, Multiple Bank, Large Buffer

Flash 2 Architecture

0 = No Die

Operating Voltage

R = V_{DDF} = V_{DDS} = V_{DDQ} = 1.7 to 1.95V

Flash 1 Density

9 = 512 Mbits

Flash 2 Density

0 = No Die

RAM 1 Density

7 = 128 Mbit

RAM 0 Density

0 = No Die

Parameter Blocks Location

E = Even Block Flash Memory Configuration

Product Version

0 = 90nm Flash technology, 93ns speed; LPSDRAM

Package

ZAD= stacked TFBGA105 D stacked footprint.

Option

Blank = Standard Packing

E = ECOPACK® Package, Standard packing

F = ECOPACK® Package, Tape & Reel packing

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

8 Revision history

Date	Version	Revision Details
29-Nov-2005	1	Initial release.