

38C1 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 38C1 group is the 8-bit microcomputer based on the 740 family core technology.

The 38C1 group has the LCD drive control circuit, an 8-channel A-D converter, and serial I/O as additional functions.

The various microcomputers in the 38C1 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

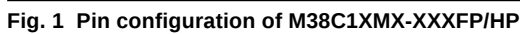
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time 0.5 μ s
(at 8 MHz oscillation frequency)
- Memory size
 - ROM 16 K to 24 K bytes
 - RAM 384 to 512 bytes
- Programmable input/output ports (Ports P2–P6) 30
- Segment output pin/Input port (Port P0) 8
- Software pull-up/pull-down resistor Ports P0, P2–P6
- Interrupts 13 sources, 13 vectors
(includes key input interrupt)
- Timers 8-bit $\times$ 3, 16-bit $\times$ 2
- Serial I/O 8-bit $\times$ 1 (Clock-synchronous)
- A-D converter 8-bit $\times$ 8 channels
(It can be used in the low-speed mode.)

- LCD drive control circuit
 - Bias 1/1, 1/2, 1/3
 - Duty Static, 1/2, 1/3, 1/4
 - Common output 4
 - Segment output 25
- Main clock generating circuit 1
(connect to external ceramic resonator or built-in ring oscillator)
- Sub clock generating circuit 1
(connect to external quartz-crystal oscillator)
- Power source voltage
 - In high-speed mode ($f(X_{IN}) \leq 8.0$ MHz) 4.0 to 5.5 V
 - In middle-speed mode (Mask ROM version: $f(X_{IN}) \leq 6.0$ MHz) 1.8 to 5.5 V
 - In middle-speed mode (One Time PROM version: $f(X_{IN}) \leq 6.0$ MHz) 2.2 to 5.5 V
 - In low-speed mode (Mask ROM version) 1.8 to 5.5 V
 - In low-speed mode (One Time PROM version) 2.2 to 5.5 V
- Power dissipation (Mask ROM version)
 - In high-speed mode (frequency divided by 2) Typ. 15 mW
($V_{CC} = 5$ V, $f(X_{IN}) = 8$ MHz, $T_a = 25$ °C)
 - In low-speed mode Typ. 18 μ W
($V_{CC} = 2.5$ V, $f(X_{IN}) = \text{stop}$, $f(X_{CIN}) = 32$ kHz, $T_a = 25$ °C)
- Operating temperature range – 20 to 85°C

APPLICATIONS

Household appliances, consumer electronics, etc.



FUNCTIONAL BLOCK DIAGRAM

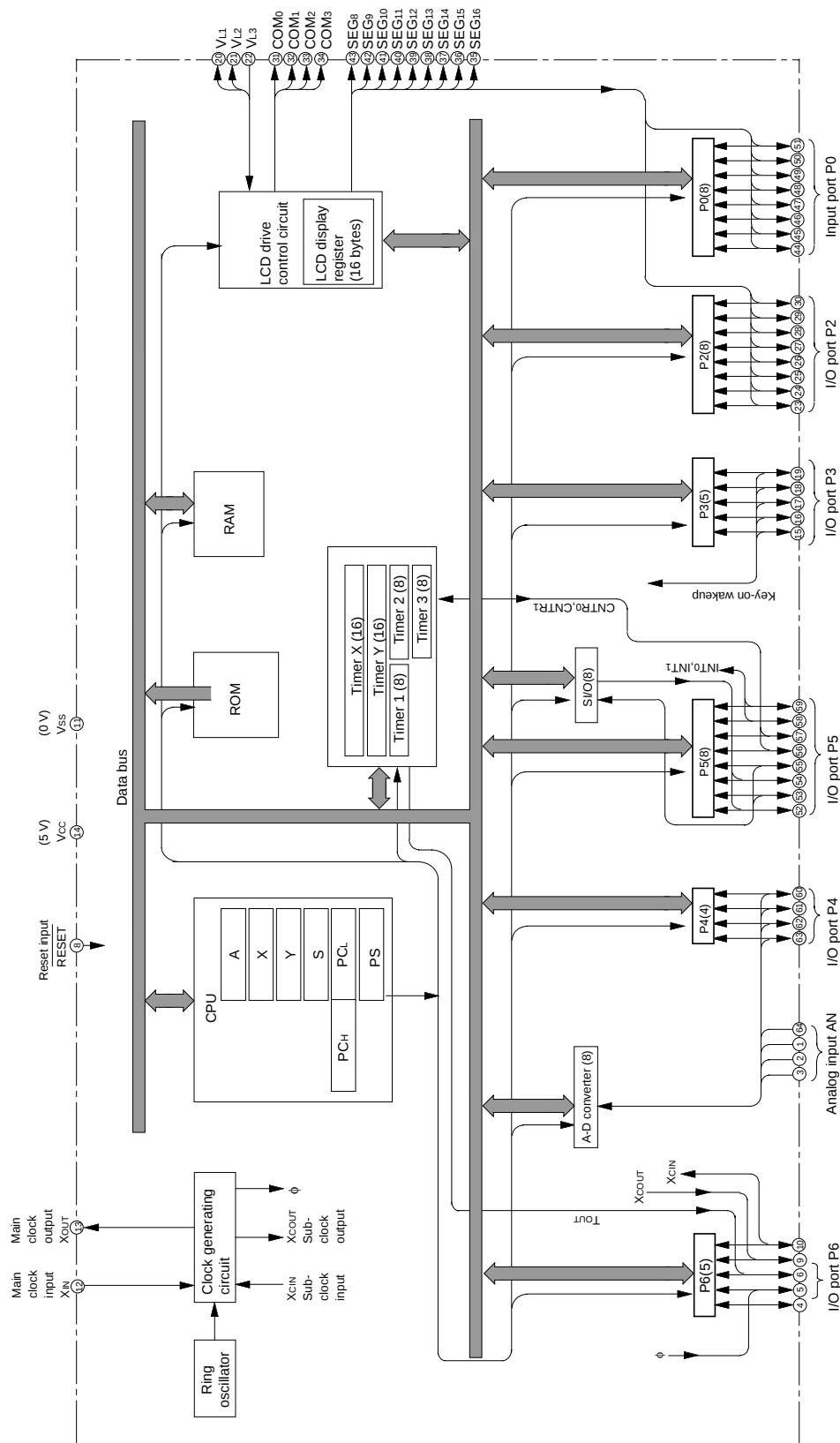


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description

Pin	Name	Function	
			Function except a port function
Vcc, Vss	Power source	Apply voltage of power source to Vcc, and 0 V to Vss. (As for Vcc, refer to the recommended operating condition)	
CNVss	CNVss	Connect to Vss.	
RESET	Reset input	Reset input pin for active "L".	
XIN	Clock input	- Input and output pins for the main clock generating circuit. - Connect a ceramic resonator or a quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. - If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. A feedback resistor is built-in.	
XOUT	Clock output		
VL1–VL3	LCD power source	Input $0 \leq VL1 \leq VL2 < VL3$ voltage.	
COM0–COM3	Common output	LCD common output pins.	
P00/SEG0– P07/SEG7	Input port P0	8-bit input port. - CMOS compatible input level. 1, 2, 4 or 8-bit input and 8-bit pull-down can be programmed.	LCD segment output pins
SEG8–/SEG16	Segment output pin	LCD segment output pin.	
P20/SEG17– P27/SEG24	I/O port P2	8-bit I/O port. - CMOS compatible input level. - CMOS 3-state output structure. 1-bit input/output and pull-down can be programmed.	LCD segment output pins
P30(LED)/KW0– P34(LED)/KW4	I/O port P3	5-bit I/O port. - CMOS compatible input level. - CMOS 3-state output structure. 1-bit input/output and pull-up can be programmed.	Key input (key-on wake-up) interrupt input pins
AN0/ADKEY0– AN3/ADKEY3	Analog input	- Analog input pins for A-D converter. - When these pins are used as ADKEY pins, the input voltage of ADKEY pin which is input "L" level is A-D converted automatically.	ADKEY input pins
P44/AN4– P47/AN7	I/O port P4	4-bit I/O port. - CMOS compatible input level. - CMOS 3-state output structure. 1-bit input/output and pull-up can be programmed.	Analog input pins for A-D converter
P50/INT0, P51/INT1	I/O port P5	8-bit I/O port. - CMOS compatible input level. - CMOS 3-state output structure. 1-bit input/output and pull-up can be programmed.	Interrupt input pins
P52/CNTR0 P53/CNTR1			Timer X, timer Y function pins
P54/SIN P55/SOUT P56/SCLK P57/SRDY			Serial I/O function pins
P60/XCIN P61/XCOUT			Sub-clock generating circuit I/O pins (Oscillator is connected. External clock cannot be input directly.)
P62/TOUT	I/O port P6	5-bit I/O port. - CMOS compatible input level. - CMOS 3-state output structure. 1-bit input/output and pull-up can be programmed.	Timer 2 output pin
P63/φOUT			System clock φ output
P64			

PART NUMBERING

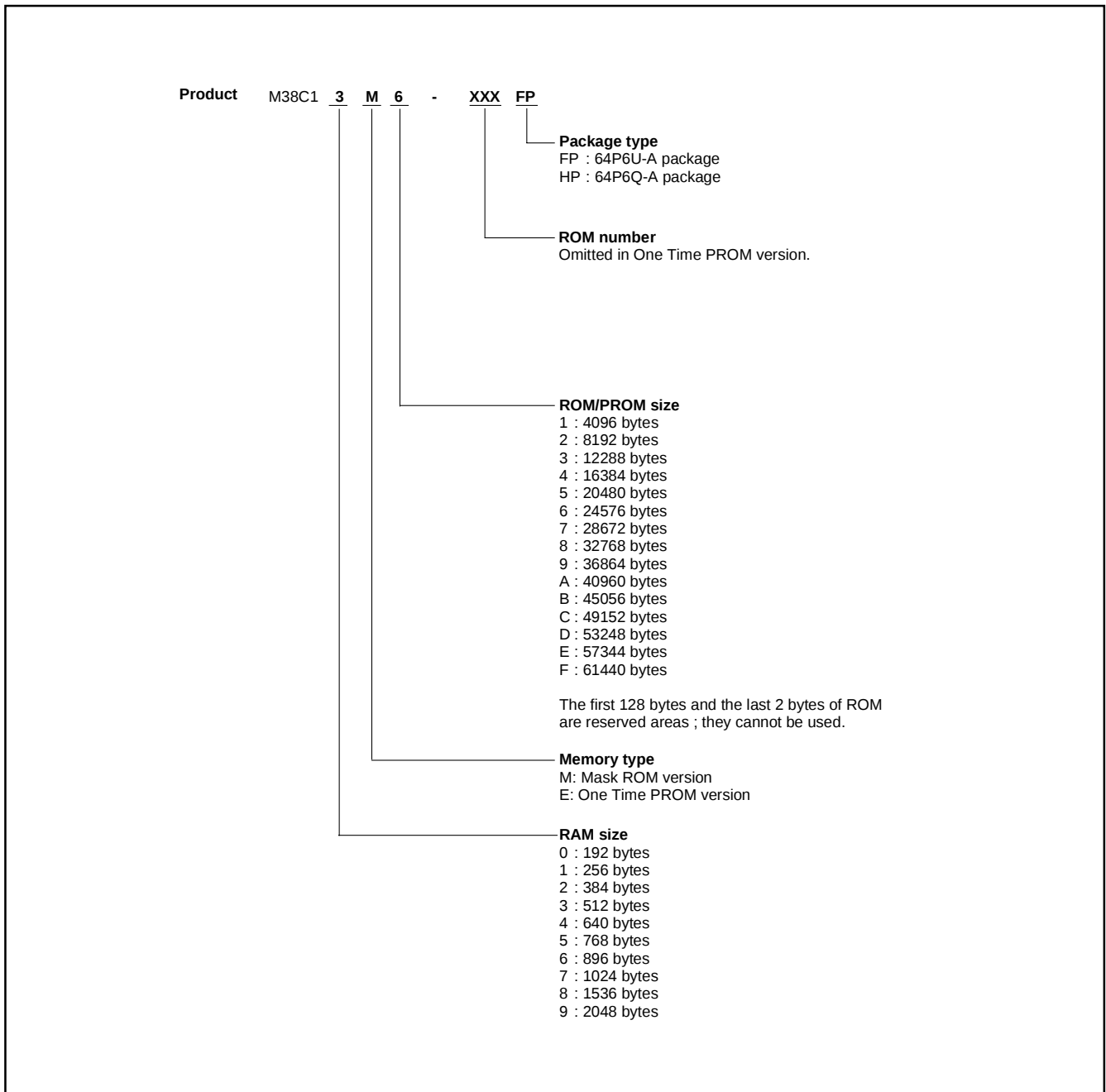


Fig. 3 Part numbering

38C1 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

GROUP EXPANSION

Mitsubishi plans to expand the 38C1 group as follows.

Memory Type

Support for Mask ROM version, One Time PROM version.

Memory Size

ROM/PROM size 16 K to 24 K bytes

RAM size 384 to 512 bytes

Packages

64P6Q-A 0.5 mm-pitch plastic molded QFP

64P6U-A 0.8 mm-pitch plastic molded QFP

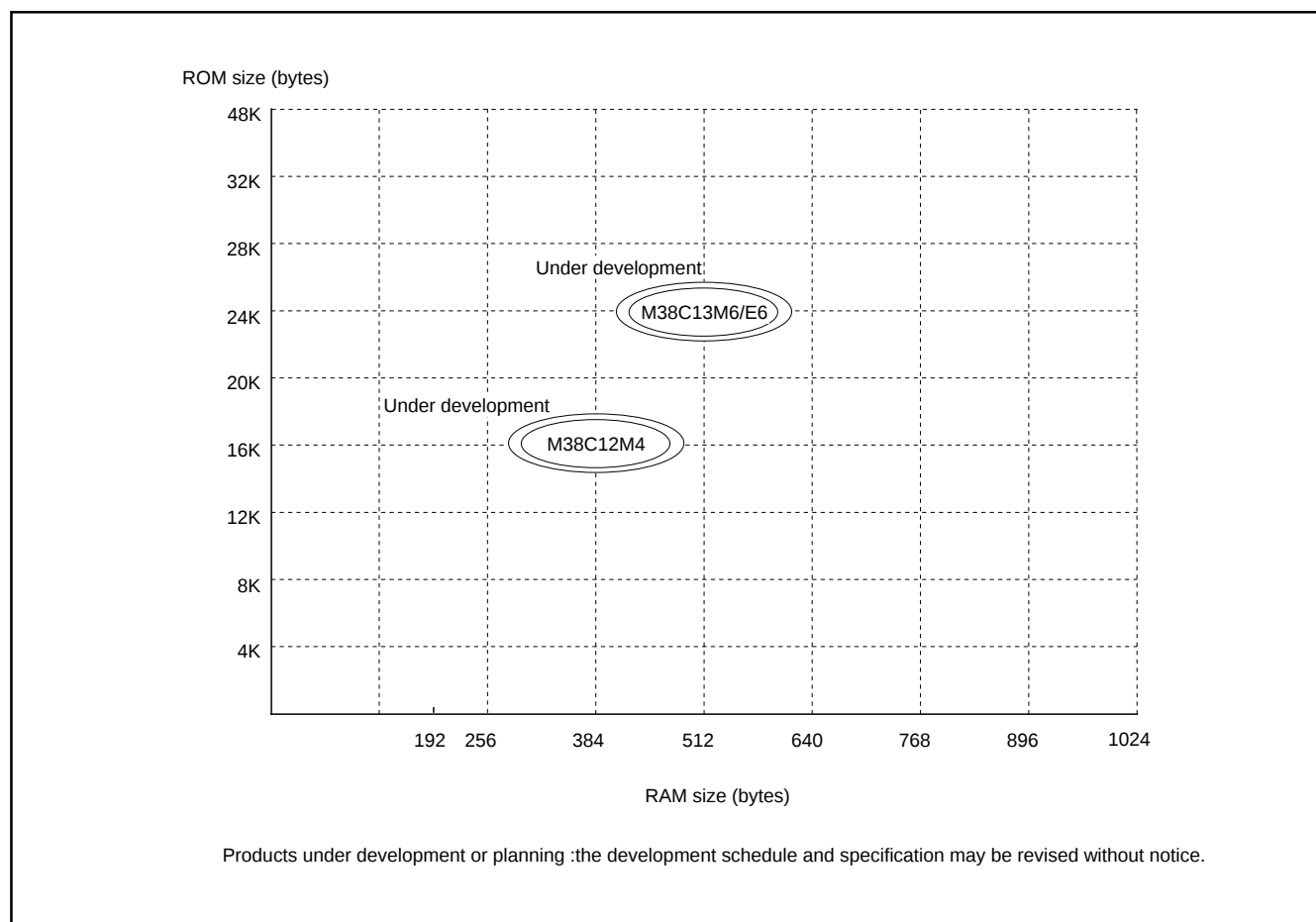


Fig. 4 Memory expansion plan

Currently products are listed below.

Table 2. List of products

As of May. 2002

Product	ROM size (bytes) ROM size for User in ()	RAM size (bytes)	Package	Remarks
M38C12M4-XXXXFP	16384 (16256)	384	64P6U-A	Mask ROM version
M38C12M4-XXXXHP			64P6Q-A	
M38C13M6-XXXXFP	24576 (24446)	512	64P6U-A	One Time PROM version (shipped in blank)
M38C13M6-XXXXHP			64P6Q-A	
M38C13E6FP			64P6U-A	
M38C13E6HP			64P6Q-A	

FUNCTIONAL DESCRIPTION

CENTRAL PROCESSING UNIT (CPU)

The 38C1 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "0116".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

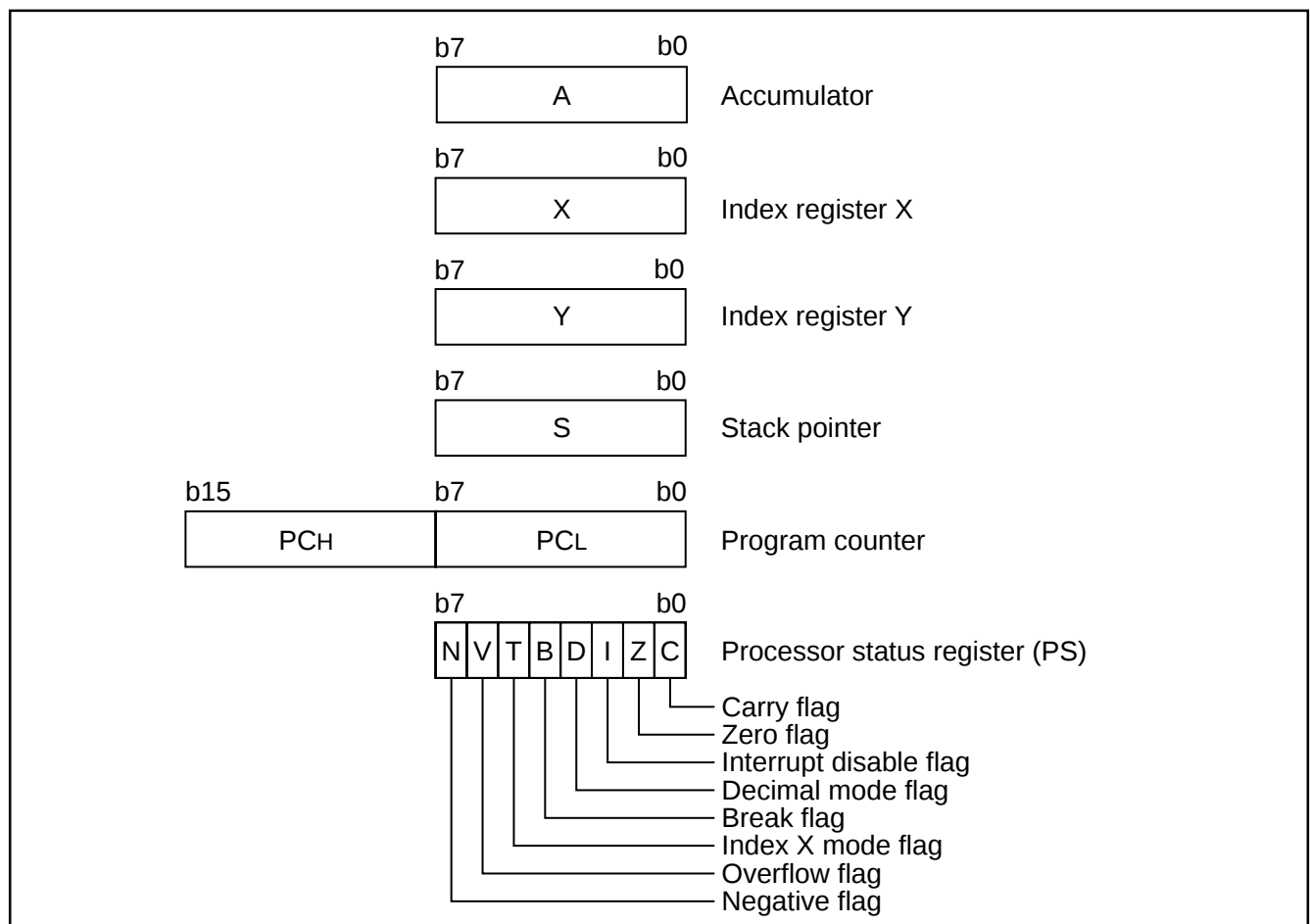


Fig. 5 740 Family CPU register structure

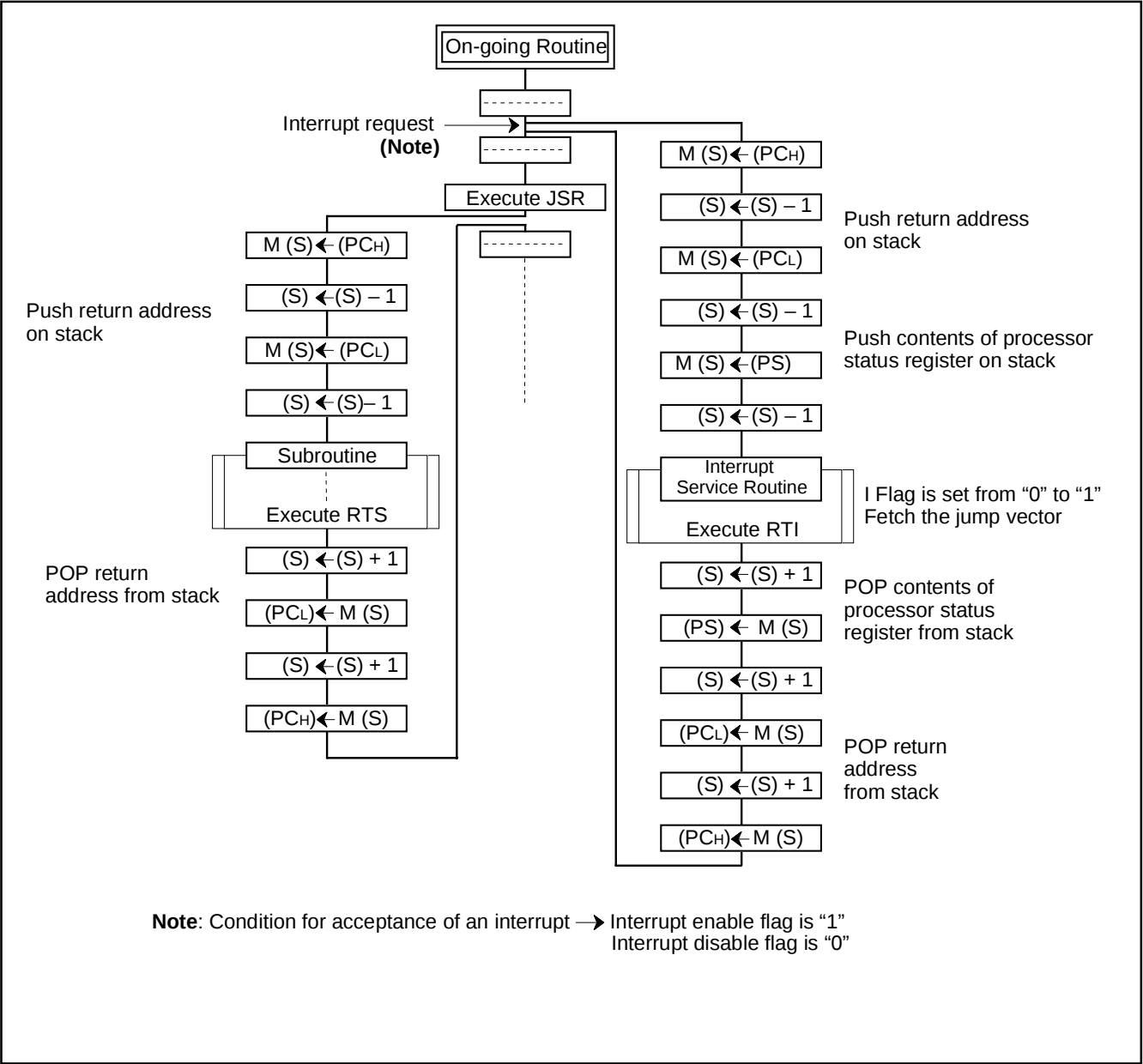


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

- Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

- Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

- Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

- Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

- Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

- Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

- Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	—	SEI	SED	—	SET	—	—
Clear instruction	CLC	—	CLI	CLD	—	CLT	CLV	—

[CPU Mode Register (CPUM)] 003B₁₆

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.

The CPU mode register is allocated at address 003B₁₆.

After system is released from reset, the ring oscillator mode is selected, and the X_{IN}–X_{OUT} oscillation and the X_{CIN}–X_{COU}T oscillation are stopped.

When the low-, middle- or high-speed mode is used after the X_{IN}–X_{OUT} oscillation and the X_{CIN}–X_{COU}T oscillation are enabled, wait in the ring oscillator mode until oscillation stabilizes, and then, switch the operation mode.

When the middle- and high-speed mode are not used (X_{IN}–X_{OUT} oscillation and external clock input are not performed), connect X_{IN} to V_{CC} through a resistor.

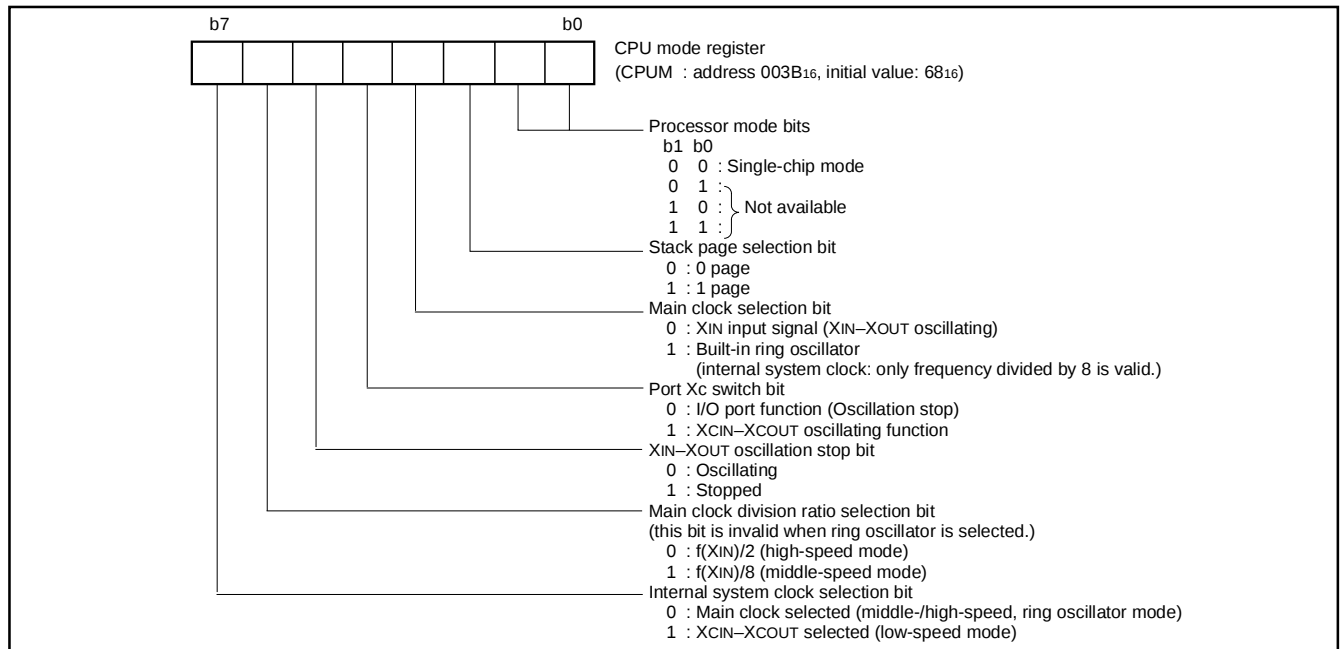


Fig. 7 Structure of CPU mode register

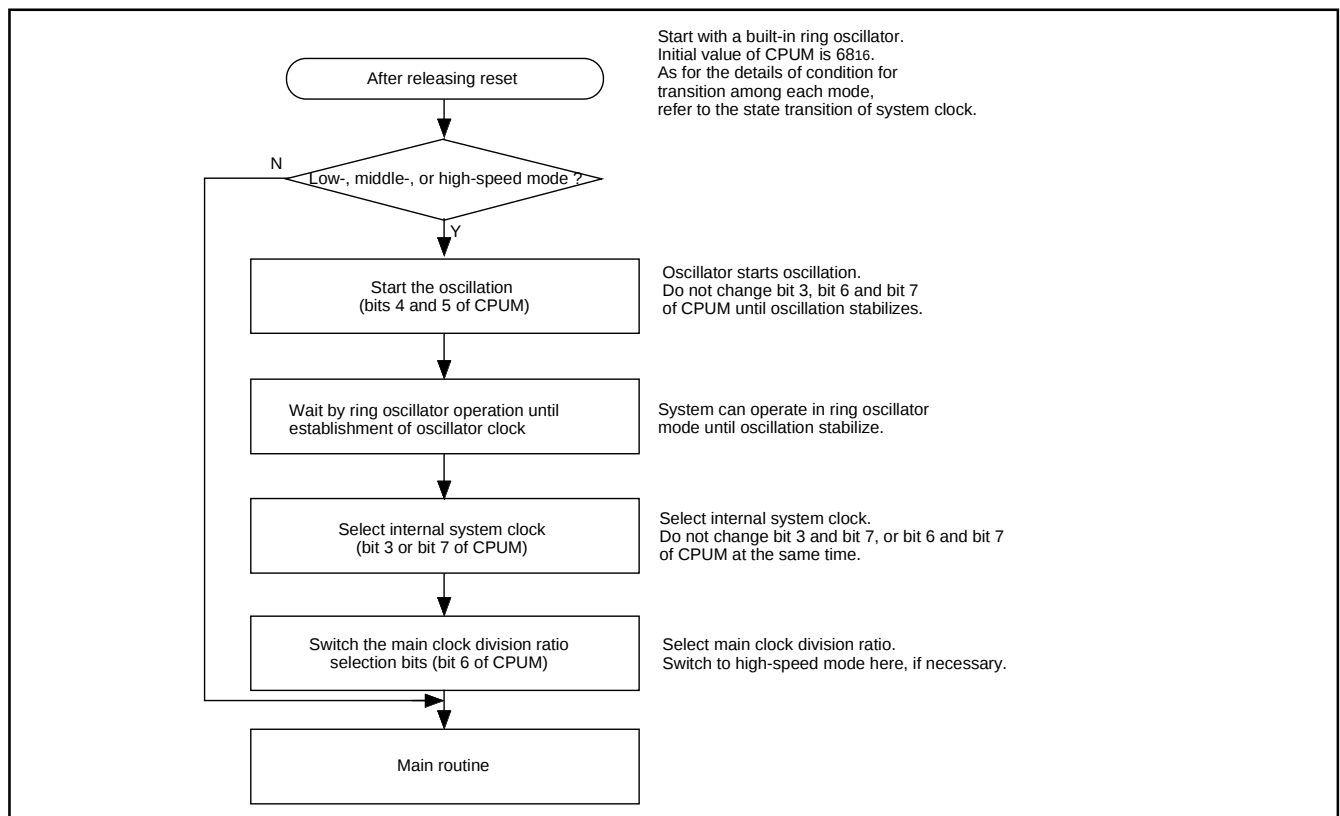


Fig. 8 Switching method of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000₁₆ to 00FF₁₆ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses FF00₁₆ to FFFF₁₆ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

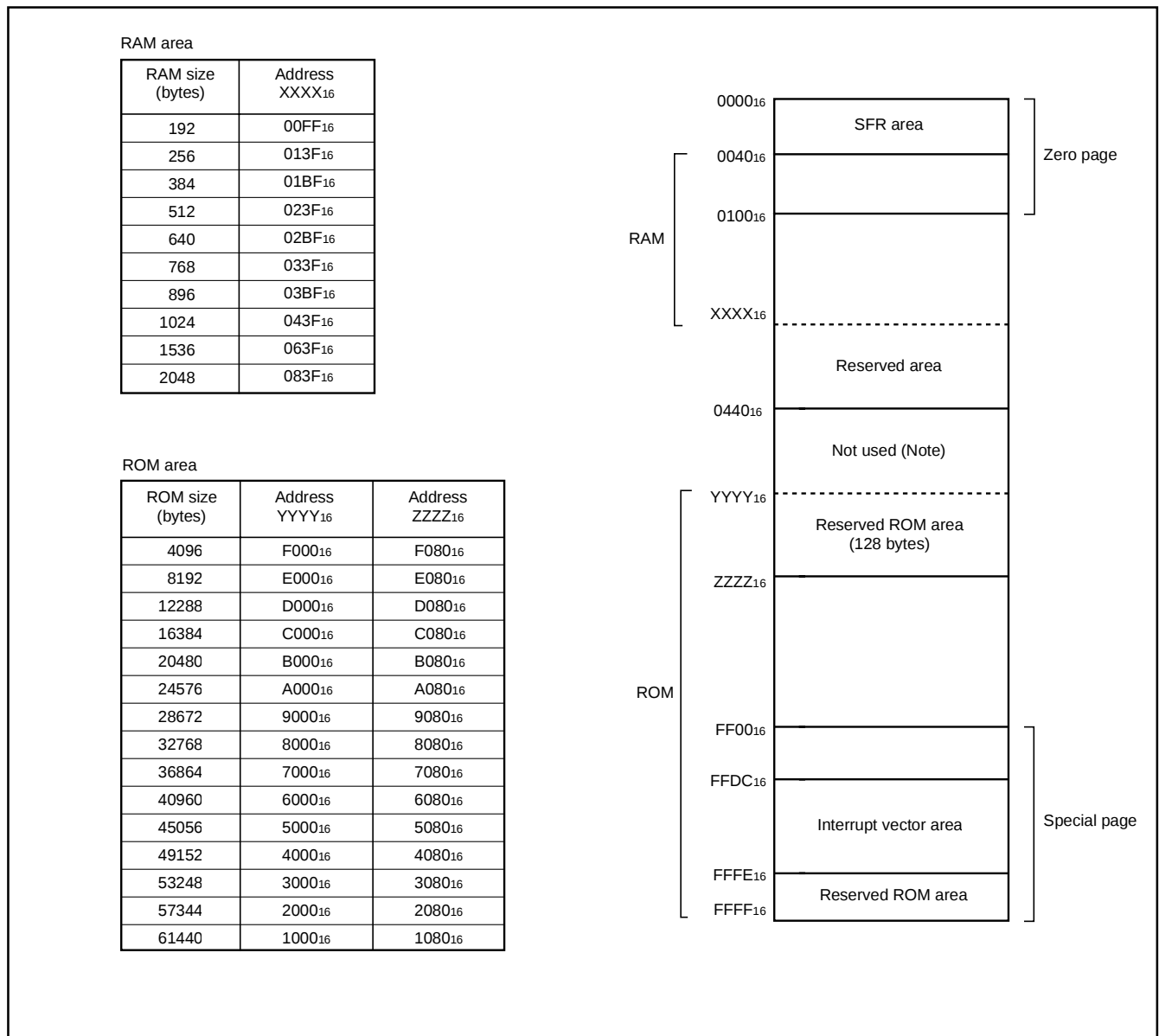


Fig. 9 Memory map diagram

0000 ₁₆	Port P0 (P0)	0020 ₁₆	Timer X (low) (TXL)
0001 ₁₆		0021 ₁₆	Timer X (high) (TXH)
0002 ₁₆		0022 ₁₆	Timer Y (low) (TYL)
0003 ₁₆		0023 ₁₆	Timer Y (high) (TYH)
0004 ₁₆	Port P2 (P2)	0024 ₁₆	Timer 1 (T1)
0005 ₁₆	Port P2 direction register (P2D)	0025 ₁₆	Timer 2 (T2)
0006 ₁₆	Port P3 (P3)	0026 ₁₆	Timer 3 (T3)
0007 ₁₆	Port P3 direction register (P3D)	0027 ₁₆	Timer X mode register (TXM)
0008 ₁₆	Port P4, ADKEY pin selection (P4)	0028 ₁₆	Timer Y mode register (TYM)
0009 ₁₆	Port P4 direction register (P4D)	0029 ₁₆	Timer 123 mode register (T123M)
000A ₁₆	Port P5 (P5)	002A ₁₆	φ output control register
000B ₁₆	Port P5 direction register (P5D)	002B ₁₆	
000C ₁₆	Port P6 (P6)	002C ₁₆	Temporary data register 1 (TD0)
000D ₁₆	Port P6 direction register (P6D)	002D ₁₆	Temporary data register 2 (TD1)
000E ₁₆		002E ₁₆	Temporary data register 3 (TD2)
000F ₁₆		002F ₁₆	RRF register (RRF)
0010 ₁₆	LCD display register 0(LCD0)	0030 ₁₆	
0011 ₁₆	LCD display register 1(LCD1)	0031 ₁₆	
0012 ₁₆	LCD display register 2(LCD2)	0032 ₁₆	
0013 ₁₆	LCD display register 3(LCD3)	0033 ₁₆	PULL register
0014 ₁₆	LCD display register 4(LCD4)	0034 ₁₆	A-D control register (ADCON)
0015 ₁₆	LCD display register 5(LCD5)	0035 ₁₆	A-D conversion register (AD)
0016 ₁₆	LCD display register 6(LCD6)	0036 ₁₆	
0017 ₁₆	LCD display register 7(LCD7)	0037 ₁₆	
0018 ₁₆	LCD display register 8(LCD8)	0038 ₁₆	Segment output enable register (SEG)
0019 ₁₆	LCD display register 9(LCD9)	0039 ₁₆	LCD mode register (LM)
001A ₁₆	LCD display register 10(LCD10)	003A ₁₆	Interrupt edge selection register (INTEDGE)
001B ₁₆	LCD display register 11(LCD11)	003B ₁₆	CPU mode register (CPUM)
001C ₁₆	LCD display register 12(LCD12)	003C ₁₆	Interrupt request register 1(IREQ1)
001D ₁₆	Serial I/O control register (SIOCON)	003D ₁₆	Interrupt request register 2(IREQ2)
001E ₁₆		003E ₁₆	Interrupt control register 1(ICON1)
001F ₁₆	Serial I/O register (SIO)	003F ₁₆	Interrupt control register 2(ICON2)

Fig. 10 Memory map of special function register (SFR)

I/O PORTS

Direction Registers (Ports P2–P6)

The I/O ports (P2–P6) have direction registers which determine the input/output direction of each individual pin.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pull-up/Pull-down Control

By setting the PULL register (address 0033₁₆), I/O ports can control pull-up/pull-down (pins also used as segment output pin: pull-down, other pins: pull-up). Pull-up/pull-down of pins are performed by setting the PULL register to “1”.

However, the contents of PULL register does not affect ports programmed as the output ports.

Input port P0 and I/O port P2 are pulled-down in the initial state.

Also, the pull-down setting is invalid for pins set to segment output with the segment output enable register (address 0038₁₆).

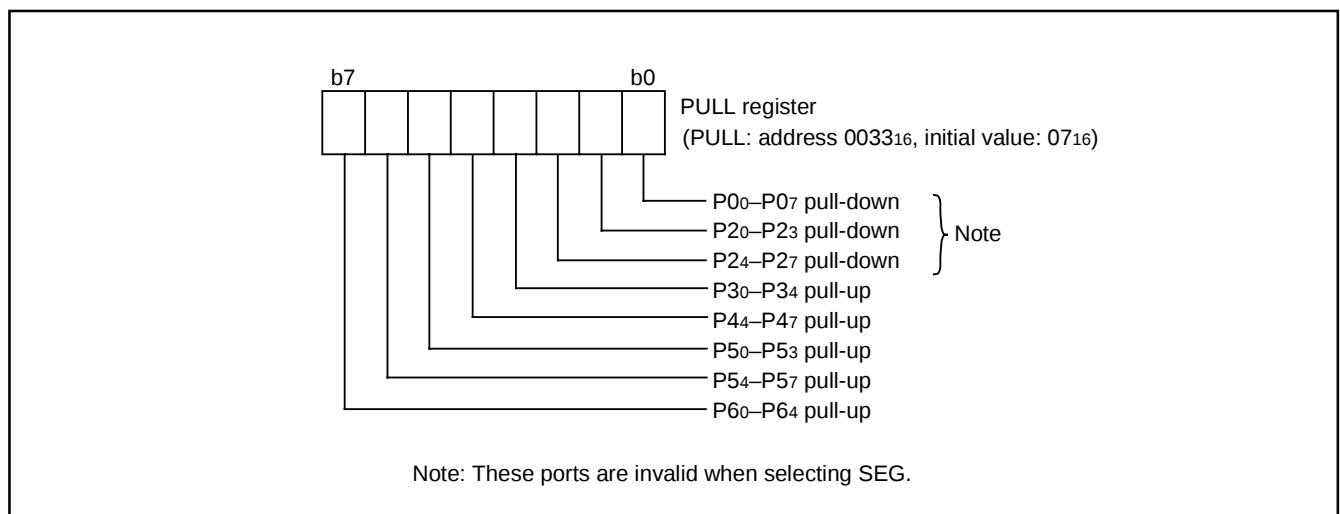


Fig. 11 Structure of PULL register

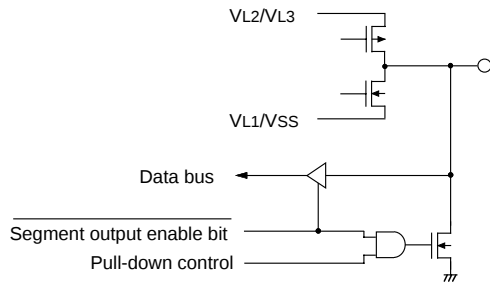
Table 5 List of I/O port function

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Fig. No.
COM0–COM3	Common	Output	LCD common output		LCD mode register	(16)
P00/SEG0– P07/SEG7	Input Port P0	Input, individual bits	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register Segment output enable register LCD0–LCD3	(1)
SEG8–/SEG16	Segment	Output	LCD segment output		LCD mode register LCD4–LCD8	(17)
P20/SEG17– P27/SEG24	I/O Port P2	Input/output individual bits	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register Segment output enable register LCD8–LCD12	(2)
P30(LED)/KW0– P34(LED)/KW4	I/O Port P3	Input/output individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register Interrupt control register	(3)
AN0/ADKEY0– AN3/ADKEY3	A-D conversion input	Input	Analog input	ADKEY input	A-D control register P4 data latch (ADKEY selected)	(15)
P44/AN4– P47/AN7	I/O Port P4	Input/output individual bits	CMOS 3-state output CMOS compatible input level	A-D conversion input	PULL register A-D control register	(4)
P50/INT0, P51/INT1	I/O Port P5	Input/output individual bits	CMOS 3-state output CMOS compatible input level	Interrupt input	PULL register Interrupt edge selection register	(3)
P52/CNTR0				Timer X function input/output	PULL register Timer X mode register	(5)
P53/CNTR1				Timer Y function input	PULL register Timer Y mode register	(6)
P54/SIN				Serial I/O function output	PULL register Serial I/O control register	(7)
P55/SOUT						(8)
P56/SCLK						(9)
P57/SRDY						(10)
P60/XCIN P61/XCOUT	I/O port P6	Input/output individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit input/output	PULL register CPU mode register	(11) (12)
P62/TOUT				Timer 2 output	PULL register Timer X mode register	(13)
P63/φOUT				φ clock output	PULL register φ output control register	(14)
P64					PULL register	(18)

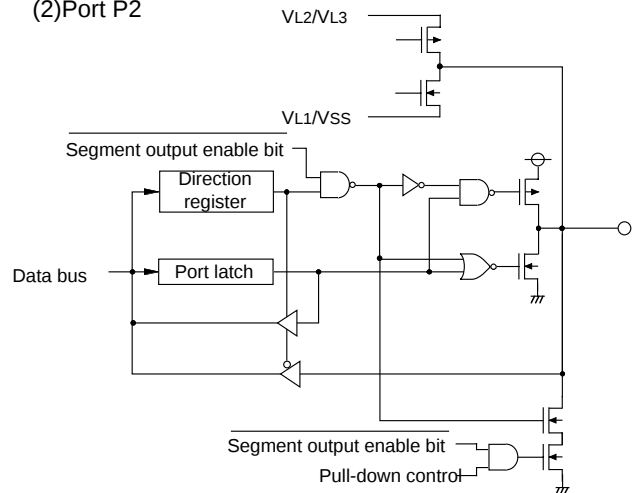
Notes 1: For details of how to use double function ports as function I/O ports, refer to the applicable sections.

2: When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate. Especially, power source current may increase during execution of the STP and WIT instructions. Fix the unused input pins to "H" or "L" through a resistor.

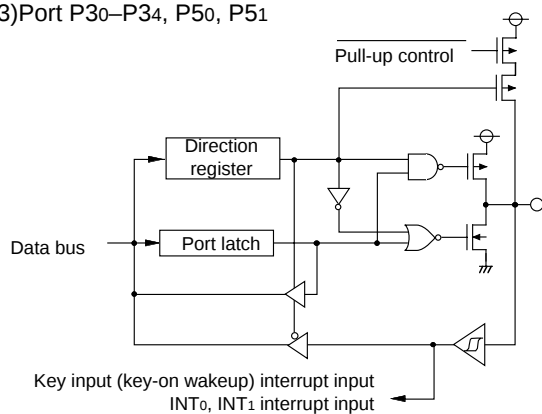
(1)Port P0



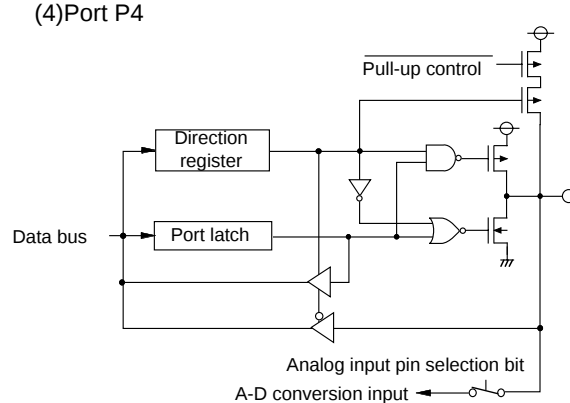
(2)Port P2



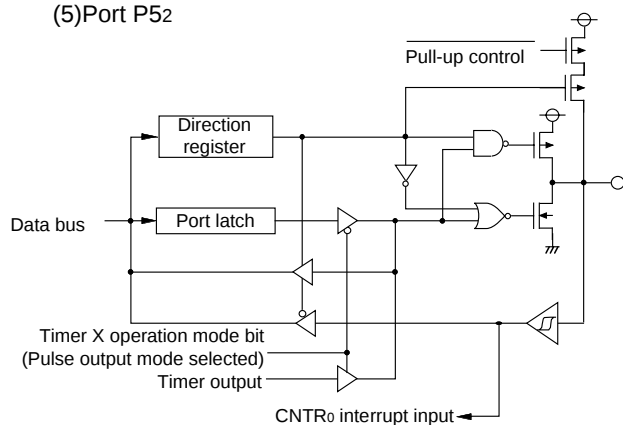
(3)Port P30–P34, P50, P51



(4)Port P4



(5)Port P52



(6)Port P53

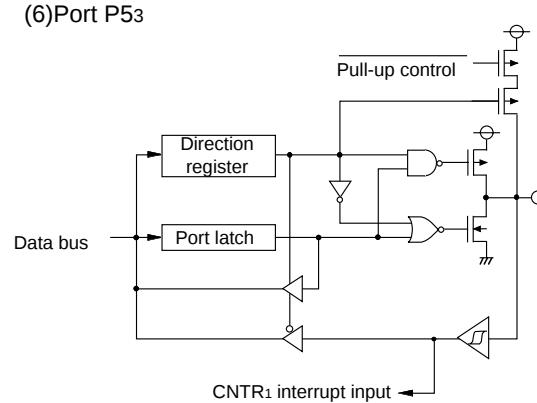


Fig. 12 Port block diagram (1)

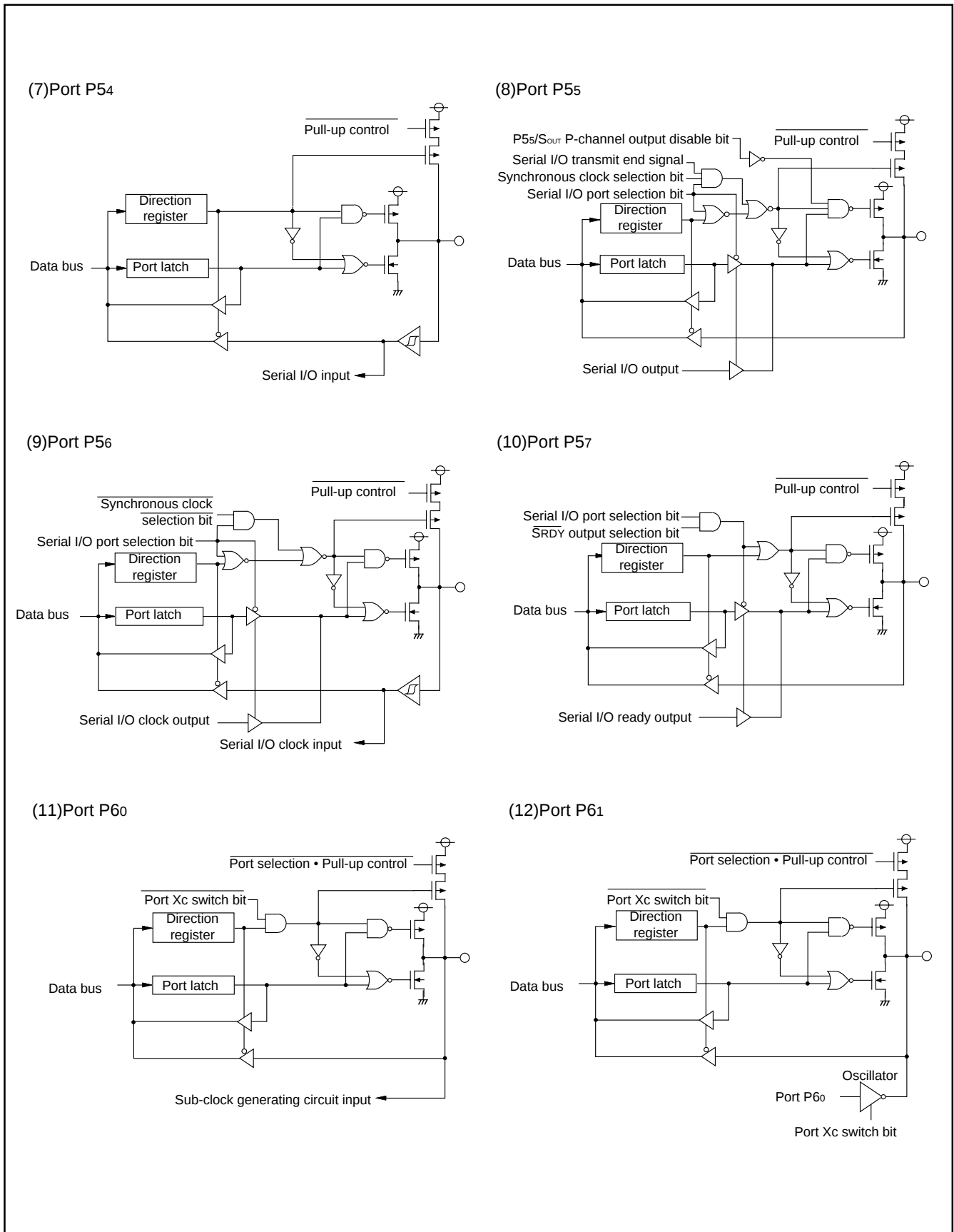
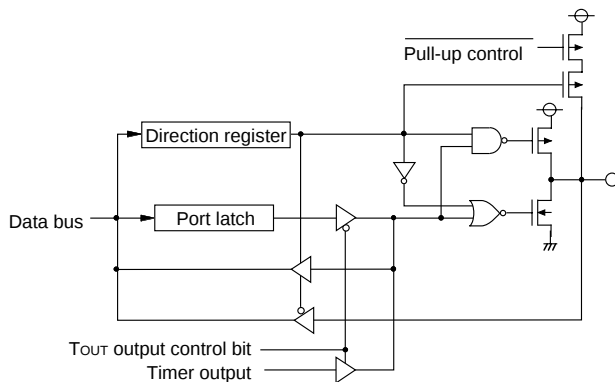
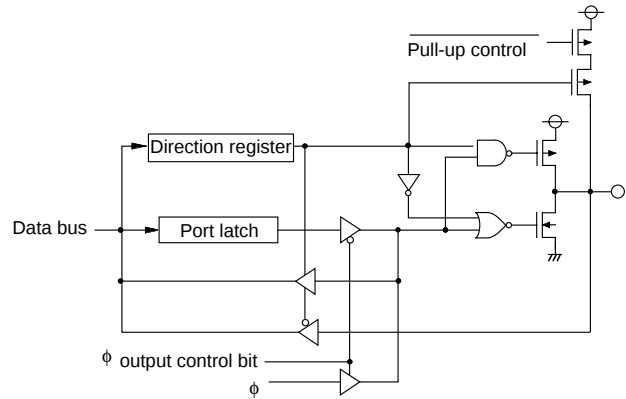


Fig. 13 Port block diagram (2)

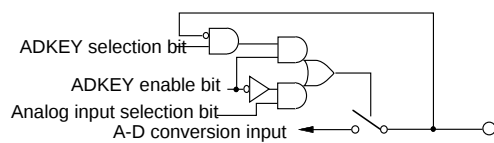
(13)Port P62



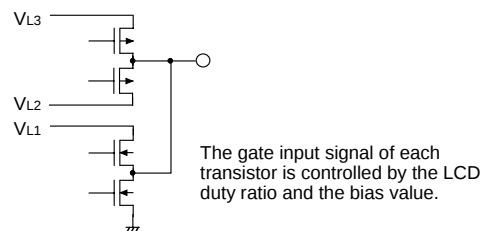
(14)Port P63



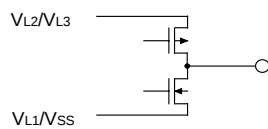
(15)AN0/ADKEY0-AN3/ADKEY3



(16)COM0-COM3



(17)SEG8-SEG16



The voltage applied to the sources of P-channel and N-channel transistors is the controlled voltage by the bias value.

(18)Port P64

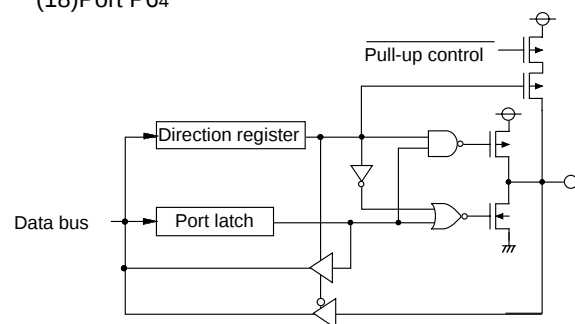


Fig. 14 Port block diagram (3)

INTERRUPTS

Interrupts occur by thirteen sources: five external, seven internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■ Notes on Interrupts

When the active edge of an external interrupt (INT0, INT1, CNTR0 or CNTR1) is set or an interrupt source where several interrupt source is assigned to the same vector address is switched, the corresponding interrupt request bit may also be set. Therefore, take following sequence:

- (1) Disable the interrupt.
- (2) Set the interrupt edge selection register (Timer X control register for CNTR0, Timer Y mode register for CNTR1).
- (3) Clear the set interrupt request bit to "0."
- (4) Enable the interrupt.

Table 6 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD ₁₆	FFFC ₁₆	At reset	Non-maskable
INT0	2	FFFB ₁₆	FFFA ₁₆	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1	3	FFF9 ₁₆	FFF8 ₁₆	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Timer X	4	FFF3 ₁₆	FFF2 ₁₆	At timer X underflow	
Timer Y	5	FFF1 ₁₆	FFF0 ₁₆	At timer Y underflow	
Timer 1	6	FFEF ₁₆	FFEE ₁₆	At timer 1 underflow	
Timer 3	7	FFED ₁₆	FFEC ₁₆	At timer 3 underflow	
CNTR0	8	FFEB ₁₆	FFEA ₁₆	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	9	FFE9 ₁₆	FFE8 ₁₆	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Timer 2	10	FFE7 ₁₆	FFE6 ₁₆	At timer 2 underflow	
Serial I/O	11	FFE3 ₁₆	FFE2 ₁₆	At completion of serial I/O data transmission or reception	
Key input (Key-on wake-up)	12	FFE1 ₁₆	FFE0 ₁₆	At falling of conjunction of input level for port P3 (at input mode)	External interrupt (valid at falling)
A-D conversion	13	FFDF ₁₆	FFDE ₁₆	At completion of A-D conversion	Valid when A-D interrupt is selected
BRK instruction	14	FFDD ₁₆	FFDC ₁₆	At BRK instruction execution	Non-maskable software interrupt

Notes1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

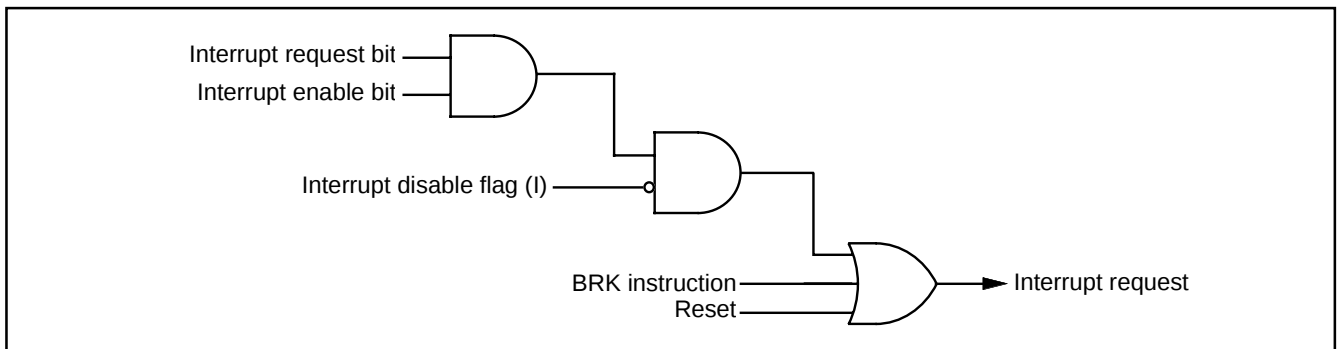


Fig. 15 Interrupt control

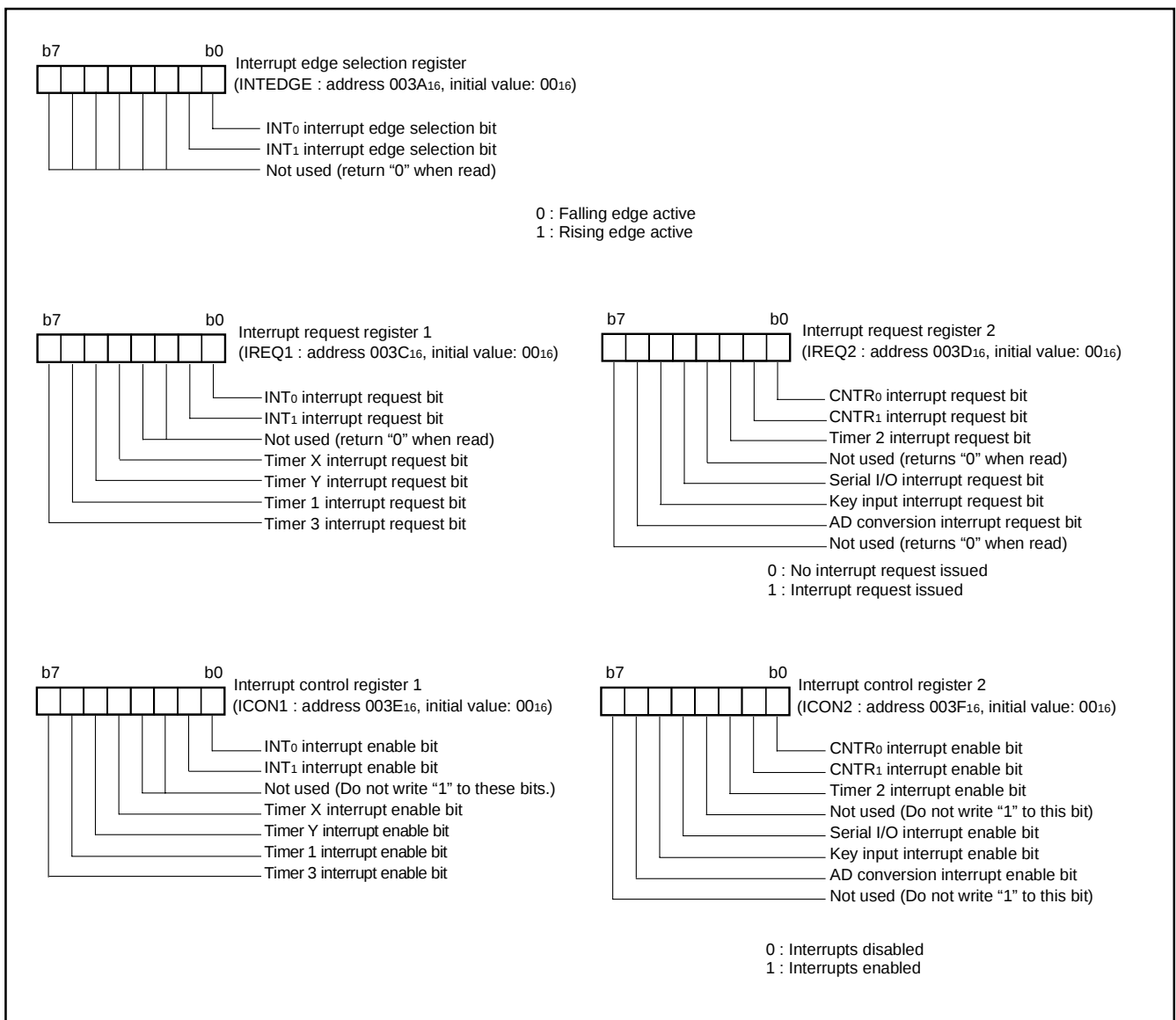


Fig. 16 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake Up)

A Key-on wake up interrupt request is generated by applying "L" level voltage to any pin of port P3 that have been set to input mode. In other words, it is generated when AND of input level

goes from "1" to "0". An example of using a key input interrupt is shown in Figure 17, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P30–P33.

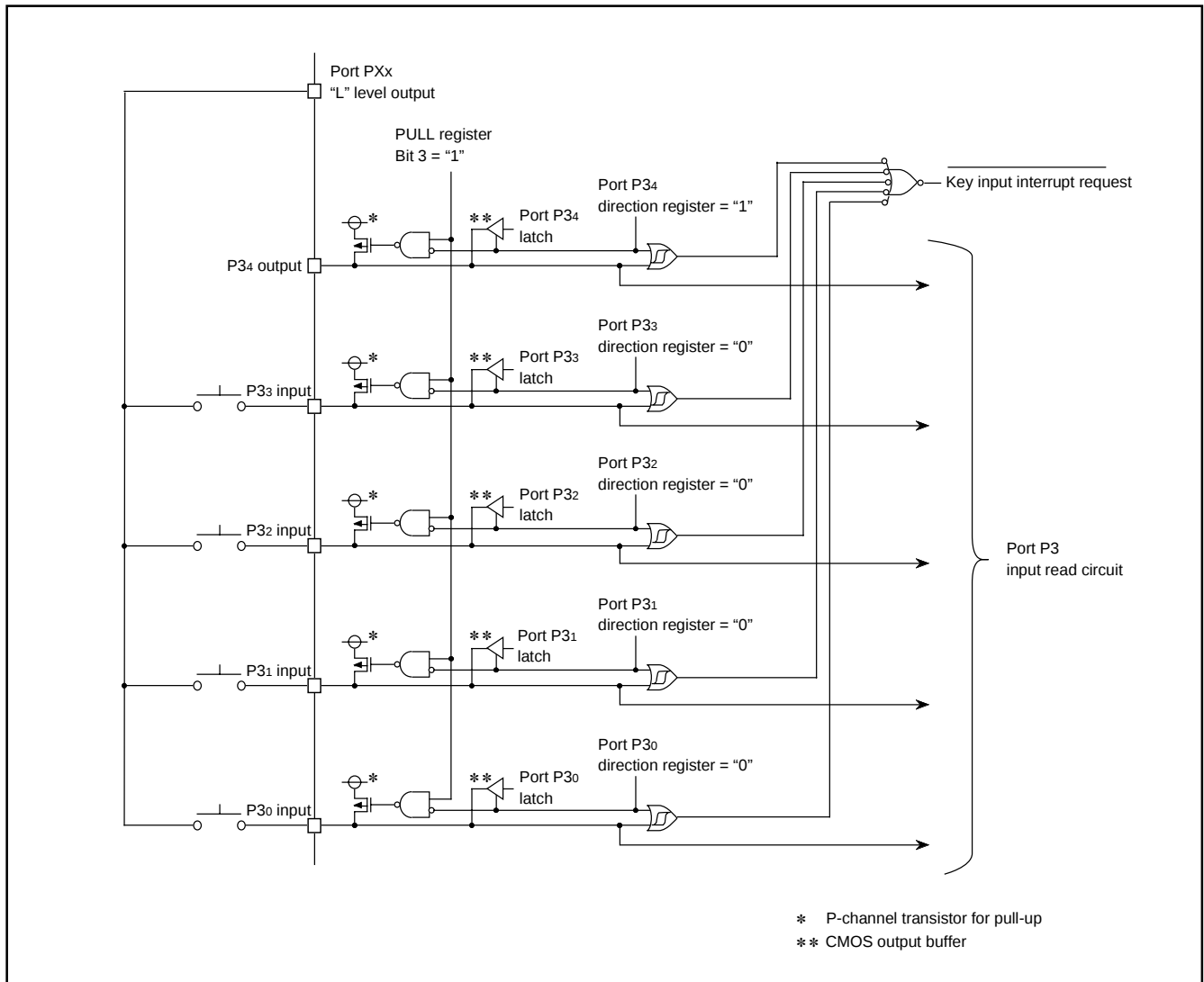


Fig. 17 Connection example when using key input control register, key input interrupt and port P3 block diagram

TIMERS

The 38C1 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "0", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

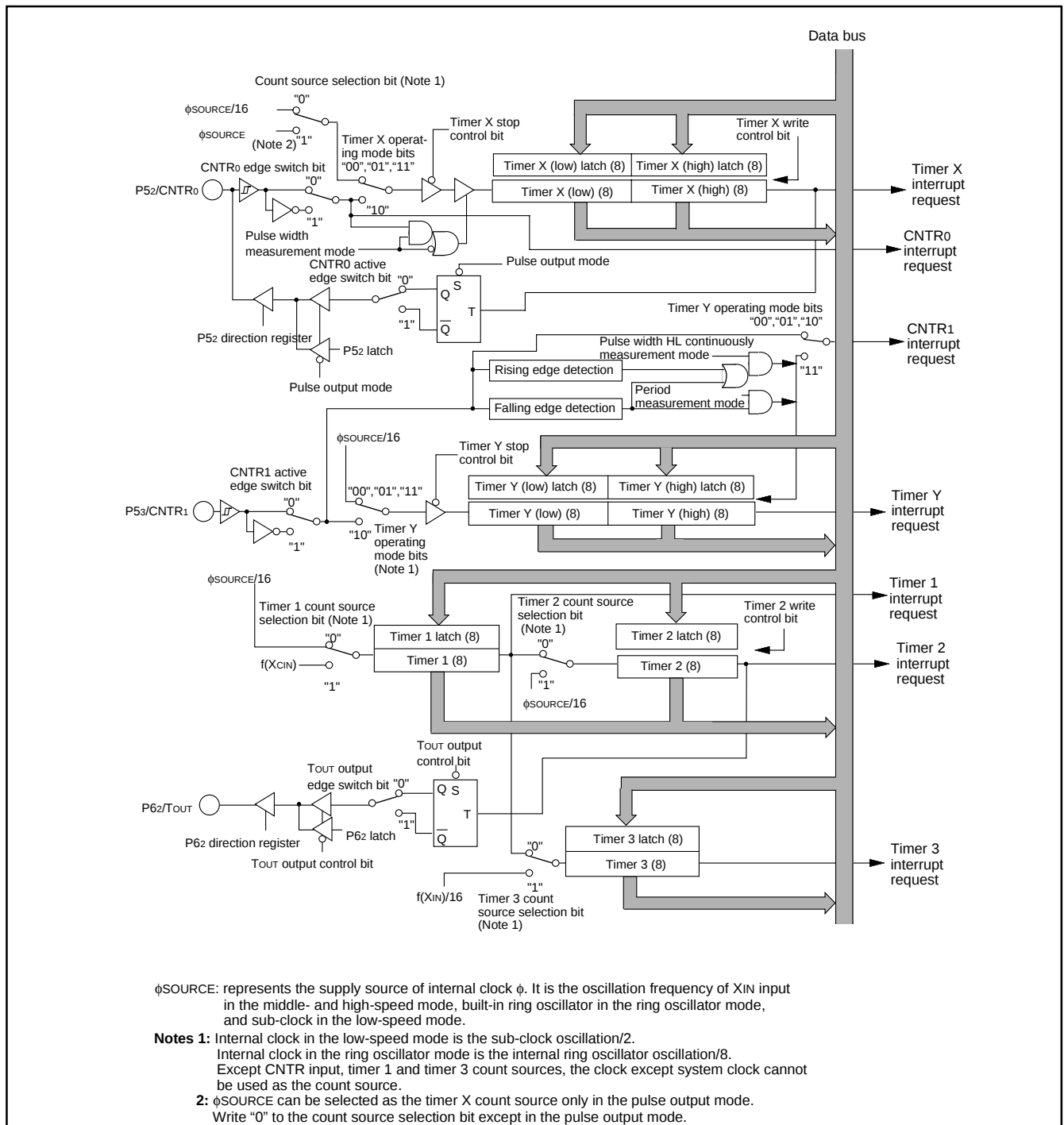


Fig. 18 Timer block diagram

Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

(1) Timer mode

The timer counts the followings;

- $f(XIN)$ (input frequency to XIN pin) divided by 16 in middle-, or high-speed mode
- $f(XCIN)$ (sub-clock oscillation frequency) divided by 16 in low-speed mode
- $f(XROSC)$ (built-in ring oscillator oscillation frequency) divided by 16 in ring oscillator mode

(2) Pulse output mode

Each time the timer underflows, a signal output from the $CNTR0$ pin is inverted and $f(XIN)$, $f(ROSC)$ or $f(XCIN)$ can be selected for the count source. Except for them, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P52 direction register to output mode.

(3) Event counter mode

The timer counts signals input through the $CNTR0$ pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P52 direction register to input mode.

(4) Pulse width measurement mode

The count source is $f(XIN)/16$ in the middle-, or high-speed mode, $f(ROSC)/16$ in ring oscillator mode, and $f(XCIN)/16$ in the low-speed mode. If $CNTR0$ active edge switch bit is "0", the timer counts while the input signal of $CNTR0$ pin is at "H". If it is "1", the timer counts while the input signal of $CNTR0$ pin is at "L". When using a timer in this mode, set the corresponding port P52 direction register to input mode.

●Timer X Write Control

If the timer X write control bit is "0", when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.

If the timer X write control bit is "1", when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.

If the value is written in latch only, when the value is written in latch at the timer underflow, the value is loaded in the timer X and the latch at the same time. Also, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

■Note on $CNTR0$ interrupt active edge selection

$CNTR0$ interrupt active edge depends on the $CNTR0$ active edge switch bit.

■Note on count source selection bit

Except the pulse output mode, write "0" to the count source selection bit.

When the timer X count source selection bit is set to "1", as for the recommended operating condition of the main clock input frequency $f(XIN)$, the rating value at the high-speed mode is applied.

■Note on interrupt in pulse output mode

When the count source selection bit is "1" in the pulse output mode, the timing when the timer X interrupt request occurs may be early or lately for one instruction cycle.

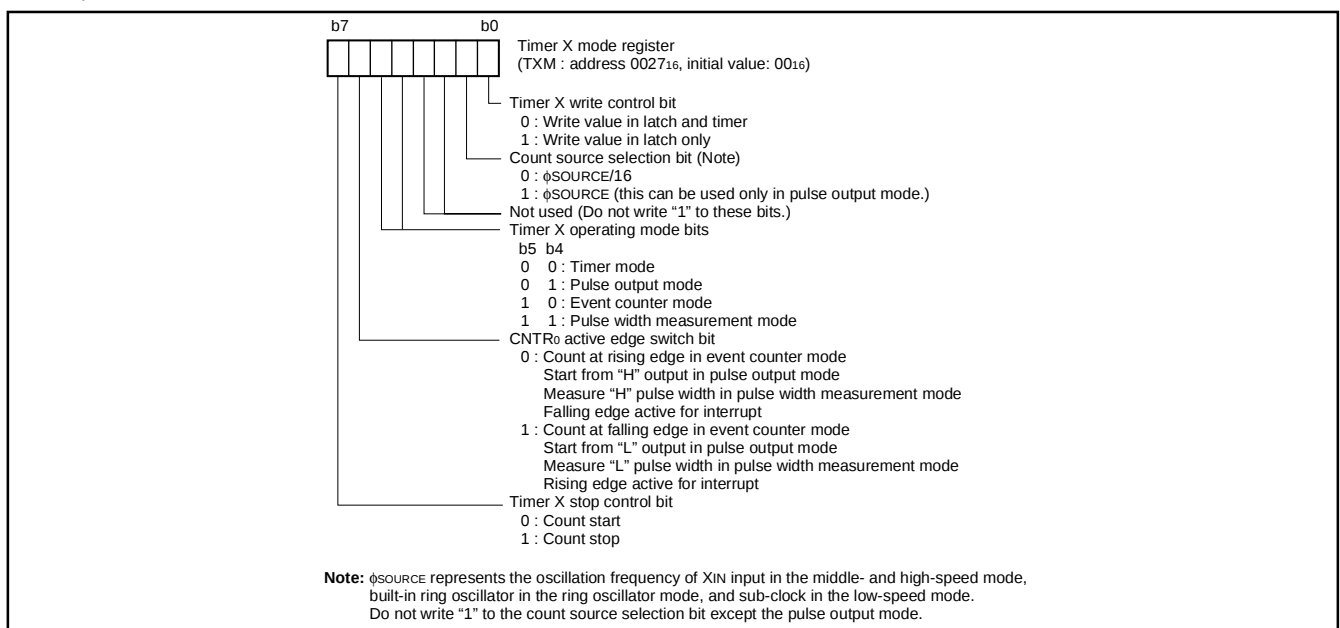


Fig. 19 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer mode

The timer counts the followings;

- $f(X_{IN})/16$ in middle-, or high-speed mode
- $f(X_{CIN})/16$ in low-speed mode
- $f(X_{ROSC})$ divided by 16 in ring oscillator mode

(2) Period measurement mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the corresponding port P53 direction register to input mode.

(3) Event counter mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P53 direction register to input mode.

(4) Pulse width HL continuously measurement mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port P53 direction register to input mode.

■Note on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

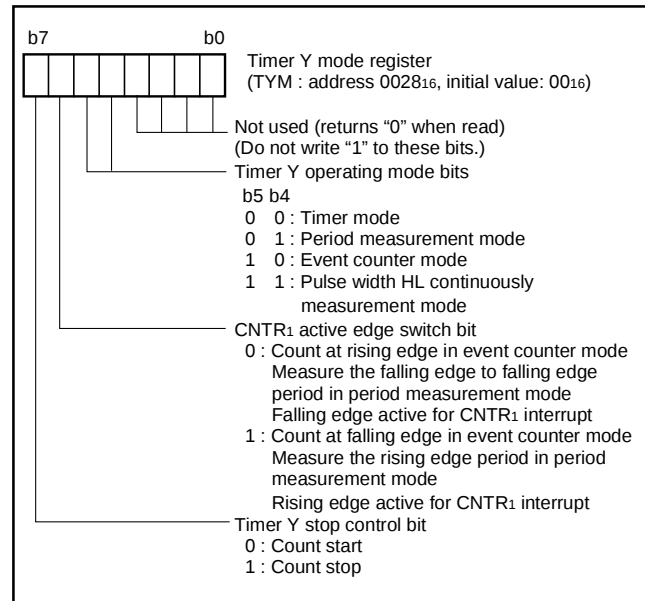


Fig. 20 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer. Therefore, rewrite the value of timer whenever the count source is changed.

●Timer 2 Write Control

If the timer 2 write control bit is "0", when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is "1", when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

●Timer 2 Output Control

When the timer 2 (TOUT) is output enabled, an inversion signal from pin TOUT is output each time timer 2 underflows.

In this case, set the port P62 shared with the port TOUT to the output mode.

■Note on Timer 1 to Timer 3

When the count source of timers 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

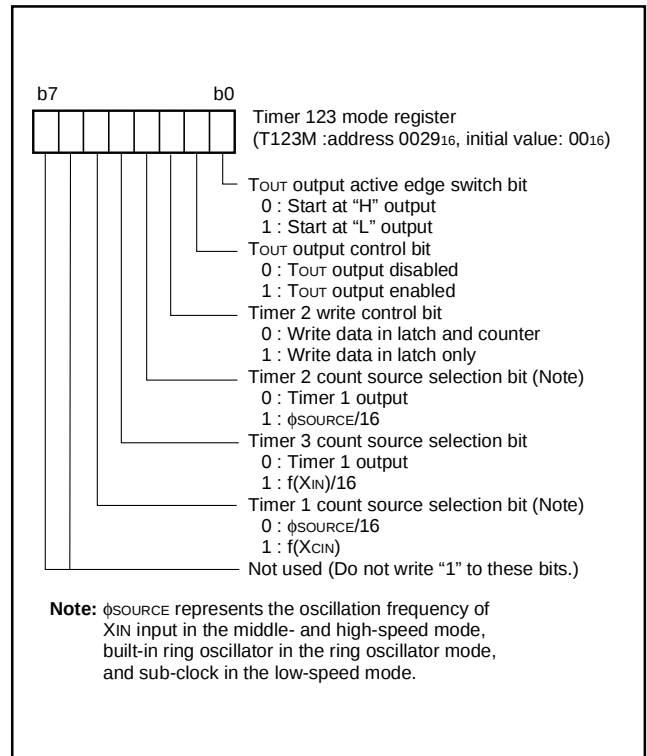


Fig. 21 Structure of timer 123 mode register

Serial I/O

The serial I/O function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. When the internal clock is used, transfer is started by a write signal to the serial I/O register.

[Serial I/O Control Register (SIOCON)] 001D16

The serial I/O control register contains 8 bits which control various serial I/O functions.

■ Notes on Serial I/O

Write data to the serial I/O register only when the SCLK pin is "H".

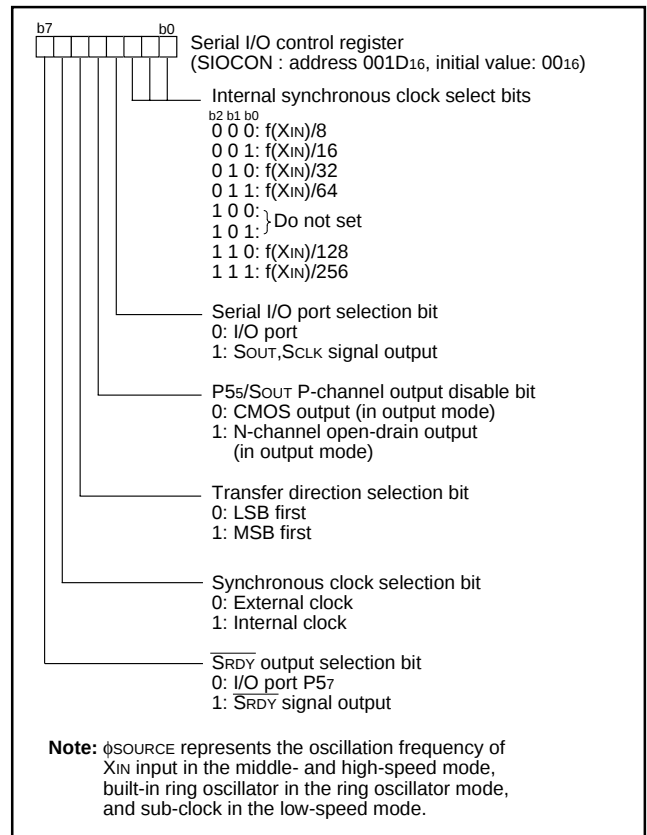


Fig. 22 Structure of serial I/O control register

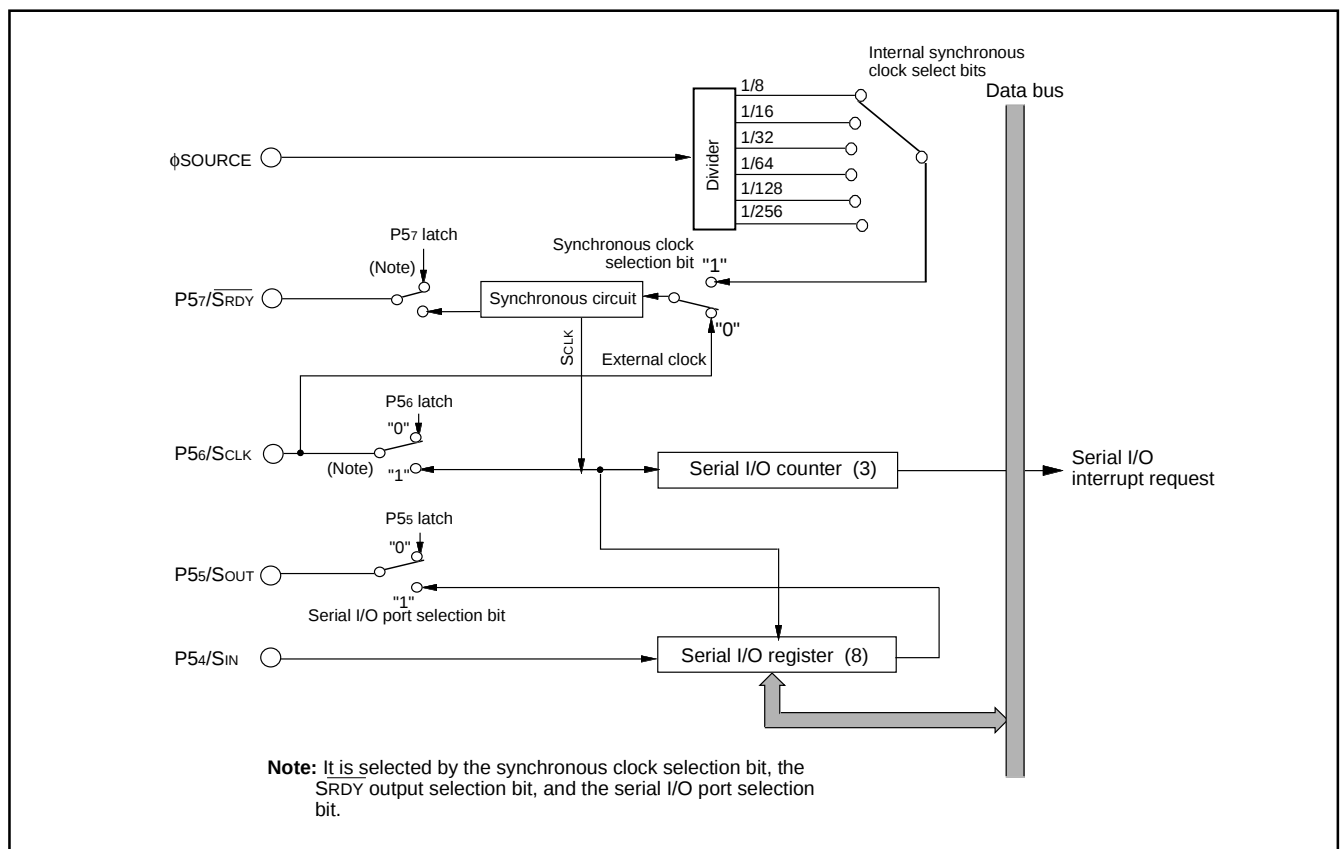


Fig. 23 Block diagram of serial I/O function

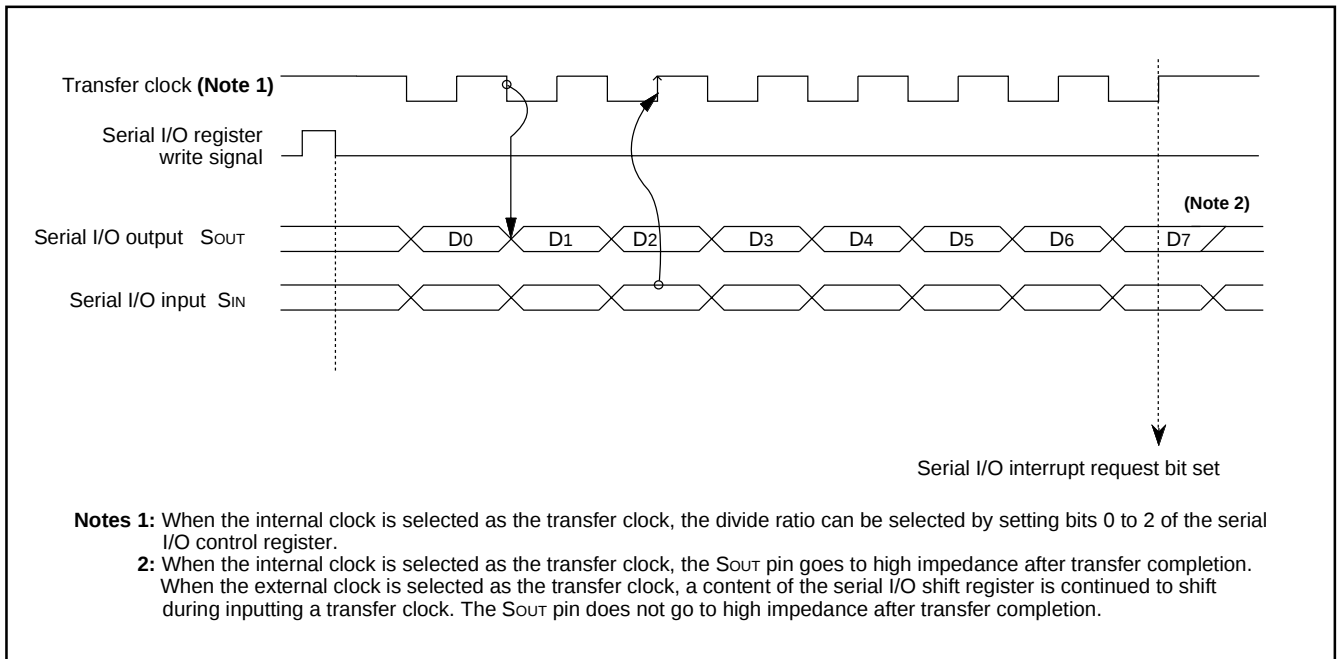


Fig. 24 Timing of serial I/O function

A-D CONVERTER

The functional blocks of the A-D converter are described below.

● A-D Converter

The conversion method of this A-D converter is the 8-bit resolution successive comparison method. This A-D converter has the ADKEY function for A-D conversion of "L" level analog input to ADKEY pin automatically.

[A-D Conversion Register (AD)] 003516

The A-D conversion register is a read-only register that contains the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read. After power on or system is released from reset, the value is undefined.

[A-D Control Register (ADCON)] 003416

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion. Bit 4 enables the ADKEY function. Writing "1" to this bit enables the ADKEY function. When this function is set to be valid, the analog input pin selection bits are invalid. Also, when the bit 4 is "1", do not write "0" to bit 3 by program.

Resistor ladder

The resistor ladder divides the voltage between Vcc and Vss by 256, and outputs the comparison voltages to the comparator.

Channel Selector

The channel selector selects one of the input ports AN7–AN0.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the charge is lost if the conversion speed is not enough.

Accordingly, set f(XIN) to at least 500kHz during A-D conversion in the middle- or high-speed mode.

Also, do not execute the STP and WIT instructions during the A-D conversion.

In the low-speed mode, since the A-D conversion is executed by the built-in self-oscillation circuit, the minimum value of f(XIN) frequency is not limited.

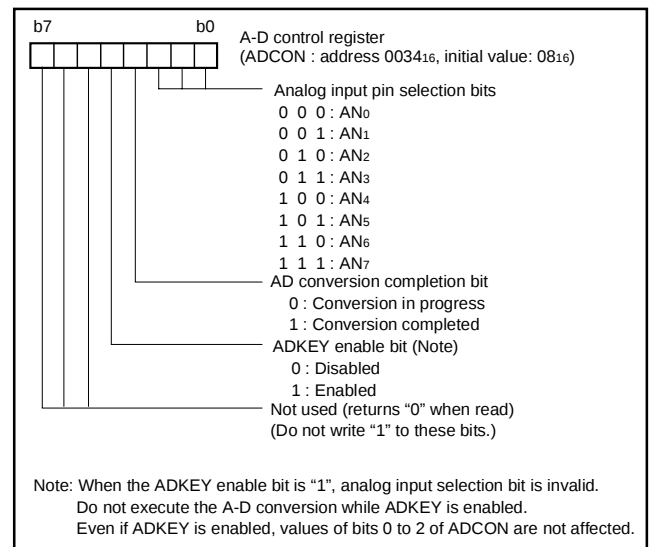


Fig. 25 Structure of A-D control register

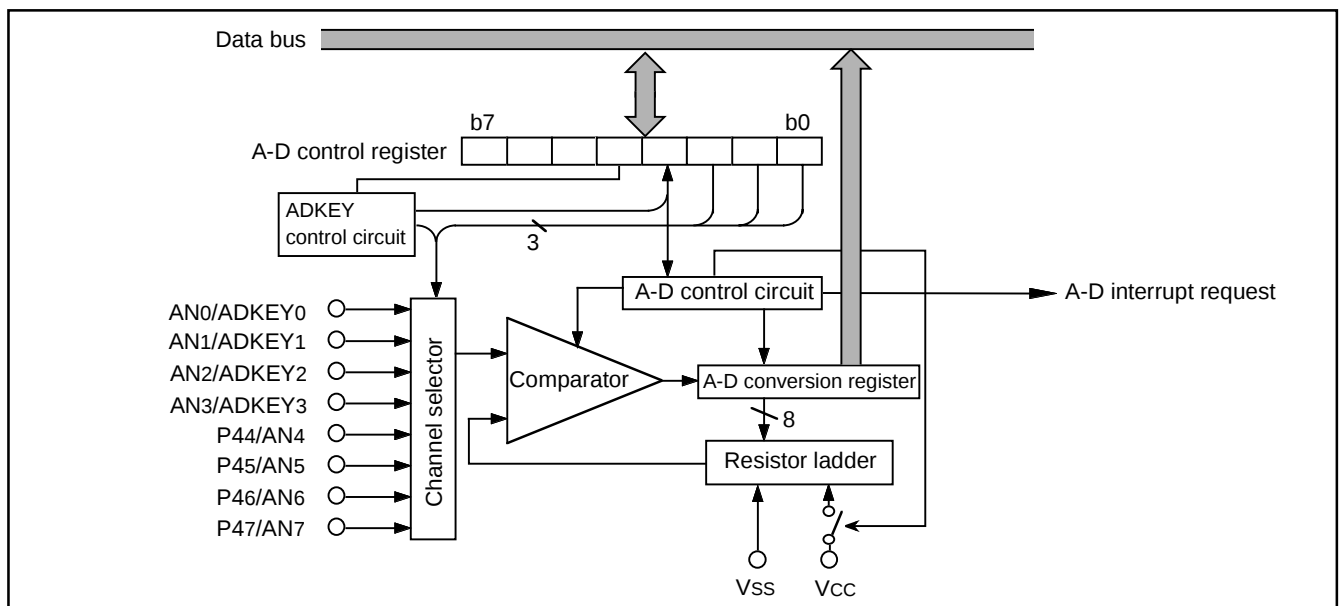


Fig. 26 A-D converter block diagram

ADKEY Control Circuit

The ADKEY function is the function for A-D conversion of the "L" level analog input voltage input to the ADKEY pin automatically. This function can be used also in the state of STP and WIT.

• ADKEY Selection

Two or more ADKEY pins can be selected by the low-order 4 bits of P4 data register.

If "L" level input to an ADKEY pin is detected, other bits are set to "0" and only the corresponding ADKEY selection bit is set to "1". As a result, the pin with "L" level input can be recognized.

• ADKEY Enable

The ADKEY function is enabled by writing "1" to the ADKEY enable bit. Surely, in order to enable ADKEY function, set "1" to the ADKEY enable bit, after selecting the ADKEY pin.

ADKEY becomes disabled automatically after the A-D conversion end by the ADKEY function. When the ADKEY enable bit of the A-D control register is "1", the analog input pin selection bits become invalid. Please do not write "0" in the AD conversion completion bit by the program during ADKEY enabled state.

[ADKEY Control Circuit]

The pins which performs A-D conversion is selected with the ranking of ADKEY0, ADKEY1, ADKEY2, and ADKEY3 when there is an "L" level input simultaneously to two or more valid ADKEY pins. In order to obtain a more exact conversion result, by the A-D conversion with ADKEY, execute the following;

- ① set the input to the ADKEY pin into a steep falling waveform,
- ② stabilize the input voltage within 8 clock cycle ($1\ \mu\text{s}$ at $f(\text{XIN}) = 8\text{MHz}$) after the input voltage is under V_{IL} , and
- ③ maintain the input voltage until the completion of the A-D conversion.

The threshold voltage with an actual ADKEY pin is the voltage between V_{IH} - V_{IL} .

In order not to make ADKEY operation perform superfluously in a noise etc., in the state of the waiting for an input, set the voltage of an ADKEY pin to V_{IH} ($0.9V_{\text{CC}}$) or more.

When the following operations are performed, the A-D conversion operation cannot be guaranteed.

- When the CPU mode register is operated during A-D conversion operation,
- When the AD conversion control register is operated during A-D conversion operation,
- When STP or WIT instructin is executed during A-D conversion operation,
- When the ADKEY pin selection bit is operated during A-D conversion operation at selecting ADKEY function, and
- Return operation by reset, STOP or WIT under A-D conversion operation at selecting ADKEY function is performed.

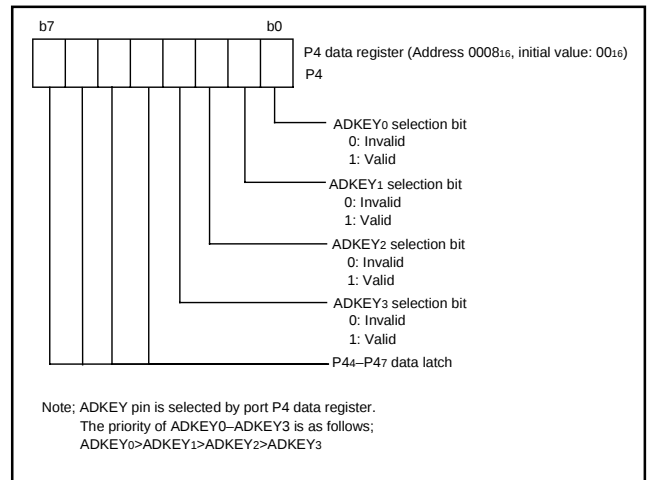


Fig. 27 Structure of ADKEY pin selection bits

Definition of A-D converter accuracy

The A-D conversion accuracy is defined below (refer to Figure 28).

• Relative accuracy

① Zero transition voltage (V_{0T})

This means an analog input voltage when the actual A-D conversion output data changes from "0" to "1."

② Full-scale transition voltage (V_{FST})

This means an analog input voltage when the actual A-D conversion output data changes from "255" to "254."

③ Linearity error

This means a deviation from the line between V_{0T} and V_{FST} of a converted value between V_{0T} and V_{FST} .

④ Differential non-linearity error

This means a deviation from the input potential difference required to change a converter value between V_{0T} and V_{FST} by 1 LSB at the relative accuracy.

• Absolute accuracy

This means a deviation from the ideal characteristics between 0 to V_{REF} (V_{CC} in 38C1 Group) of actual A-D conversion characteristics.

V_n : Analog input voltage when the output data changes from "n" to "n+1" ($n = 0$ to 254)

$$\bullet \text{ 1LSB at relative accuracy} \rightarrow \frac{V_{FST} - V_{0T}}{254} \quad (V)$$

$$\bullet \text{ 1LSB at absolute accuracy} \rightarrow \frac{V_{REF}^*}{256} \quad (V)$$

* $V_{REF} = V_{CC}$ in the 38C1 Group.

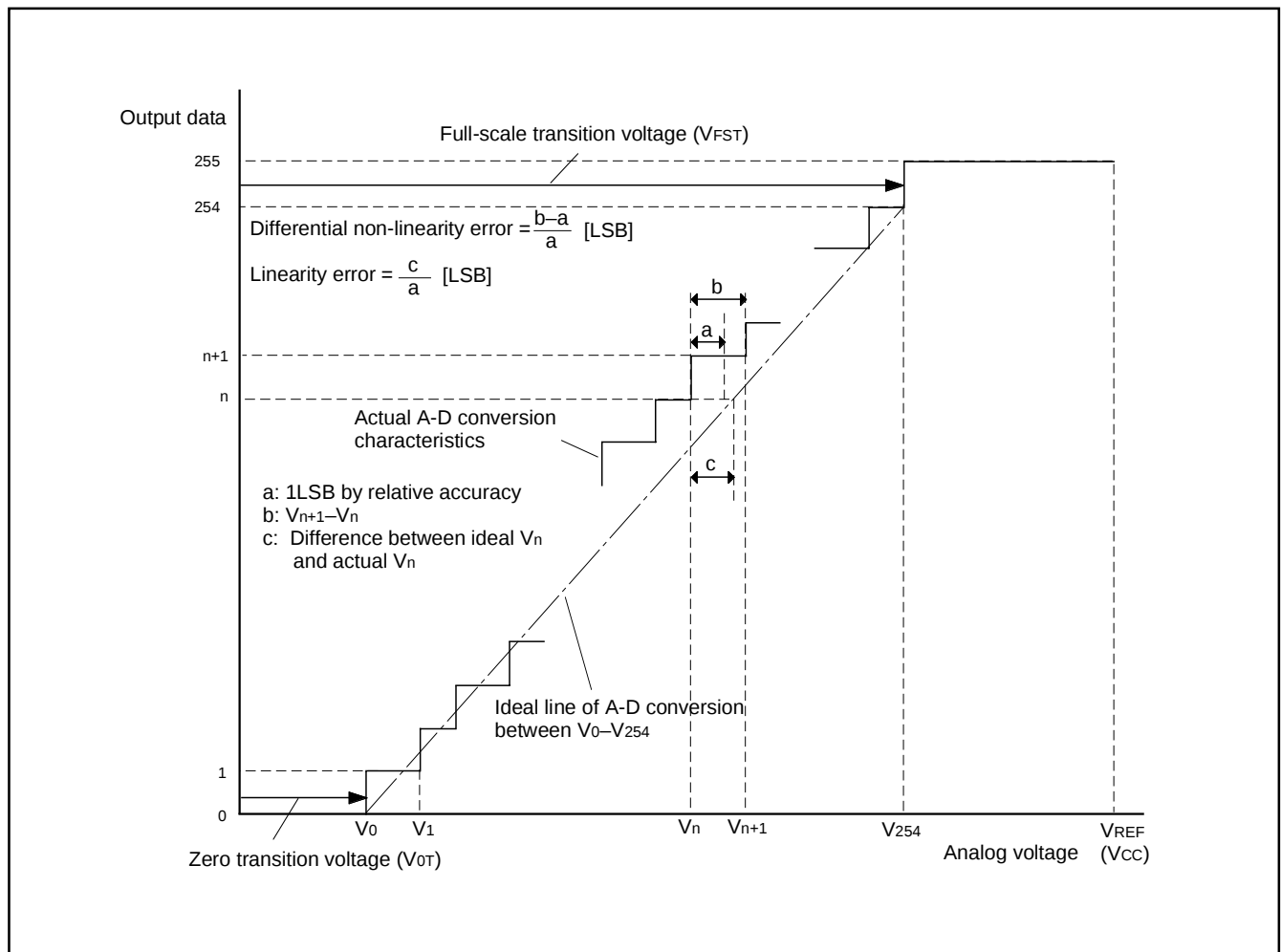


Fig. 28 Definition of A-D conversion accuracy

LCD DRIVE CONTROL CIRCUIT

The 38C1 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

- LCD display register
- Segment output enable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 25 segment output pins and 4 common output pins can be used.

Up to 100 pixels can be controlled for LCD display. When the LCD enable bit is set to "1" after data is set in the LCD mode register,

the segment output enable register and the LCD display register, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 7. Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
1	25 dots or 8 segment LCD 3 digits
2	50 dots or 8 segment LCD 6 digits
3	75 dots or 8 segment LCD 9 digits
4	100 dots or 8 segment LCD 12 digits

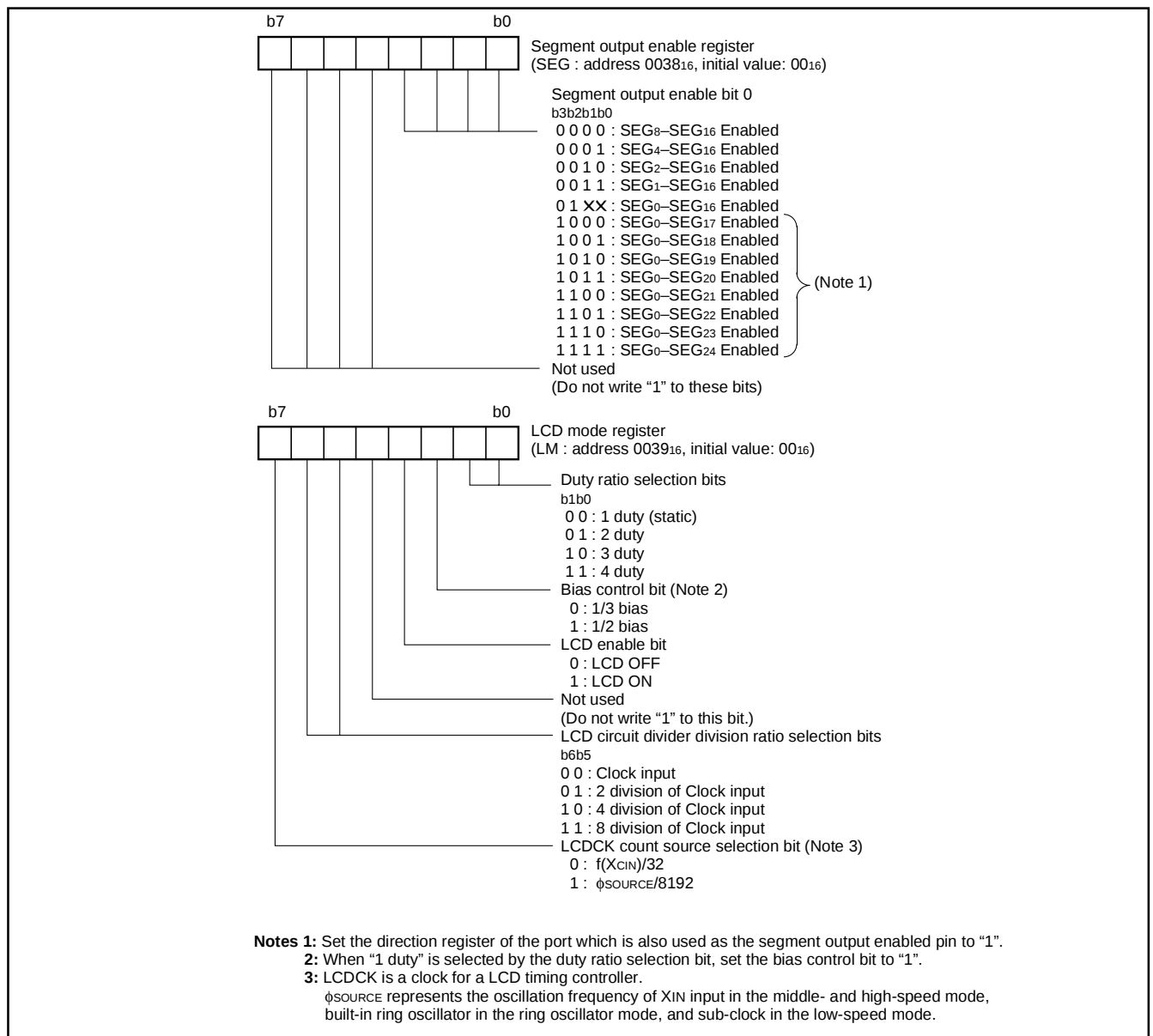


Fig. 29 Structure of segment output enable register and LCD mode register

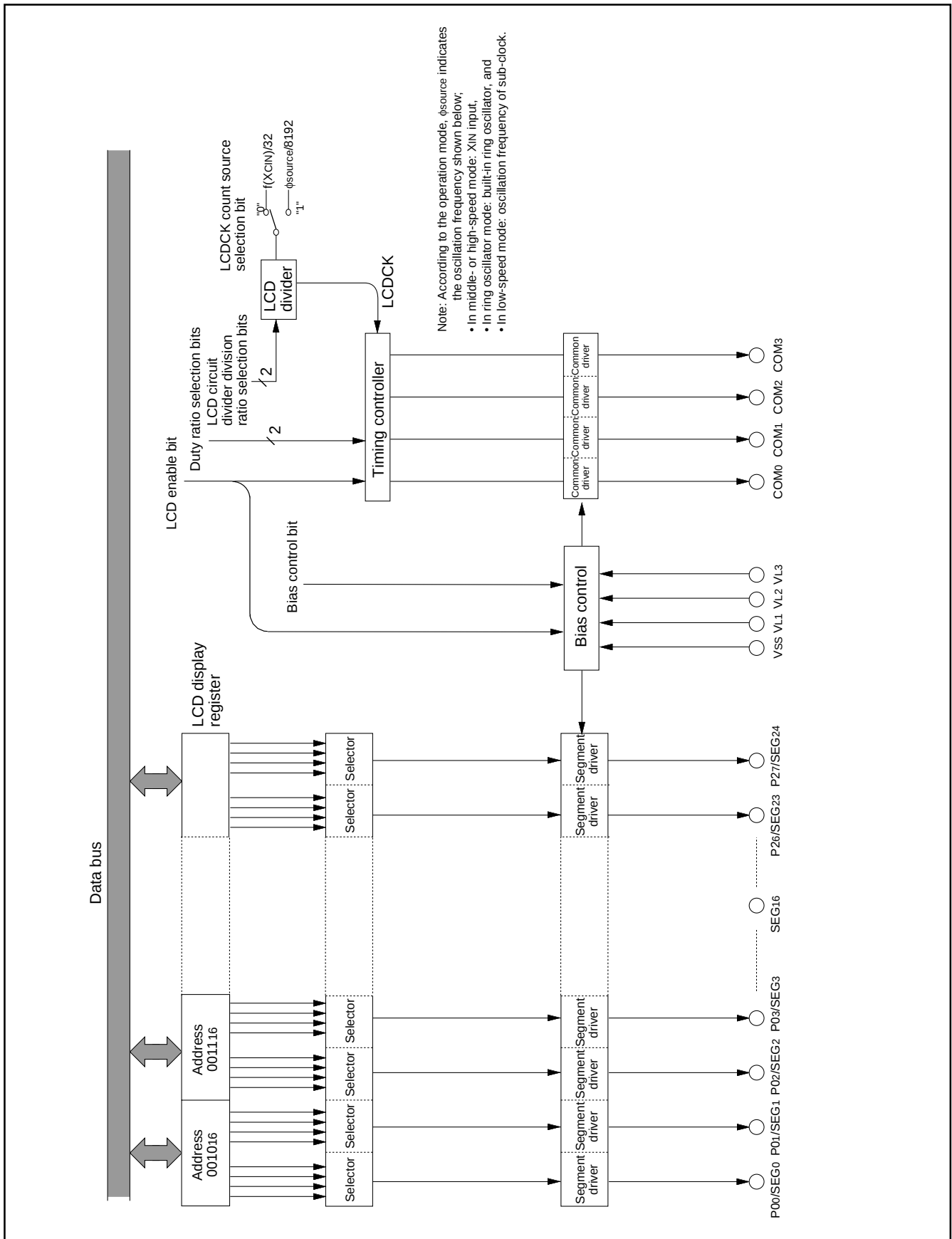


Fig. 30 Block diagram of LCD controller/driver

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (VL1–VL3), apply the voltage shown in Table 8 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM0–COM3) to be used are determined by duty ratio.

Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

When the LCD enable bit is “0”, the output of COM0–COM3 is “L” level.

Table 8. Bias control and applied voltage to VL1–VL3

Bias value	Voltage value
1/3 bias	VL3=VLCD VL2=2/3 VLCD VL1=1/3 VLCD
1/2 bias	VL3=VLCD VL2=VL1=1/2 VLCD
1/1 bias (static)	VL3=VLCD VL2=VL1=1/2 VSS

Note : VLCD is the maximum value of supplied voltage for the LCD panel.

Table 9. Duty ratio control and common pins used

Duty ratio	Duty ratio selection bits		Common pins used
	Bit 1	Bit 0	
1	0	0	COM0 (Note 1)
2	0	1	COM0, COM1 (Note 2)
3	1	0	COM0–COM2 (Note 3)
4	1	1	COM0–COM3

Notes 1: Set COM1, COM2 and COM3 to be open.

2: Set COM2 and COM3 to be open.

3: Set COM3 to be open.

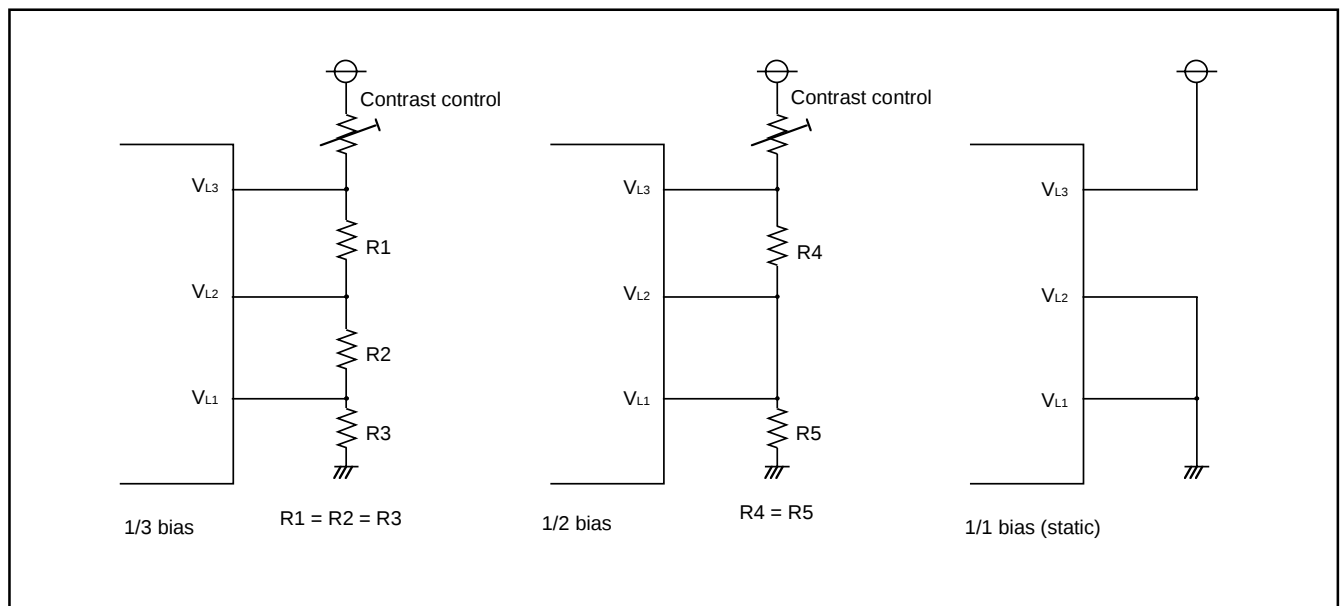


Fig. 31 Example of circuit at each bias

LCD Display register

Address 0010₁₆ to 001C₁₆ is the LCD display register. When “1” are written to these addresses, the corresponding segments of the LCD display panel are turned on.

$$f(\text{LCDCK}) = \frac{\text{frequency of count source for LCDCK}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(\text{LCDCK})}{\text{duty ratio}}$$

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

Address \ Bits	7	6	5	4	3	2	1	0
0010 ₁₆	SEG ₁				SEG ₀			
0011 ₁₆	SEG ₃				SEG ₂			
0012 ₁₆	SEG ₅				SEG ₄			
0013 ₁₆	SEG ₇				SEG ₆			
0014 ₁₆	SEG ₉				SEG ₈			
0015 ₁₆	SEG ₁₁				SEG ₁₀			
0016 ₁₆	SEG ₁₃				SEG ₁₂			
0017 ₁₆	SEG ₁₅				SEG ₁₄			
0018 ₁₆	SEG ₁₇				SEG ₁₆			
0019 ₁₆	SEG ₁₉				SEG ₁₈			
001A ₁₆	SEG ₂₁				SEG ₂₀			
001B ₁₆	SEG ₂₃				SEG ₂₂			
001C ₁₆	—				SEG ₂₄			
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Fig. 32 LCD display register map

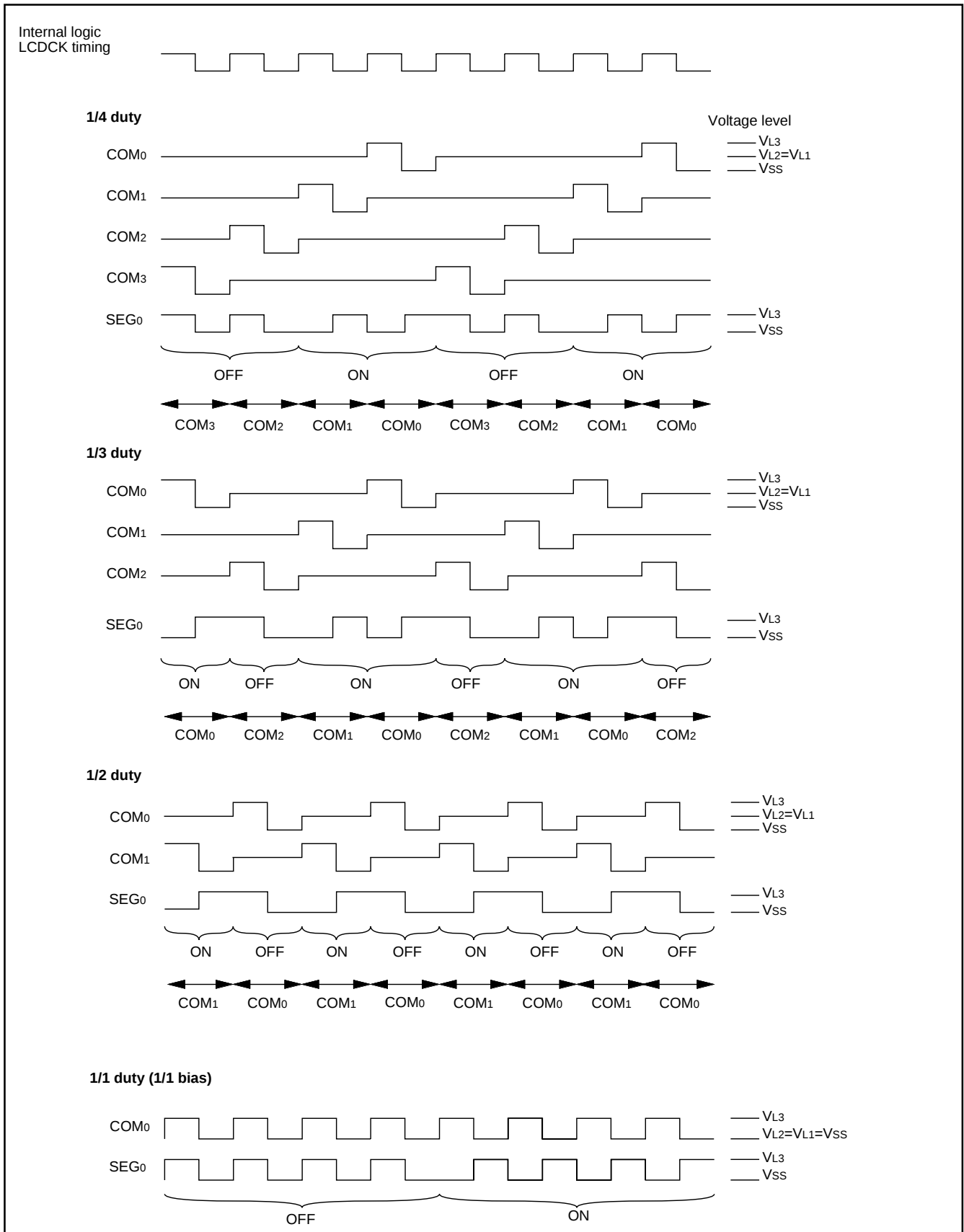


Fig. 33 LCD drive waveform (1/2 bias, 1/1 bias)

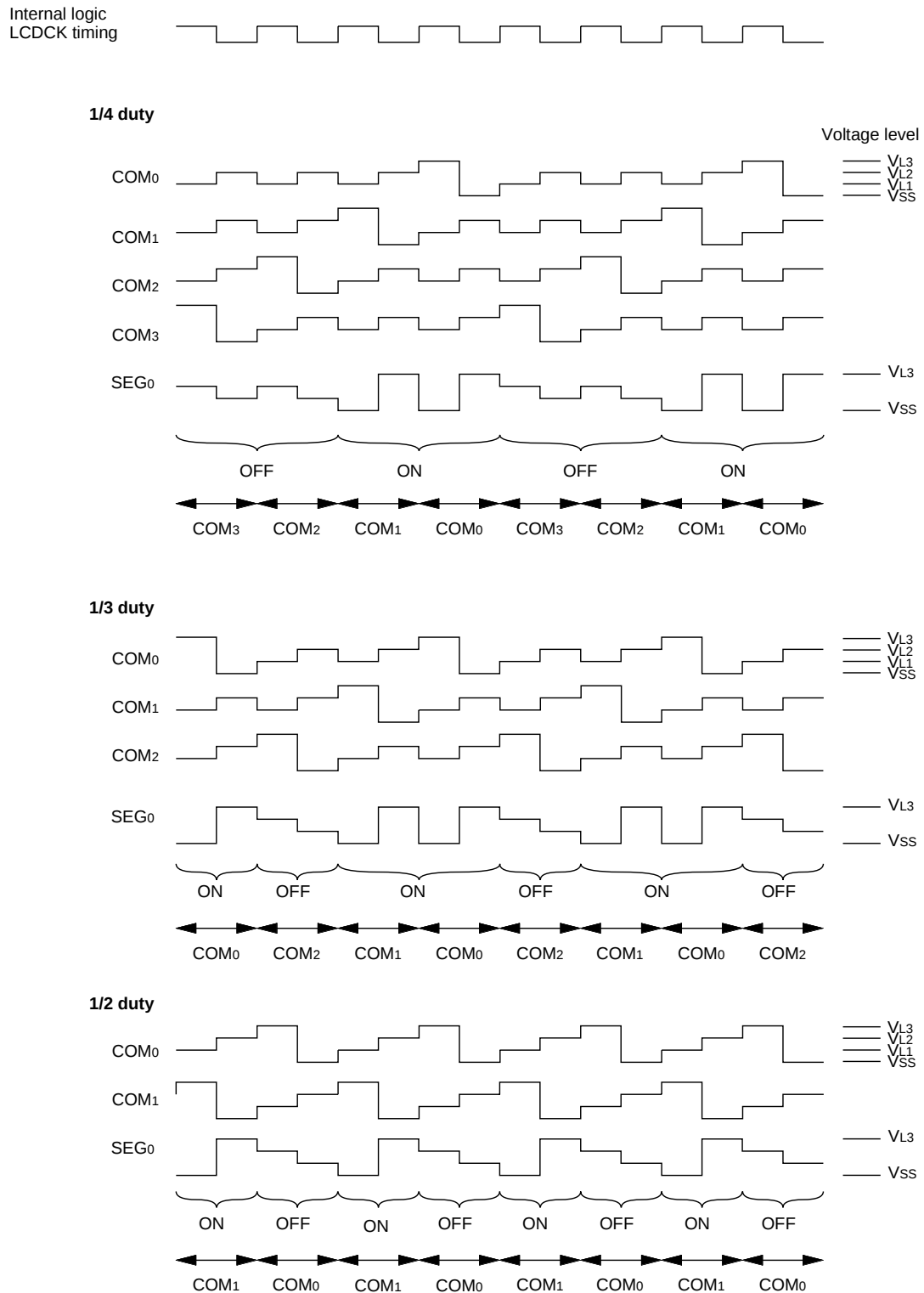


Fig. 34 LCD drive waveform (1/3 bias)

OTHER FUNCTION REGISTERS

● ϕ clock output function

The internal clock ϕ can be output from port P6₃ by setting the ϕ output control register.

At ϕ clock output, set "1" to the bit 3 of the port P6 direction register.

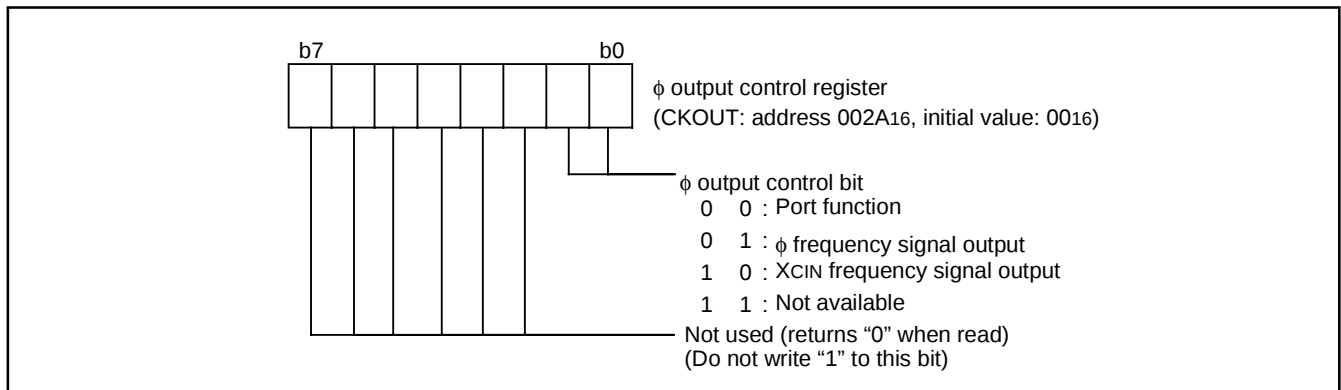


Fig. 35 Structure of clock output control register

● Temporary data register

The temporary data register (addresses 002C₁₆ to 002E₁₆) is the 8-bit register and does not have the control function. It can be used to store data temporarily. It is initialized after reset.

● RRF register

The RRF register (address 002F₁₆) is the 8-bit register and does not have the control function.

As for the value written in this register, high-order 4 bits and low-order 4 bits interchange.

It is initialized after reset.

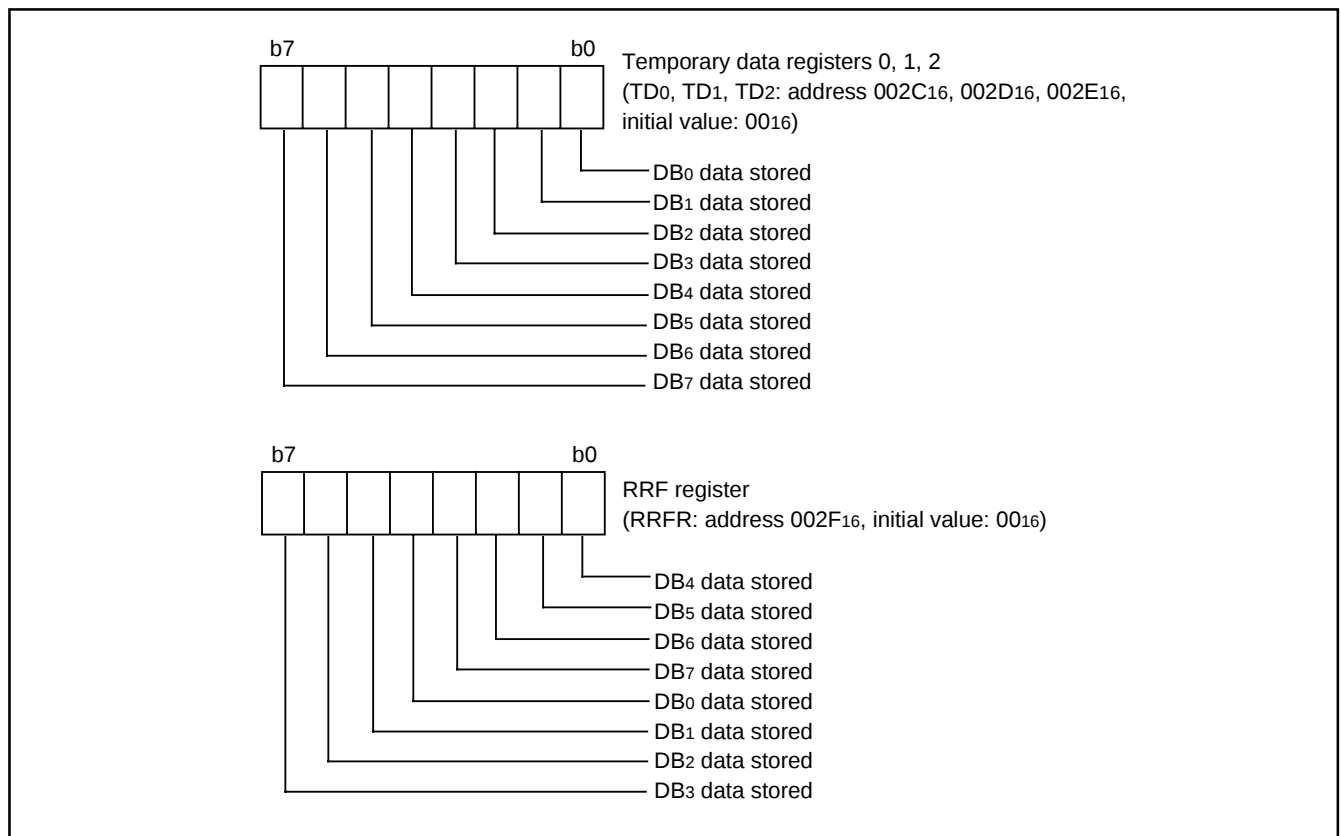


Fig. 36 Structure of temporary data register, RRF register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between $V_{\text{CC}}(\text{min.})$ and 5.5 V), reset is released. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order byte) and address FFFC_{16} (low-order byte). Make sure that the reset input voltage is less than 0.2 V_{CC} for V_{CC} of $V_{\text{CC}}(\text{min.})$.

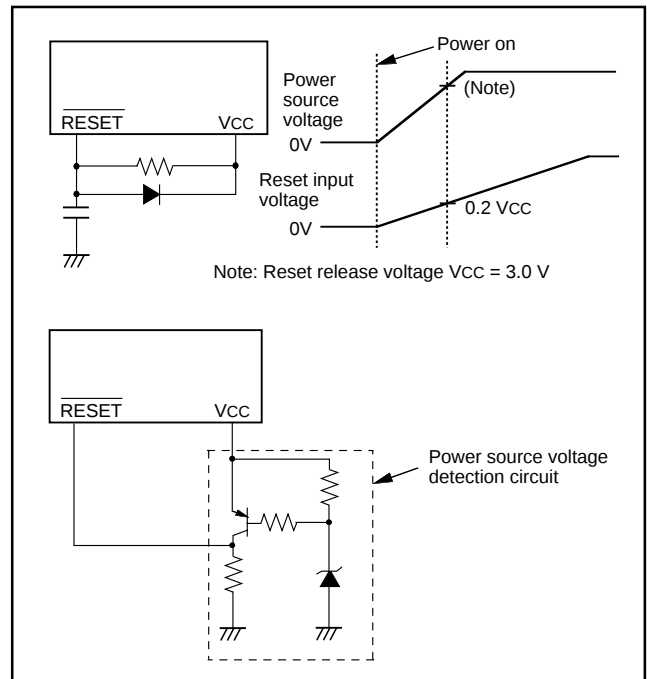


Fig. 37 Example of reset circuit

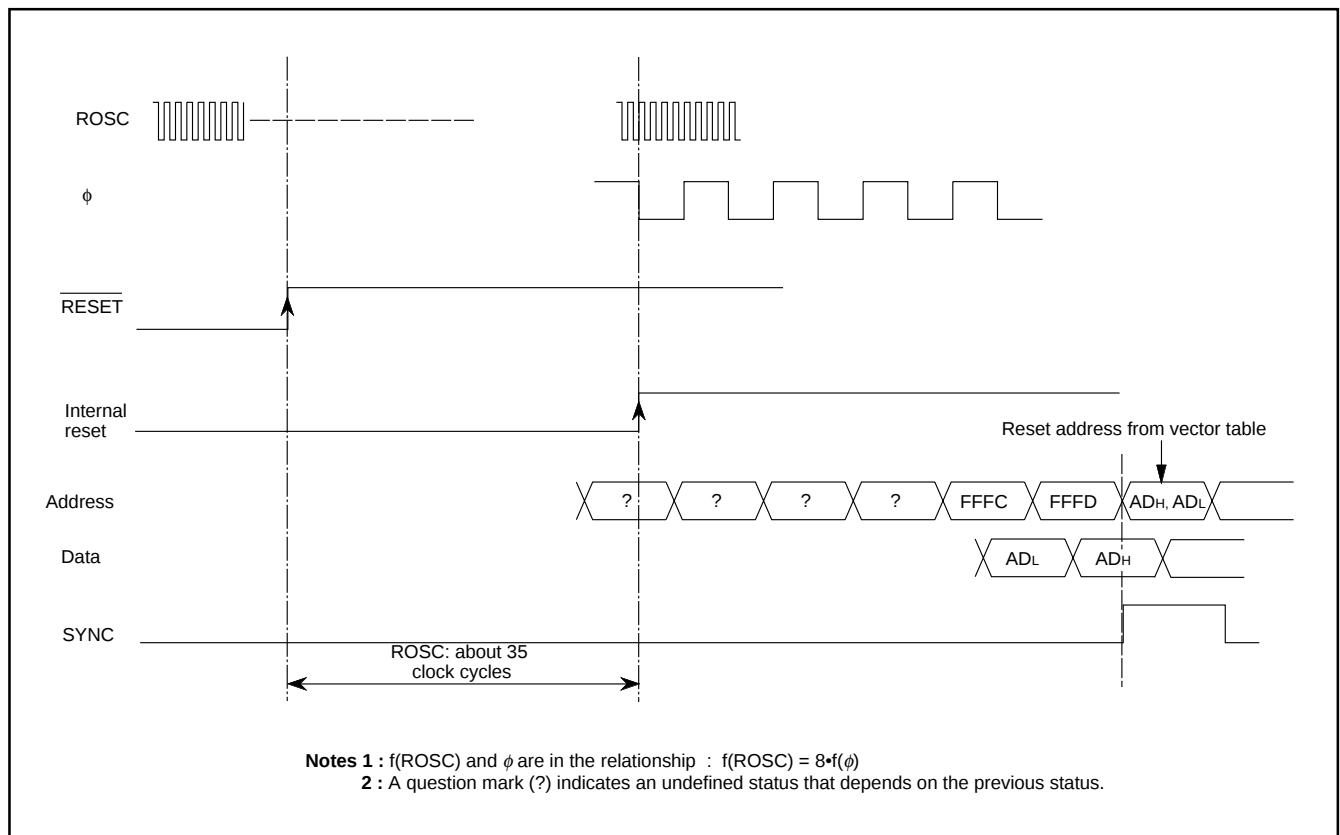


Fig. 38 Reset Sequence

	Address	Register contents
(1) Port P2 direction register	0005 ₁₆	00 ₁₆
(2) Port P3 direction register	0007 ₁₆	00 ₁₆
(3) Port P4 direction register	0009 ₁₆	00 ₁₆
(4) Port P5 direction register	000B ₁₆	00 ₁₆
(5) Port P6 direction register	000D ₁₆	00 ₁₆
(6) Serial I/O control register	001D ₁₆	00 ₁₆
(7) Timer X (low)	0020 ₁₆	FF ₁₆
(8) Timer X (high)	0021 ₁₆	FF ₁₆
(9) Timer Y (low)	0022 ₁₆	FF ₁₆
(10) Timer Y (high)	0023 ₁₆	FF ₁₆
(11) Timer 1	0024 ₁₆	10 ₁₆
(12) Timer 2	0025 ₁₆	FF ₁₆
(13) Timer 3	0026 ₁₆	FF ₁₆
(14) Timer X mode register	0027 ₁₆	00 ₁₆
(15) Timer Y mode register	0028 ₁₆	00 ₁₆
(16) Timer 123 mode register	0029 ₁₆	00 ₁₆
(17) φ output control register	002A ₁₆	00 ₁₆
(18) Temporary data register 0	002C ₁₆	00 ₁₆
(19) Temporary data register 1	002D ₁₆	00 ₁₆
(20) Temporary data register 2	002E ₁₆	00 ₁₆
(21) RRF register	002F ₁₆	00 ₁₆
(22) PULL register	0033 ₁₆	07 ₁₆
(23) A-D control register	0034 ₁₆	08 ₁₆
(24) Segment output enable register	0038 ₁₆	00 ₁₆
(25) LCD mode register	0039 ₁₆	00 ₁₆
(26) Interrupt edge selection register	003A ₁₆	00 ₁₆
(27) CPU mode register	003B ₁₆	68 ₁₆
(28) Interrupt request register 1	003C ₁₆	00 ₁₆
(29) Interrupt request register 2	003D ₁₆	00 ₁₆
(30) Interrupt control register 1	003E ₁₆	00 ₁₆
(31) Interrupt control register 2	003F ₁₆	00 ₁₆
(32) Processor status register	(PS)	X X X X X 1 X X
(33) Program counter	(PCH)	Contents of address FFFD ₁₆
	(PCL)	Contents of address FFFC ₁₆

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.

X : Undefined

Fig. 39 Internal state of microcomputer immediately after reset

CLOCK GENERATING CIRCUIT

The oscillation circuit of 38C1 group can be formed by connecting an oscillator, capacitor and resistor between XIN and XOUT (XCIN and XCOUT). To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The clocks that are externally generated cannot be directly input to XCIN. Use the circuit constants in accordance with the oscillator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, a 10 MΩ external feed-back resistor is needed between XCIN and XCOUT. Immediately after reset is released, only the built-in ring oscillator starts oscillating, XIN-XOUT oscillation stops oscillating, and XCIN and XCOUT pins function as I/O ports.

Operation mode

(1) Ring oscillator mode

The internal clock ϕ is the built-in ring oscillator oscillation divided by 8.

(2) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8.

(3) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(4) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

After reset release and when system returns from the stop mode, the ring oscillator mode is selected.

Refer to the clock state transition diagram for the setting of transition to each mode.

The XIN-XOUT oscillation is controlled by the bit 5 of CPUM, and the sub-clock oscillation is controlled by the bit 4 of CPUM. When the mode is switched to the ring oscillator mode, set the bit 3 of CPUM to "1".

In the ring oscillator mode, the oscillation by the oscillator can be stopped. In the low-speed mode, the power consumption can be reduced by stopping the XIN-XOUT oscillation.

When the mode is switched from the ring oscillator mode to the low-speed mode, the built-in ring oscillator is stopped.

Set enough time for oscillation to stabilize by programming to restart the stopped oscillation and switch the operation mode. Also, set enough time for oscillation to stabilize by programming to switch the timer count source.

Note: If you switch the mode between ring oscillator mode, middle/high-speed mode and low-speed mode, stabilize both XIN and XCIN oscillations. Especially be careful immediately after power-on and at returning from stop mode. Refer to the clock state transition diagram for the setting of transition to each mode. Set the frequency in the condition that $f(XIN) > 3 \cdot f(XCIN)$.

When the middle- and high-speed mode are not used (XIN-XOUT oscillation and external clock input are not performed), connect XIN to VCC through a resistor.

Oscillation Control

(1) Stop mode

Set the timer 1 interrupt enable bit to disabled ("0") before executing the STP instruction. If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and main clock, ring oscillator and sub-clock oscillators stop.

In this time, "0116" is set to timer 1 and the ring oscillator is connected forcibly for the system clock and the timer 1 count source. Also, the bits of the timer 123 mode register except bit 4 are cleared to "0".

When an external interrupt is received, the clock oscillated before stop mode and the ring oscillator start oscillating.

However, bit 3 of CPUM is set to "1" forcibly and system returns to the ring oscillator mode.

The internal clock ϕ is supplied to the CPU after timer 1 underflows. However, when the system clock is switched from the ring oscillator to main clock and sub-clock, generate the wait time enough for oscillation stabilizing by program.

(2) Wait mode

If the WIT instruction is executed, only the internal clock ϕ stops at an "H" level. The states of main clock, ring oscillator and sub-clock are the same as the state before the executing the WIT instruction and the oscillation does not stop. Since the internal clock ϕ restarts when an interrupt is received, the instruction is executed immediately.

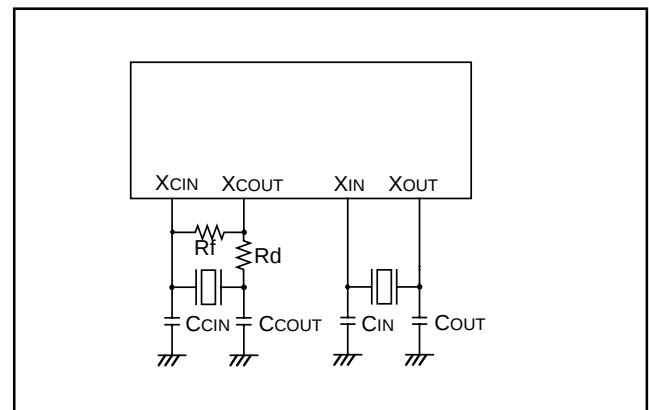


Fig. 40 Oscillator circuit

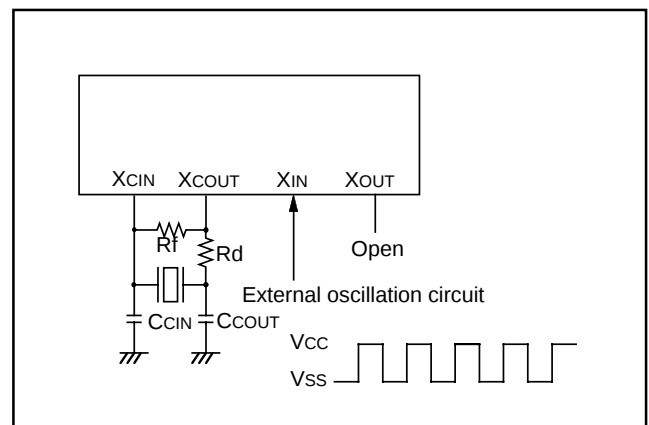
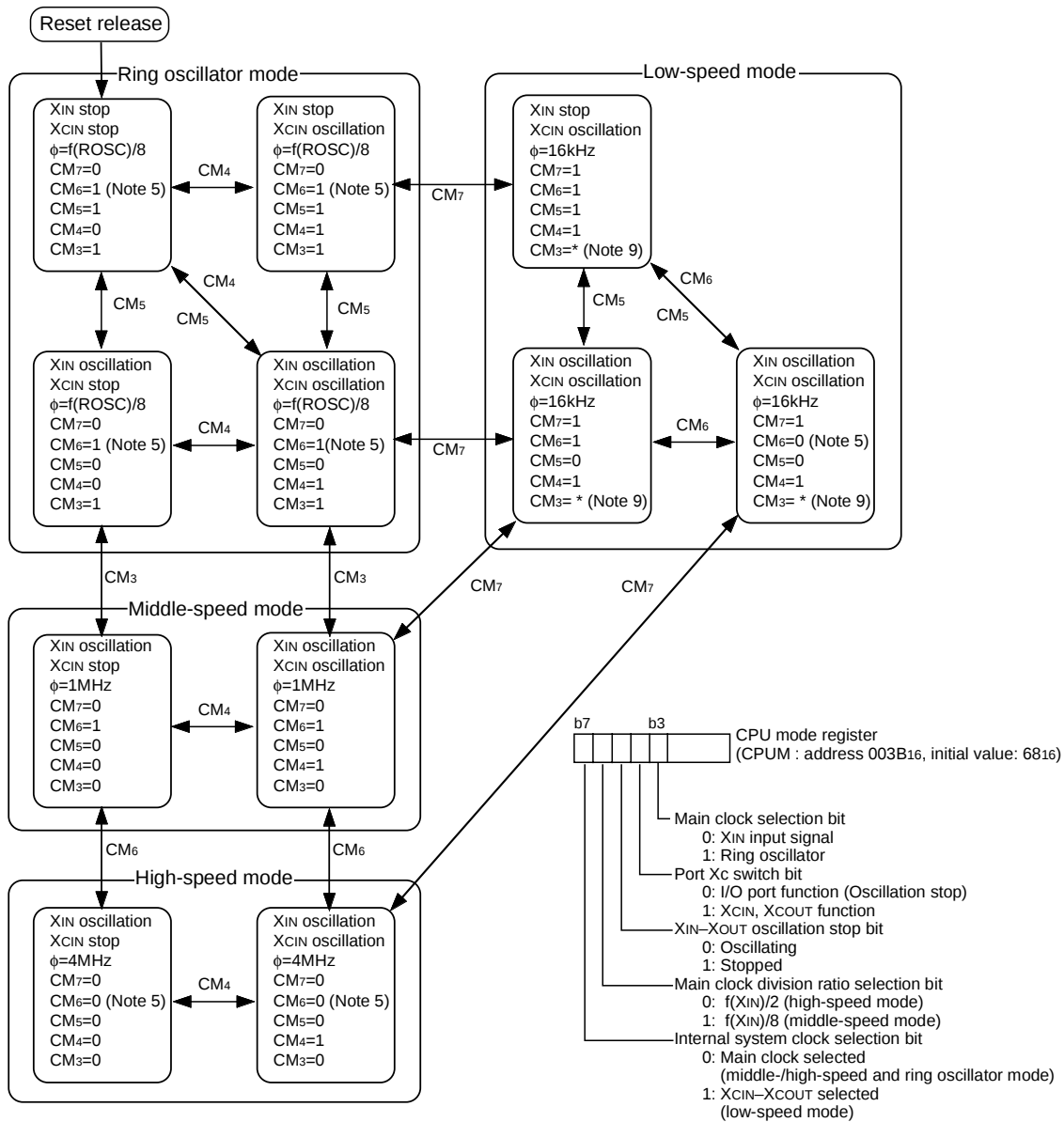


Fig. 41 External clock input circuit

Fig. 42 Clock generating circuit block diagram



Notes 1: Switch the mode by the arrows shown between the mode blocks.

The all modes can be switched to the stop mode or the wait mode.

2: Timer and LCD operate in the wait mode. System is returned to the source mode when the wait mode is ended.

3: CM4, CM5 and CM6 are retained in the stop mode. System is returned to the ring oscillator mode (CM3=1, CM7=0).

4: When the stop mode is ended, set the oscillation stabilizing wait time in the ring oscillator mode.

5: When the stop mode is ended, set the initial value to CM6 (CM6=1).

6: Execute the transition after the oscillation used in the destination mode is stabilized.

7: When system goes to ring oscillator mode, the oscillation stabilizing wait time is not needed.

8: Do not go to the high-speed mode from the ring oscillator mode.

9: Write the proper values for destination mode beforehand.

10: The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin.

$f(\text{ROSC})$ indicates the oscillation frequency of ring oscillator.

Fig. 43 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution.

In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n + 1)$.

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.

The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".

In serial I/O, the SOUT pin goes to high impedance state after transmission is completed.

A-D Converter

The comparator is constructed linked to a capacitor. The conversion accuracy may be low because the charge is lost if the conversion speed is not enough.

Accordingly, set $f(\text{XIN})$ to at least 500kHz during A-D conversion in the middle- or high-speed mode.

Also, do not execute the STP or WIT instruction during an A-D conversion.

In the low-speed mode, since the A-D conversion is executed by the built-in self-oscillation circuit, the minimum value of $f(\text{XIN})$ frequency is not limited.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the XIN frequency.

NOTES ON USE

VL3 pin

When LCD drive control circuit is not used, connect VL3 to Vcc.

Countermeasures against noise

(1) Shortest wiring length

① Wiring for RESET pin

Make the length of wiring which is connected to the RESET pin as short as possible. Especially, connect a capacitor across the RESET pin and the Vss pin with the shortest possible wiring (within 20mm).

● Reason

The width of a pulse input into the RESET pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the RESET pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

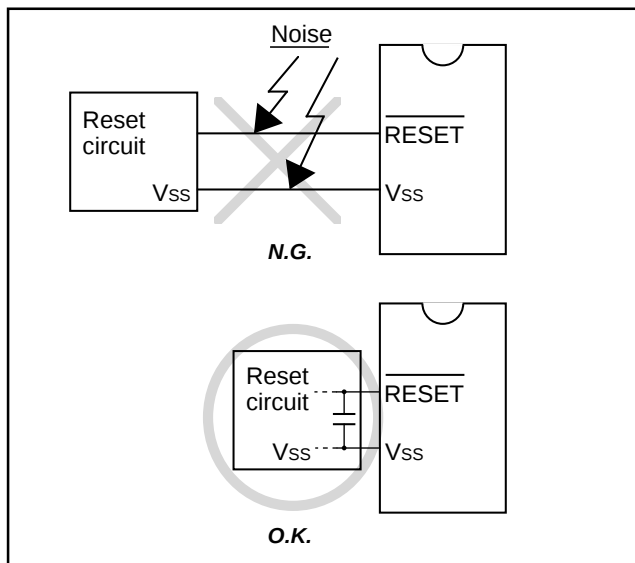


Fig. 44 Wiring for the RESET pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

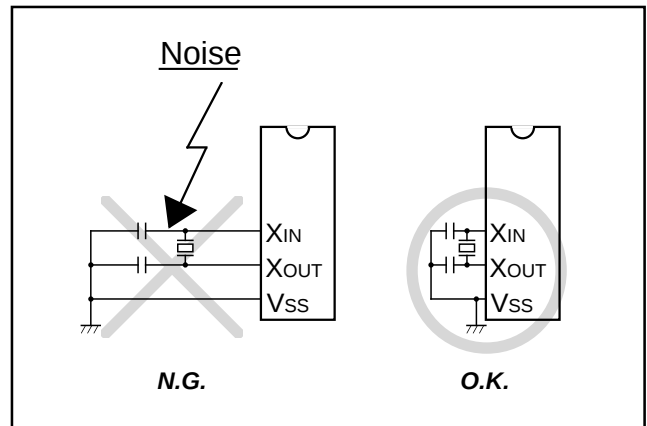


Fig. 45 Wiring for clock I/O pins

(2) Connection of bypass capacitor across Vss line and Vcc line
In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 μ F bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

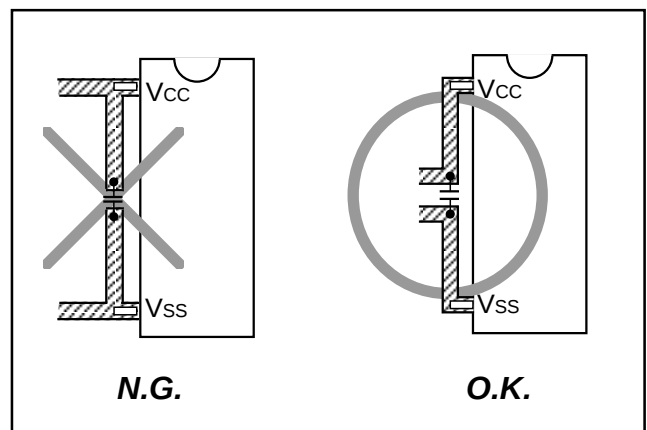


Fig. 46 Bypass capacitor across the Vss line and the Vcc line

(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of voltage or/and temperature is wide.

Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

① Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

② Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

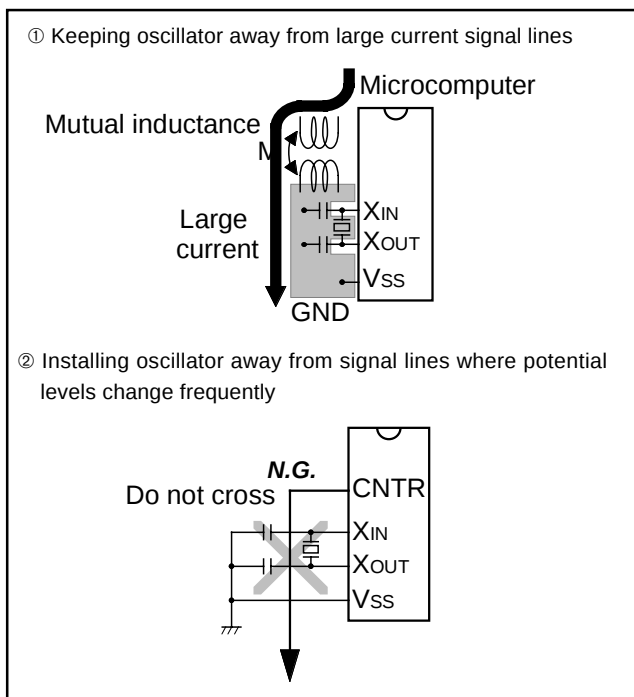


Fig. 47 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A-D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A-D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory type and size

When Mask ROM and PROM version and memory size differ in one group, actual values such as an electrical characteristics, A-D conversion accuracy, and the amount of -proof of noise incorrect operation may differ from the ideal values.

When these products are used switching, perform system evaluation for each product of every after confirming product specification.

(6) Wiring to VPP pin of One Time PROM version

Connect an approximately 5 kΩ resistor to the VPP pin the shortest possible in series and also to the VSS pin.

Note: Even when a circuit which included an approximately 5 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason

The VPP pin of the One Time PROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for writing flow into the built-in PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

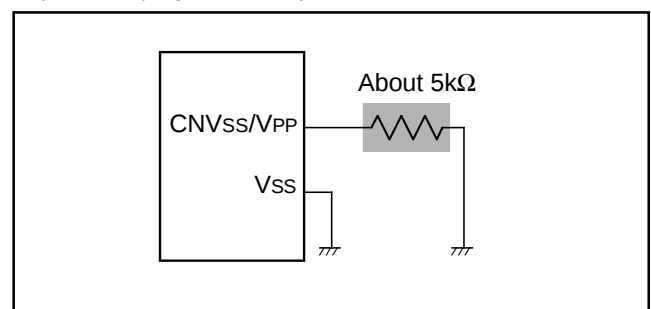


Fig. 48 Wiring for the VPP pin of One Time PROM

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- 1.Mask ROM Order Confirmation Form*
- 2.Mark Specification Form*
- 3.Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

*For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage (<http://www.infocom.maec.co.jp/indexe.htm>).

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version (M38C13E6FP/HP) can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 10. Programming adapter

Package	Name of Programming Adapter
M38C13E6FP	PCA7438F-64A
M38C13E6HP	PCA7438H-64A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 49 is recommended to verify programming.

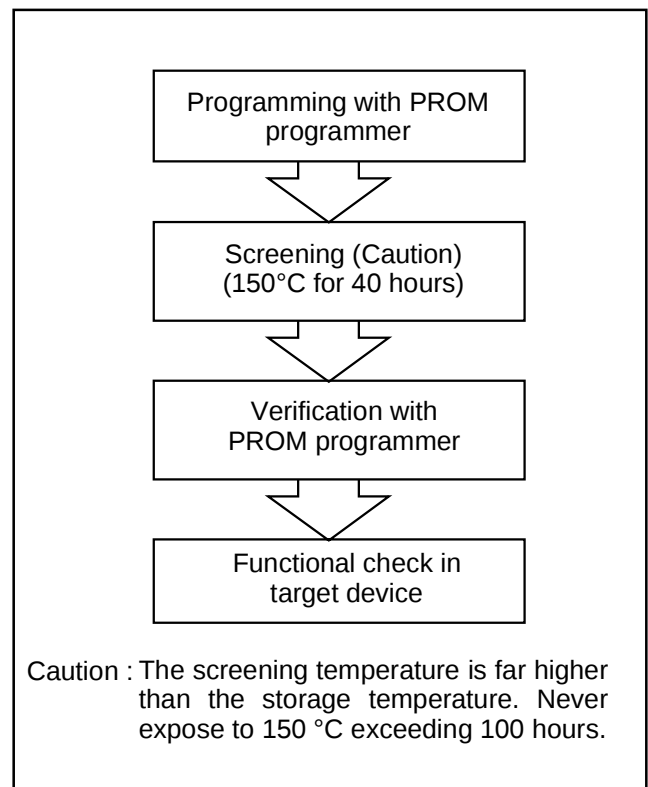


Fig. 49 Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Table 11 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Power source voltage	All voltages are based on V _{SS} . Output transistors are cut off.	−0.3 to 6.5	V
V _I	Input voltage P00–P07, P20–P27, P30–P34, P44–P47, P50–P57, P60–P64		−0.3 to V _{CC} +0.3	V
V _I	Input voltage V _{L1}		−0.3 to V _{L2}	V
V _I	Input voltage V _{L2}		V _{L1} to V _{L3}	V
V _I	Input voltage V _{L3}		V _{L2} to 6.5	V
V _I	Input voltage $\overline{\text{RESET}}$, X _{IN}		−0.3 to V _{CC} +0.3	V
V _I	Input voltage AN ₀ –AN ₃		−0.3 to V _{CC} +0.3	V
V _I	Input voltage CNV _{SS} (Mask ROM version)		−0.3 to V _{CC} +0.3	V
V _I	Input voltage CNV _{SS} (One Time PROM version)		−0.3 to 13	V
V _O	Output voltage P20–P27	At output port	−0.3 to V _{CC} +0.3	V
		At segment output	−0.3 to V _{L3} +0.3	V
V _O	Output voltage P30–P34, P44–P47, P50–P57, P60–P64		−0.3 to V _{CC} +0.3	V
V _O	Output voltage SEG ₀ –SEG ₂₄		−0.3 to V _{L3} +0.3	V
V _O	Output voltage X _{OUT}		−0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _a = 25°C	300	mW
T _{opr}	Operating temperature		−20 to 85	°C
T _{stg}	Storage temperature		−40 to 125	°C

Recommended Operating Conditions

Table 12 Recommended operating conditions

(V_{cc} = 1.8 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
Vcc	Power source voltage (Note 1)	High-speed mode	f(XIN) ≤ 8 MHz	4.0	5.0	5.5	V
			f(XIN) ≤ 6 MHz	3.0	5.0	5.5	V
	Mask ROM version	High-speed mode	f(XIN) ≤ 4 MHz	2.0	5.0	5.5	V
		Middle-speed mode	f(XIN) ≤ 8 MHz	2.0	5.0	5.5	V
			f(XIN) ≤ 6 MHz	1.8	5.0	5.5	V
		Low-speed, ring oscillator operation mode		1.8	5.0	5.5	V
	One Time PROM version	High-speed mode	f(XIN) ≤ 4 MHz	2.5	5.0	5.5	V
		Middle-speed mode	f(XIN) ≤ 8 MHz	2.5	5.0	5.5	V
			f(XIN) ≤ 6 MHz	2.2	5.0	5.5	V
		Low-speed, ring oscillator operation mode		2.2	5.0	5.5	V
When oscillation starts (Note 2)	Mask ROM version		2.2	5.0	5.5	V	
	One Time PROM version		2.5	5.0	5.5	V	
Vss	Power source voltage				0		V
CNVss					0	0.2Vcc	V
VL3	LCD power source voltage			2.5			V
VIA	Analog input voltage AN0–AN7			Vss		Vcc	V
VIH	“H” input voltage		P00–P07, P20–P27, P44–P47, P55, P57, P62–P64	0.7Vcc		Vcc	V
VIH	“H” input voltage		P60, P61 (CM4=0)	0.7Vcc		Vcc	V
VIH	“H” input voltage		P30–P34, P50–P54, P56	0.8Vcc		Vcc	V
VIH	“H” input voltage		RESET	0.8Vcc		Vcc	V
VIH	“H” input voltage		XIN	0.8Vcc		Vcc	V
VIL	“L” input voltage		P00–P07, P20–P27, P44–P47, P55, P57, P62–P64	0		0.3Vcc	V
VIL	“L” input voltage		P60, P61 (CM4=0)	0		0.3Vcc	V
VIL	“L” input voltage		P30–P34, P50–P54, P56	0		0.2Vcc	V
VIL	“L” input voltage		RESET	0		0.2Vcc	V
VIL	“L” input voltage		XIN	0		0.2Vcc	V

Notes 1: When the A-D converter is used, refer to the recommended operating condition for A-D conversion.

2: Oscillation start voltage and oscillation start time depend on the oscillator, the circuit constant and temperature. Especially, be careful that an oscillation start of the high-frequency oscillator may be difficult at low-voltage. Until the oscillation is stabilized, wait in the ring oscillator mode.

Table 13 Recommended operating conditions

(Vcc = 1.8 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$\Sigma I_{OH}(\text{peak})$	"H" total peak output current (Note 1) P20-P27, P30-P34			-40	mA
$\Sigma I_{OH}(\text{peak})$	"H" total peak output current (Note 1) P44-P47, P50-P57, P60-P64			-60	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P20-P27, P30-P34			80	mA
$\Sigma I_{OL}(\text{peak})$	"L" total peak output current (Note 1) P44-P47, P50-P57, P60-P64			60	mA
$\Sigma I_{OH}(\text{avg})$	"H" total average output current (Note 1) P20-P27, P30-P34			-20	mA
$\Sigma I_{OH}(\text{avg})$	"H" total average output current (Note 1) P44-P47, P50-P57, P60-P64			-30	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P20-P27, P30-P34			40	mA
$\Sigma I_{OL}(\text{avg})$	"L" total average output current (Note 1) P44-P47, P50-P57, P60-P64			30	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P20-P27			-2	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P30-P34			-5	mA
$I_{OH}(\text{peak})$	"H" peak output current (Note 2) P44-P47, P50-P57, P60-P64			-5	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P20-P27			5	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P30-P34			30	mA
$I_{OL}(\text{peak})$	"L" peak output current (Note 2) P44-P47, P50-P57, P60-P64			10	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P20-P27			-1.0	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P30-P34			-2.5	mA
$I_{OH}(\text{avg})$	"H" average output current (Note 3) P44-P47, P50-P57, P60-P64			-2.5	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P20-P27			2.5	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P30-P34			15	mA
$I_{OL}(\text{avg})$	"L" average output current (Note 3) P44-P47, P50-P57, P60-P64			5	mA

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is average value measured over 100 ms.

Table 14 Recommended operating conditions

(Vcc = 1.8 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
f(CNTR0)	Timer X and Timer Y	(4.0 V ≤ Vcc ≤ 5.5 V)			4.0	MHz
f(CNTR1)	Input frequency (duty cycle 50%)	(Mask ROM version: 2.0V ≤ Vcc ≤ 4.0 V)			Vcc	MHz
		(One Time PROM version: 3.0 V ≤ Vcc ≤ 4.0 V)				MHz
		(Mask ROM version: Vcc ≤ 2.0 V)			5XVcc-8	MHz
		(One Time PROM version: 2.5 V ≤ Vcc ≤ 3.0 V)			2XVcc-3	MHz
		(One Time PROM version: Vcc ≤ 2.5 V)			$\frac{10XVcc-19}{3}$	MHz
f(XIN)	Main clock input frequency (duty cycle 50%) (Note 1)	High-speed mode (4.0 V < Vcc ≤ 5.5 V)			8.0	MHz
		High-speed mode (Mask ROM version: 2.0V ≤ Vcc ≤ 4.0 V) (One Time PROM version: 3.0 V ≤ Vcc ≤ 4.0 V)			2XVcc	MHz
		High-speed mode (One Time PROM version: 2.5 V ≤ Vcc ≤ 3.0 V)			4XVcc-6	MHz
		Middle-speed mode (Note 3) (Note 4) (Mask ROM version: 2.0 V ≤ Vcc ≤ 5.5 V) (One Time PROM version: 2.5 V ≤ Vcc ≤ 5.5 V)			8.0	MHz
		Middle-speed mode (Note 3) (Note 4)			6.0	MHz
f(XCIN)	Sub-clock input oscillation frequency (Note 2) (Note 4) (duty cycle 50%)			32.768	80	kHz

Notes 1: When the A-D converter is used, refer to the recommended operating condition for A-D conversion.

2: When using the microcomputer in low-speed mode, set the clock input oscillation frequency on condition that f(XCIN) < f(XIN)/3.

3: When the timer X count source selection bit is set to "1", as for the recommended operating condition of the main clock input frequency f(XIN), the rating value at the high-speed mode is applied.

4: Oscillation start voltage and oscillation start time depend on the oscillator, the circuit constant and temperature.
 Especially, be careful that an oscillation start of the high-frequency oscillator may be difficult at low-voltage.
 Until the oscillation is stabilized, wait in the ring oscillator mode.

Electrical Characteristics

Table 15 Electrical characteristics

(V_{CC} = 4.0 to 5.5 V, T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V _{OH}	“H” output voltage P20–P27	I _{OH} = -1.0 mA	V _{CC} -2.0			V
		I _{OH} = -0.2 mA	V _{CC} -0.8			V
		V _{CC} = 1.8 to 5.5 V (Note)				
V _{OH}	“H” output voltage P30–P34, P44–P47, P50–P57, P60–P64	I _{OH} = -2.5 mA	V _{CC} -2.0			V
		I _{OH} = -0.5 mA	V _{CC} -0.8			V
		V _{CC} = 1.8 to 5.5 V (Note)				
V _{OL}	“L” output voltage P20–P27	I _{OL} = 2.5 mA			2.0	V
		I _{OL} = 0.5 mA			0.8	V
		V _{CC} = 1.8 to 5.5 V (Note)				
V _{OL}	“L” output voltage P44–P47, P50–P57, P60–P64	I _{OL} = 5 mA			2.0	V
		I _{OL} = 1 mA			0.8	V
		V _{CC} = 1.8 to 5.5 V (Note)				
V _{OL}	“L” output voltage P30–P34	I _{OL} = 15 mA			2.0	V
		I _{OL} = 3 mA			0.8	V
		V _{CC} = 1.8 to 5.5 V (Note)				
V _{T+} –V _{T-}	Hysteresis INT0, INT1, CNTR0, CNTR1, P30–P34			0.5		V
V _{T+} –V _{T-}	Hysteresis SCLK, SIN			0.5		V
V _{T+} –V _{T-}	Hysteresis RESET			0.5		V
I _{IH}	“H” input current P30–P34, P44–P47, P50–P57, P60–P64	V _I = V _{CC}			5.0	μA
I _{IH}	“H” input current P00–P07, P20–P27	V _I = V _{SS} Pull-down “OFF”			5.0	μA
		V _{CC} = 5.0 V, V _I = V _{CC} Pull-down “ON”	60	120	240	μA
		V _{CC} = 3.0 V, V _I = V _{CC} Pull-down “ON”	25	50	100	μA
I _{IH}	“H” input current RESET, AN0–AN3	V _I = V _{CC}			5.0	μA
I _{IH}	“H” input current X _{IN}	V _I = V _{CC}		4.0		μA
I _{IL}	“L” input current P00–P07, P20–P27	V _I = V _{SS}			-5.0	μA
I _{IL}	“L” input current P30–P34, P44–P47, P50–P57, P60–P64	V _I = V _{SS} Pull-up “OFF”			-5.0	μA
		V _{CC} = 5.0 V, V _I = V _{SS} Pull-up “ON”	-60	-120	-240	μA
		V _{CC} = 3.0 V, V _I = V _{SS} Pull-up “ON”	-25	-50	-100	μA
I _{IL}	“L” input current RESET, CNV _{SS} , AN0–AN3	V _I = V _{SS}			-5.0	μA
I _{IL}	“L” input current X _{IN}	V _I = V _{SS}		-4.0		μA
VRAM	RAM hold voltage (Mask ROM version)	At clock stop	1.8		5.5	V
	RAM hold voltage (One Time PROM version)	At clock stop	2.2		5.5	V
ROSC	Ring oscillator oscillation frequency	V _{CC} = 5.0 V, T _a = 25 °C	2500	5000	7500	kHz

Note: One Time PROM version: 2.2 to 5.5 V.

Table 16 Electrical characteristics

(Vcc = 1.8 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), Ta = -20 to 85°C, f(XCIN) = 32.768 kHz, output transistors "OFF", AD converter stopped, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
Icc	Power source current	High-speed mode	Vcc = 5 V	f(XIN) = 8 MHz		3.0	6.0	mA
			Mask ROM version	f(XIN) = 8 MHz (in WIT state)		0.8	1.6	mA
				f(XIN) = 4 MHz		1.5	3.0	mA
			Vcc = 5 V	f(XIN) = 8 MHz		4.7	9.4	mA
			One Time PROM version	f(XIN) = 8 MHz (in WIT state)		0.9	1.8	mA
				f(XIN) = 4 MHz		2.5	5.0	mA
			Vcc = 2.5 V	f(XIN) = 4 MHz		0.6	1.2	mA
			Mask ROM version	f(XIN) = 4 MHz (in WIT state)		0.3	0.6	mA
				f(XIN) = 2 MHz		0.4	0.8	mA
			Vcc = 2.5 V	f(XIN) = 4 MHz		0.9	1.8	mA
			One Time PROM version	f(XIN) = 4 MHz (in WIT state)		0.3	0.6	mA
				f(XIN) = 2 MHz		0.6	1.2	mA
		Middle-speed mode	Vcc = 5 V	f(XIN) = 8 MHz		1.2	2.4	mA
			Mask ROM version	f(XIN) = 8 MHz (in WIT state)		0.8	1.6	mA
				f(XIN) = 4 MHz		0.8	1.6	mA
			Vcc = 5 V	f(XIN) = 8 MHz		1.8	3.6	mA
			One Time PROM version	f(XIN) = 8 MHz (in WIT state)		0.9	1.8	mA
				f(XIN) = 4 MHz		1.0	2.0	mA
			Vcc = 2.5 V	f(XIN) = 8 MHz		0.5	1.0	mA
			Mask ROM version	f(XIN) = 8 MHz (in WIT state)		0.3	0.6	mA
				f(XIN) = 4 MHz		0.3	0.6	mA
			Vcc = 2.5 V	f(XIN) = 8 MHz		0.7	1.4	mA
			One Time PROM version	f(XIN) = 8 MHz (in WIT state)		0.4	0.8	mA
				f(XIN) = 4 MHz		0.4	0.8	mA
		Low-speed mode	Vcc = 5 V	f(XIN) = stop		13	26	μA
			Mask ROM version	WIT instruction executed		5.5	11	μA
				Vcc = 5 V	f(XIN) = stop		19	38
			One Time PROM version	WIT instruction executed		6.5	13	μA
				Vcc = 2.5 V	f(XIN) = stop		7.0	14
			Mask ROM version	WIT instruction executed		3.5	7.0	μA
				Vcc = 2.5 V	f(XIN) = stop		10	20
			One Time PROM version	WIT instruction executed		3.5	7	μA
		Ring oscillator mode		Vcc = 5 V		600	1200	μA
		f(XCIN) = stop		Vcc = 2.5 V		90	270	μA
				Vcc = 2.5 V (in WIT state)		30	90	μA
		All oscillations stop (STP instruction executed)		Ta = 25 °C		0.1	1.0	μA
				Ta = 85 °C			10	μA
		Current increased when AD converter is operating		f(XIN) = 8 MHz, Vcc = 5 V at middle-, high-speed mode		0.5		mA
				f(XIN) = stop, Vcc = 5 V at ring oscillator operation mode		0.5		mA
				f(XIN) = stop, Vcc = 5 V at low-speed mode		0.4		mA

A-D Converter Characteristics

Table 17 A-D converter recommended operating condition

(V_{CC} = 2.0 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit		
				Min.	Typ.	Max.			
V _{DD}	Power source voltage	Mask ROM version		2.0	5.0	5.5	V		
		One Time PROM version		2.2	5.0	5.5	V		
V _{IH}	“H” input voltage ADKEY ₀ –ADKEY ₃			0.9V _{CC}		V _{CC}	V		
V _{IL}	“L” input voltage ADKEY ₀ –ADKEY ₃			0		0.7V _{CC} X–0.5	V		
f(X _{IN})	AD converter control clock (low-speed mode and ring oscillator mode excluded)	Mask ROM version	V _{CC} ≤ 2.2 V			20XV _{CC} –38	MHz		
			2.2 < V _{CC} ≤ 2.5 V			$\frac{20 \times V_{CC} - 26}{3}$			
		One Time PROM version	V _{CC} ≤ 2.5 V			$\frac{40 \times V_{CC} - 82}{3}$	MHz		
			2.5 < V _{CC} ≤ 2.7 V			10XV _{CC} –19			
		Mask ROM version		2.5 < V _{CC} ≤ 5.5 V				8.0	MHz
		One Time PROM version		2.7 < V _{CC} ≤ 5.5 V					

Table 18 A-D converter characteristics

(V_{CC} = 2.0 to 5.5 V (One Time PROM version: 2.2 to 5.5 V), T_a = -20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	BIT
LIN	Linearity error	T _a = 25 °C, 2.5 ≤ V _{CC} ≤ 5.5 V			±1	LSB
DIF	Differential non-linearity error	T _a = 25 °C, 2.5 ≤ V _{CC} ≤ 5.5 V			±0.9	LSB
V _{0T}	Zero transition voltage	V _{CC} = 5.12 V, T _a = 25 °C	0	20	50	mV
		V _{CC} = 2.56 V, T _a = 25 °C	0	10	25	mV
V _{FST}	Full-scale transition voltage	V _{CC} = 5.12 V, T _a = 25 °C	5070	5100	5120	mV
		V _{CC} = 2.56 V, T _a = 25 °C	2535	2550	2560	mV
ABS	Absolute accuracy (quantification error excluded)	2.2 < V _{CC} ≤ 5.5 V (2.7 < V _{CC} ≤ 5.5 V for One Time PROM version), f(X _{IN}) ≤ 8.0 MHz, or low-speed or ring oscillator mode			±2	LSB
		2.2 < V _{CC} ≤ 2.5 V (2.5 < V _{CC} ≤ 2.7 V for One Time PROM version), f(X _{IN}) ≤ 2.0 MHz, or low-speed or ring oscillator mode			±2	LSB
		2.2 ≤ V _{CC} < 2.3 V for One Time PROM version Low-speed or ring oscillator mode excluded			±5	LSB
		Condition except above			±3	LSB
T _{conv}	Conversion time (Note)		106		109	tc(φAD)
I _{IA}	Analog input current				±5	μA

Note: The operation clock is X_{IN} in the middle- or high-speed mode, or the ring oscillator in the other modes.

When the A-D conversion is executed in the middle- or high-speed mode, set f(X_{IN}) ≥ 500 kHz.

tc(φAD): One cycle of control clock for A-D converter. X_{IN} input is used in the middle- or high-speed mode, and ring oscillator is used in the low- or ring oscillator mode for the control clock.

Timing Requirements And Switching Characteristics

Table 19 Timing requirements 1

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	125			ns
t _{wH} (X _{IN})	Main clock input "H" pulse width	50			ns
t _{wL} (X _{IN})	Main clock input "L" pulse width	50			ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	250			ns
t _{wH} (CNTR)	CNTR0, CNTR1 input "H" pulse width	105			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input "L" pulse width	105			ns
t _{wH} (INT)	INT0, INT1 input "H" pulse width	80			ns
t _{wL} (INT)	INT0, INT1 input "L" pulse width	80			ns
t _c (SCLK)	Serial I/O clock input cycle time	1000			ns
t _{wH} (SCLK)	Serial I/O clock input "H" pulse width	400			ns
t _{wL} (SCLK)	Serial I/O clock input "L" pulse width	400			ns
t _{su} (S _{IN} -SCLK)	Serial I/O input setup time	200			ns
t _h (SCLK-S _{IN})	Serial I/O input hold time	200			ns

Table 20 Timing requirements 2

(V_{CC} = 1.8 to 4.0 V (2.2 to 4.0 V for One Time PROM version), V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _w (RESET)	Reset input "L" pulse width	2			μs
t _c (X _{IN})	Main clock input cycle time (X _{IN} input)	2.0 V (One Time PROM version: 2.5 V) ≤ V _{CC} ≤ 4.0 V	125		ns
		V _{CC} ≤ 2.0 V (One Time PROM version: 2.5 V)	166		ns
t _{wH} (X _{IN})	Main clock input "H" pulse width	2.0 V (One Time PROM version: 2.5 V) ≤ V _{CC} ≤ 4.0 V	50		ns
		V _{CC} ≤ 2.0 V (One Time PROM version: 2.5 V)	70		ns
t _{wL} (X _{IN})	Main clock input "L" pulse width	2.0 V (One Time PROM version: 2.5 V) ≤ V _{CC} ≤ 4.0 V	50		ns
		V _{CC} ≤ 2.0 V (One Time PROM version: 2.5 V)	70		ns
t _c (CNTR)	CNTR0, CNTR1 input cycle time	2.0 V (One Time PROM version: 2.5 V) ≤ V _{CC} ≤ 4.0 V	1000/V _{CC}		ns
		V _{CC} ≤ 2.0 V (One Time PROM version: 2.5 V)	1000/(5XV _{CC} –8)		ns
t _{wH} (CNTR)	CNTR0, CNTR1 input "H" pulse width	t _c (CNTR)/2–20			ns
t _{wL} (CNTR)	CNTR0, CNTR1 input "L" pulse width	t _c (CNTR)/2–20			ns
t _{wH} (INT)	INT0, INT1 input "H" pulse width	230			ns
t _{wL} (INT)	INT0, INT1 input "L" pulse width	230			ns
t _c (SCLK)	Serial I/O clock input cycle time	2000			ns
t _{wH} (SCLK)	Serial I/O clock input "H" pulse width	950			ns
t _{wL} (SCLK)	Serial I/O clock input "L" pulse width	950			ns
t _{su} (RxD-SCLK)	Serial I/O input setup time	400			ns
t _h (SCLK-RxD)	Serial I/O input hold time	200			ns

Table 21 Switching characteristics 1

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{WH} (SCLK)	Serial I/O clock output "H" pulse width	t _c (SCLK)/2–30			ns
t _{WL} (SCLK)	Serial I/O clock output "L" pulse width	t _c (SCLK)/2–30			ns
t _d (SCLK-SOUT)	Serial I/O output delay time (Note 1)			140	ns
t _v (SCLK-SOUT)	Serial I/O output valid time (Note 1)	–30			ns
t _r (SCLK)	Serial I/O clock output rising time			30	ns
t _f (SCLK)	Serial I/O clock output falling time			30	ns
t _r (CMOS)	CMOS output rising time P20–P27			200	ns
	CMOS output rising time P30–P34, P44–P47, P50–P57, P60–P64 (Note 2)		25	40	ns
t _f (CMOS)	CMOS output falling time (Note 2)		25	40	ns

Notes 1: When the P5s/Sout P-channel output disable bit of the serial I/O control register (bit 4 of address 001D16) is "0."

2: The XOUT, XCOUNT pins are excluded.

Table 22 Switching characteristics 2

(V_{CC} = 1.8 to 4.0 V (2.2 to 4.0 V for One Time PROM version), V_{SS} = 0 V, T_a = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t _{WH} (SCLK)	Serial I/O clock output "H" pulse width	t _c (SCLK)/2–80			ns
t _{WL} (SCLK)	Serial I/O clock output "L" pulse width	t _c (SCLK)/2–80			ns
t _d (SCLK-SOUT)	Serial I/O output delay time (Note 1)			350	ns
t _v (SCLK-SOUT)	Serial I/O output valid time (Note 1)	–30			ns
t _r (SCLK)	Serial I/O clock output rising time			80	ns
t _f (SCLK)	Serial I/O clock output falling time			80	ns
t _r (CMOS)	CMOS output rising time P20–P27			400	ns
	CMOS output rising time P30–P34, P44–P47, P50–P57, P60–P64 (Note 2)		60	120	ns
t _f (CMOS)	CMOS output falling time (Note 2)		60	120	ns

Notes 1: When the P5s/Sout P-channel output disable bit of the serial I/O control register (bit 4 of address 001D16) is "0."

2: The XOUT, XCOUNT pins are excluded.

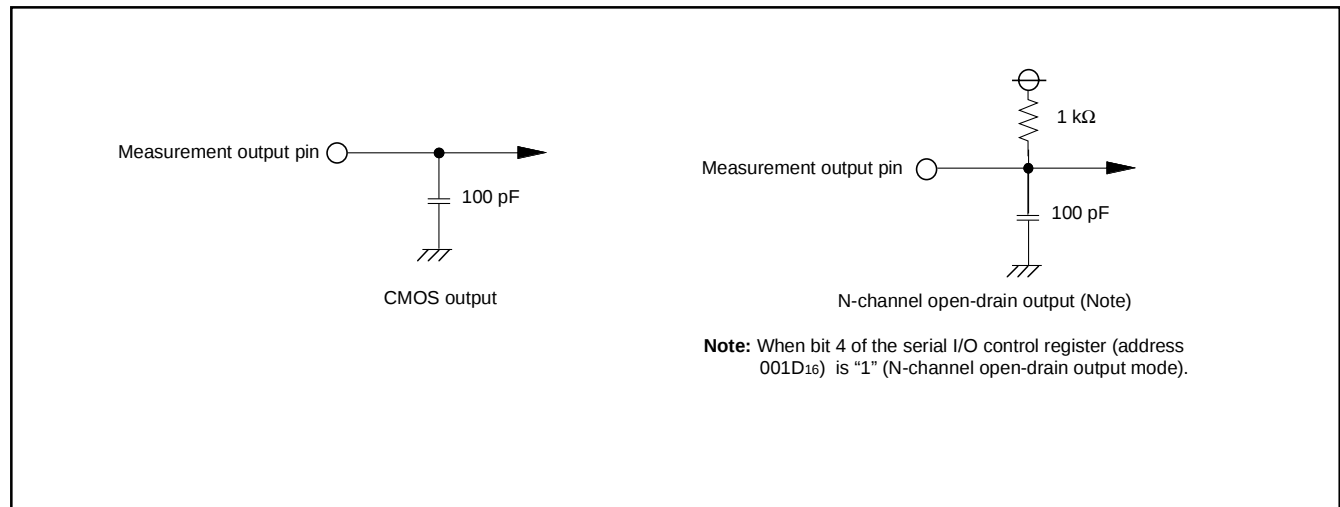


Fig. 50 Circuit for measuring output switching characteristics

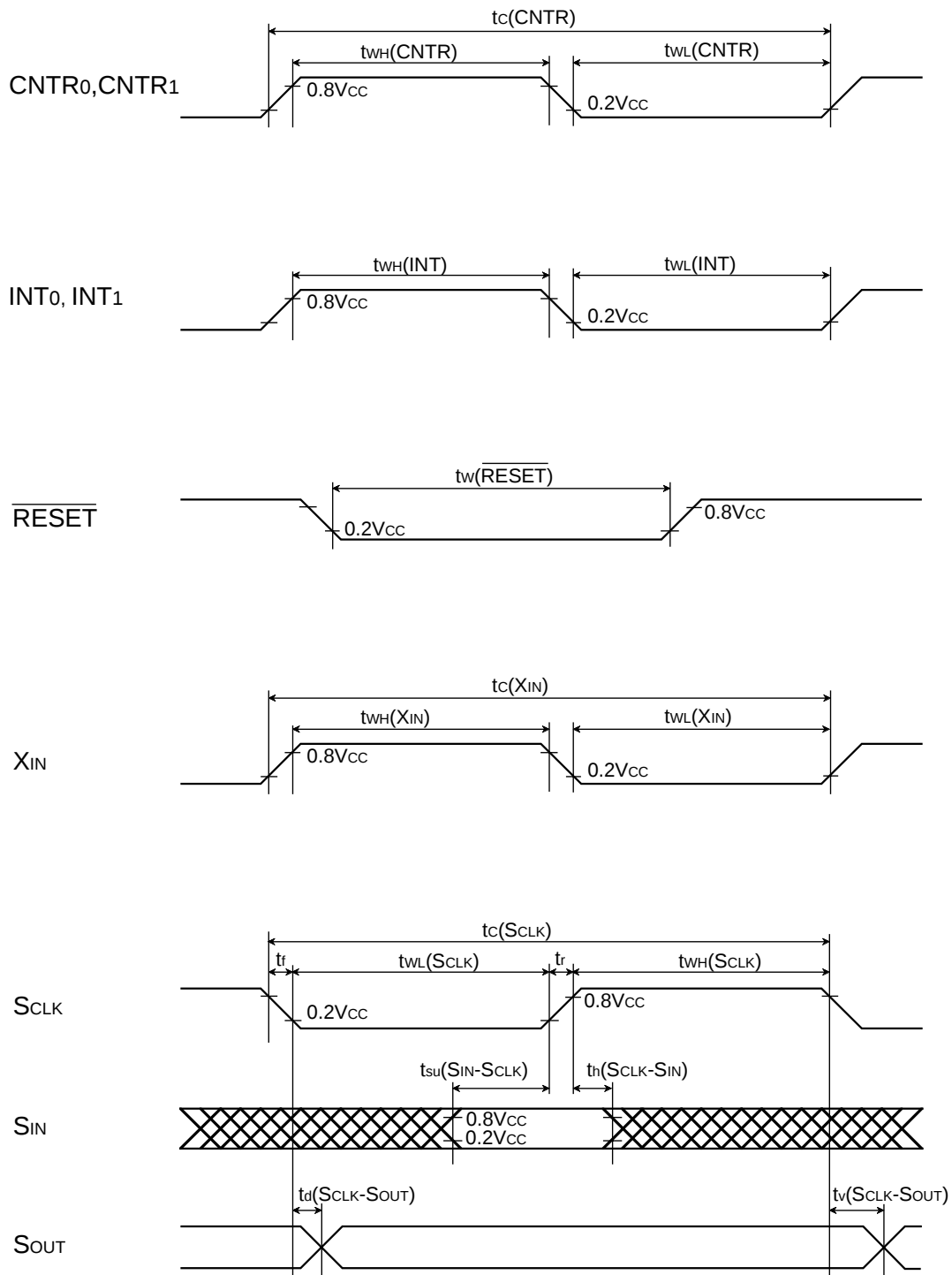


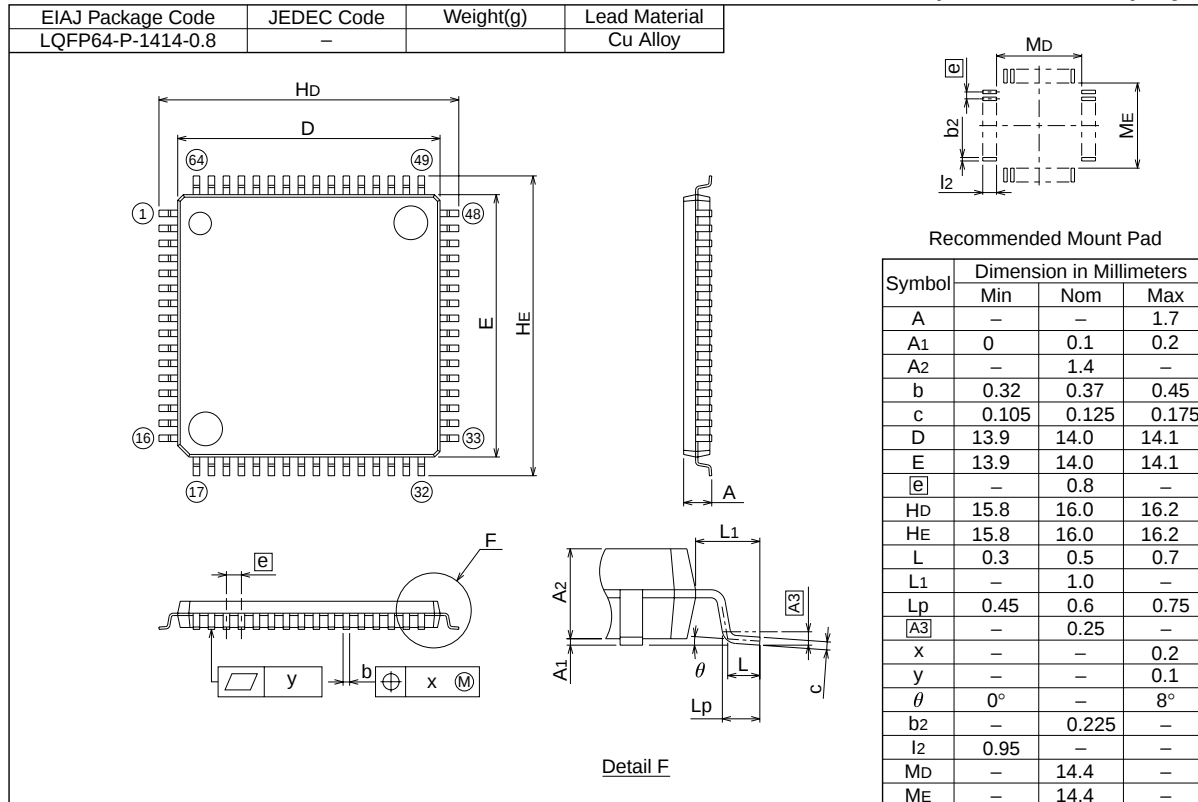
Fig. 51 Timing chart

PACKAGE OUTLINE

64P6U-A

(MMP)

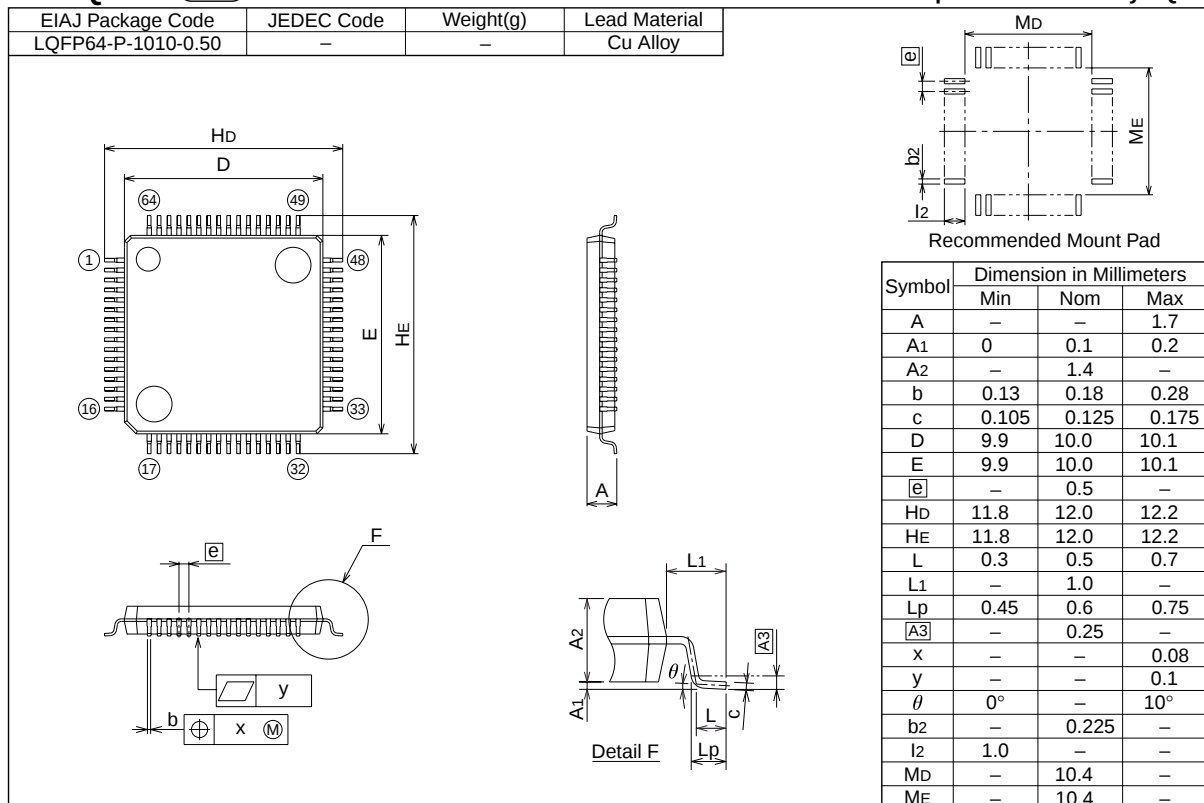
Plastic 64pin 14X14mm body LQFP



64P6Q-A

(MMP)

Plastic 64pin 10X10mm body LQFP





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REVISION HISTORY	38C1 GROUP DATA SHEET
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Rev.	Date	Description	
		Page	Summary
1.0	01/16/02		First Edition
2.0	03/28/02	1	FEATURES; • Interrupts and • Power dissipation revised.
		4	PIN DESCRIPTION; $VL1-VL3$ $0 \leq VL1 \leq VL2 \leq VL3 \rightarrow 0 \leq VL1 \leq VL2 < VL3$
		6	Table 2; Date revised. Jan. $\rightarrow$ Mar.
		10	Fig. 7; Bits 3 and 6 Description added.
		12	Fig. 10; Address 0007_{16} Port P3 <u>direction</u> register (P3D) Address 0008_{16} "ADKEY pin selection" added.
		14	Table 5; Note 2 revised.
		18	INTERRUPTS; <u>fourteen</u> sources $\rightarrow$ <u>thirteen</u> sources, <u>eight</u> internal $\rightarrow$ <u>seven</u> internal
		20	Fig. 17; PULL register A Bit <u>2</u> = "1" $\rightarrow$ PULL register Bit <u>3</u> = "1"
		27	● A-D Converter description added.
		28	A-DKEY Control Circuit; Description revised all. Fig. 27; Figure title and note "pin" added.
		32	Common Pin and Duty Ratio Control; Description added. Table 9; Note revised.
		36	Fig. 35; Bits 0 and 1 Functional description revised. ● RRF register; Description revised.
		41	Fig. 43; Low-speed mode $CM3 = 1 \rightarrow CM3 = *$ (Note 9)
		44	(3) line 5; voltage and temperature $\rightarrow$ voltage <u>or</u> /and temperature
		47 to 54	ELECTRICAL CHARACTERISTICS ; Most contents revised.
		47	Table 12; Vcc revised, VL3 and Notes added.
		49	Table 14; Note revised.
		51	Table 16; Most contents revised.
		52	Table 17; Added. Table 18; Most contents revised.
		53	Table 20; "(2.2 to 4.0 V for One Time PROM version)" added.
		54	Table 22; "(2.2 to 4.0 V for One Time PROM version)" added.
		56	PACKAGE OUTLINE revised.
2.1	05/09/02	6	Fig. 4 and Table 2; Revised.
		10	[CPU Mode Register (CPUM)] ; Description revised.
		16	Fig. 13; Revised.
		22	● Timer X, ■ Note on count source selection bit; Description revised.
		25	Fig. 23; Note revised.
		39	Clock generating circuit; Note revised.
		47	Table 12; "H" input voltage ADKEY0–ADKEY3, "L" input voltage ADKEY0–ADKEY3 eliminated.
		49	Table 14; Note 3 added.
		52	Table 17; "H" input voltage ADKEY0–ADKEY3, "L" input voltage ADKEY0–ADKEY3 added.

