

KA5M0965Q

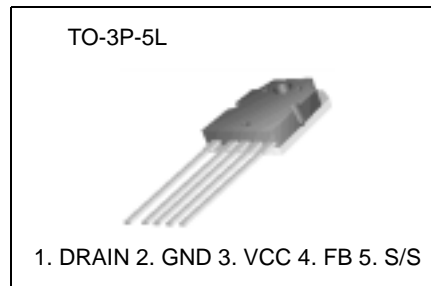
Fairchild Power Switch(SPS)

Features

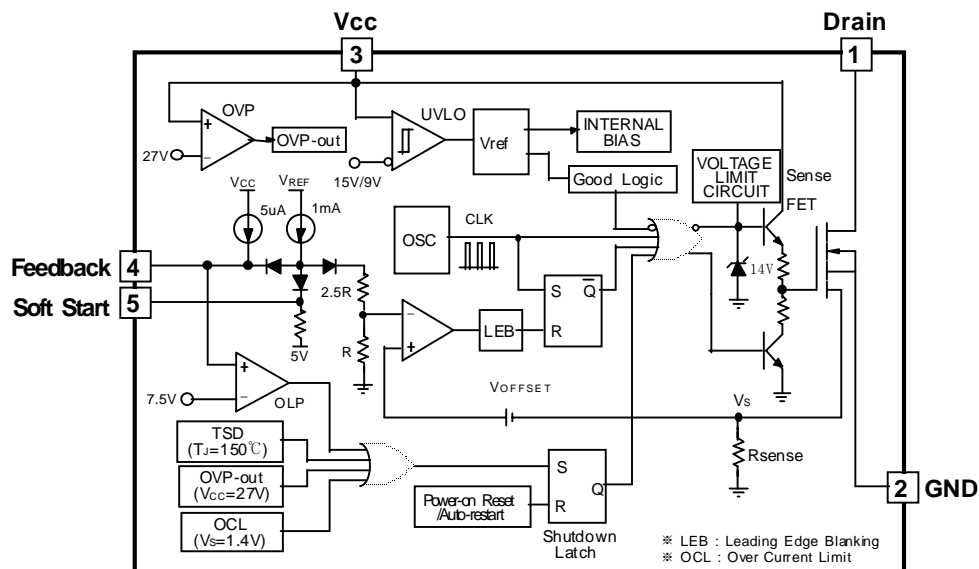
- Precision fixed operating frequency (70kHz)
- Low start-up current(typ. 100uA)
- Pulse by pulse current limiting
- Over Load protection
- Over current protection
- Over voltage protection (Min. 25V)
- Internal thermal shutdown function
- Under voltage lockout
- Internal high voltage sense FET
- Latch mode

Description

The SPS product family is specially designed for an off-line SMPS with minimal external components. The SPS consist of high voltage power SenseFET and current mode PWM IC. Included PWM controller features integrated fixed frequency oscillator, under voltage lock-out, leading edge blanking, optimized gate turn-on/turn-off driver, thermal shutdown protection, over voltage protection, and temperature compensated precision current sources for loopcompensation and fault protection circuitry. Compared to discrete MOSFET and PWM controller or RCC solution, a SPS can reduce total component count, design size, weight and at the same time increase efficiency, productivity, and system reliability. It has a basic platform well suited for cost-effective design in either a flyback converter or a forward converter.



Internal Block Diagram



Absolute Maximum Ratings

| Characteristic | Symbol | Value | Unit |
|--|---------------------------|--------------------------|------|
| Maximum Drain voltage ⁽¹⁾ | V _{D,MAX} | 650 | V |
| Drain-Gate voltage (R _{GS} =1MΩ) | V _{DGR} | 650 | V |
| Gate-source (GND) voltage | V _{GS} | ±30 | V |
| Drain current pulsed ⁽²⁾ | I _{DM} | 36.0 | ADC |
| Single pulsed avalanche energy ⁽³⁾ | E _{AS} | 950 | mJ |
| Continuous drain current (T _C =25°C) | I _D | 9.0 | ADC |
| Continuous drain current (T _C =100°C) | I _D | 5.8 | ADC |
| Maximum Supply voltage | V _{CC,MAX} | 30 | V |
| Input voltage range | V _{FB} | -0.3 to V _S D | V |
| Total power dissipation | P _D (watt H/S) | 170 | W |
| | Derating | 1.33 | W/°C |
| Operating ambient temperature | T _A | -25 to +85 | °C |
| Storage temperature | T _{STG} | -55 to +150 | °C |

Notes:

1. T_j=25°C to 150°C
2. Repetitive rating: Pulse width limited by maximum junction temperature
3. L=20mH, V_{DD}=50V, R_G=27Ω, starting T_j=25°C

Electrical Characteristics (SFET part)

(Ta = 25°C unless otherwise specified)

| Characteristic | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|---|---------|--|------|------|------|------|
| Drain-source breakdown voltage | BVDSS | VGS=0V, ID=50μA | 650 | - | - | V |
| Zero gate voltage drain current | IDSS | VDS=Max., Rating, VGS=0V | - | - | 50 | μA |
| | | VDS=0.8Max., Rating, VGS=0V, TC=125°C | - | - | 200 | mA |
| Static drain-source on resistance ^(note) | RDS(ON) | VGS=10V, ID=4.5A | - | 0.96 | 1.2 | W |
| Forward transconductance ^(note) | gfs | VDS=50V, ID=4.5A | 5.0 | - | - | S |
| Input capacitance | Ciss | VGS=0V, VDS=25V, f=1MHz | - | 1200 | - | pF |
| Output capacitance | Coss | | - | 135 | - | |
| Reverse transfer capacitance | Crss | | - | 25 | - | |
| Turn on delay time | td(on) | VDD=0.5BVDSS, ID=9.0A (MOSFET switching time are essentially independent of operating temperature) | - | 25 | 60 | nS |
| Rise time | tr | | - | 75 | 160 | |
| Turn off delay time | td(off) | | - | 130 | 270 | |
| Fall time | tf | | - | 70 | 150 | |
| Total gate charge (gate-source+gate-drain) | Qg | VGS=10V, ID=9.0A, VDS=0.8BVDSS | - | 45 | 60 | nC |
| Gate-source charge | Qgs | | - | 8 | - | |
| Gate-drain (Miller) charge | Qgd | | - | 22 | - | |

Note:

Pulse test: Pulse width ≤ 300μS, duty ≤ 2%

$$S = \frac{1}{R}$$

Electrical Characteristics (SFET part) (Continued)

(Ta = 25°C unless otherwise specified)

| Characteristic | Symbol | Test condition | Min. | Typ. | Max. | Unit |
|--|-------------------|-----------------------|------|------|------|------|
| UVLO SECTION | | | | | | |
| Start threshold voltage | VSTART | - | 8.4 | 9 | 9.6 | V |
| Stop threshold voltage | VSTOP | After turn on | 14 | 15 | 16 | V |
| OSCILLATOR SECTION | | | | | | |
| Initial accuracy | FOSC | Ta=25°C | 61 | 67 | 73 | kHz |
| Frequency change with temperature ⁽²⁾ | - | -25°C≤Ta≤+85°C | - | ±5 | ±10 | % |
| Maximum duty cycle | Dmax | - | 74 | 77 | 80 | % |
| FEEDBACK SECTION | | | | | | |
| Feedback source current | IFB | Ta=25°C, 0V≤Vfb≤3V | 0.7 | 0.9 | 1.1 | mA |
| Shutdown Feedback voltage | VSD | Vfb≥6.5V | 6.9 | 7.5 | 8.1 | V |
| Shutdown delay current | Idelay | Ta=25°C, 5V≤Vfb≤VSD | 4 | 5 | 6 | μA |
| SOFT START SECTION | | | | | | |
| Soft Start Voltage | VSS | VFB =2V | 4.7 | 5.0 | 5.3 | V |
| Soft Start Current | ISS | Sync & S/S=GND | 0.8 | 1.0 | 1.2 | mA |
| CURRENT LIMIT(SELF-PROTECTION)SECTION | | | | | | |
| Peak Current Limit | I _{OVER} | Max. inductor current | 5.28 | 6.00 | 6.72 | A |
| PROTECTION SECTION | | | | | | |
| Thermal shutdown temperature (Tj) ⁽¹⁾ | TSD | - | 140 | 160 | - | °C |
| Over voltage protection voltage | VOVP | VCC≥24V | 25 | 27 | 29 | V |
| TOTAL DEVICE SECTION | | | | | | |
| Start Up current | ISTART | VCC=14V | - | 0.1 | 0.17 | mA |
| Operating supply current (control part only) | IOP | VCC≤28 | - | 7 | 12 | mA |

NOTE:

1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS(water test) process
3. These parameters are indicated Inductor current.

Typical Performance Characteristics

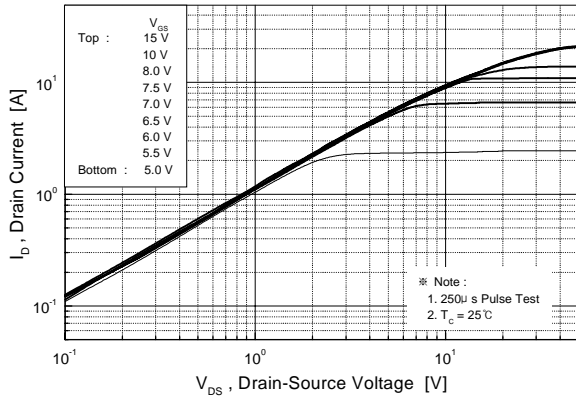


Figure 1. Output Characteristics

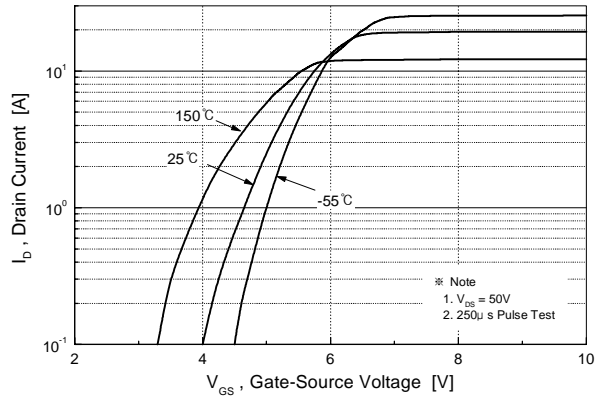


Figure 2. Transfer Characteristics

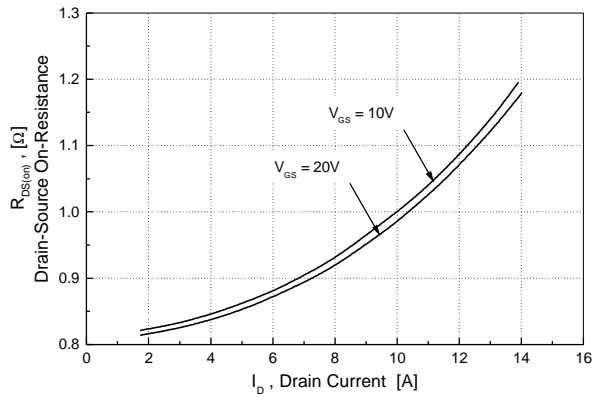


Figure 3. On-Resistance vs. Drain Current

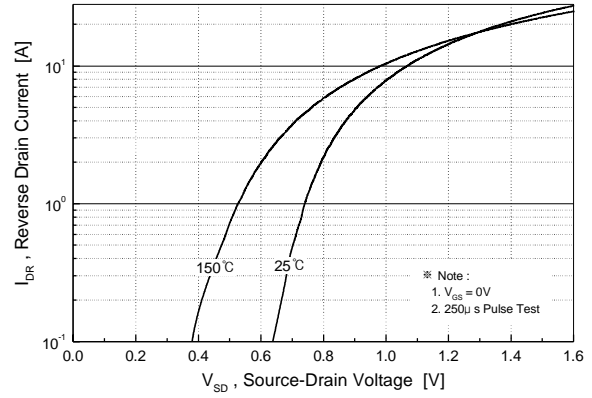


Figure 4. Source-Drain Diode Forward Voltage

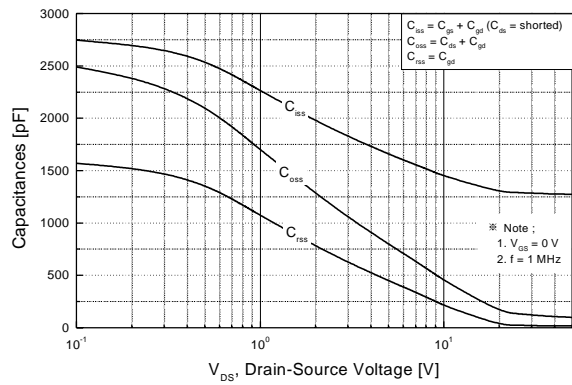


Figure 5. Capacitance vs. Drain-Source Voltage

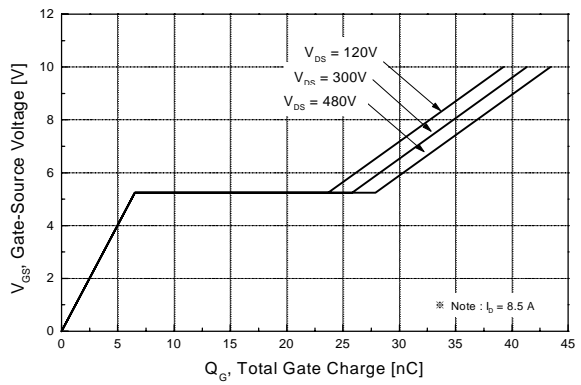


Figure 6. Gate Charge vs. Gate-Source Voltage

Typical Performance Characteristics (Continued)

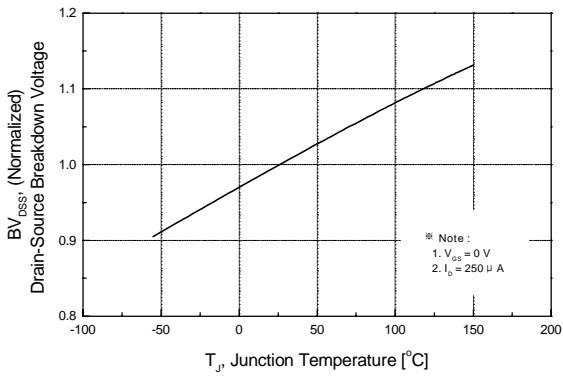


Figure 7. Breakdown Voltage vs. Temperature

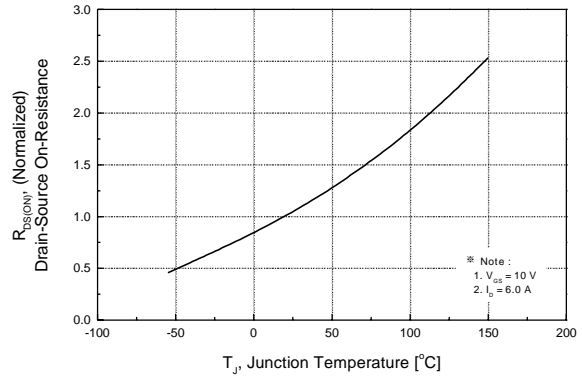


Figure 8. On-Resistance vs. Temperature

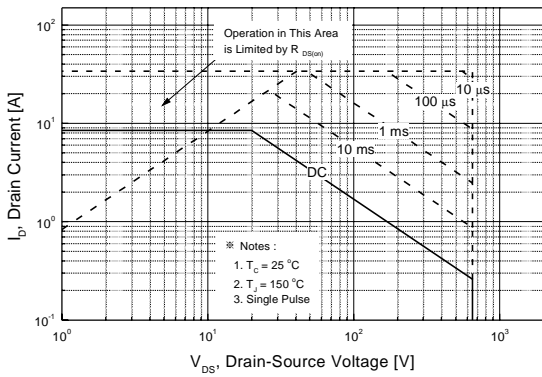


Figure 9. Max. Safe Operating Area

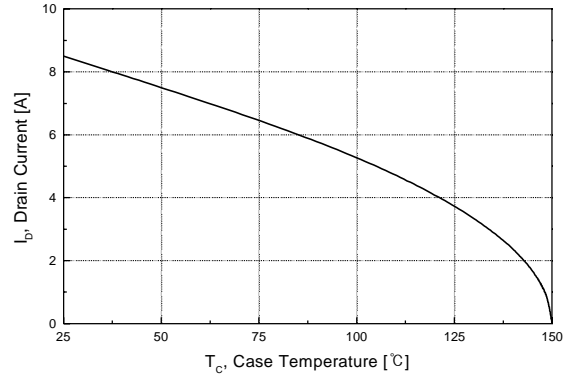


Figure 10. Max. Drain Current vs. Case Temperature

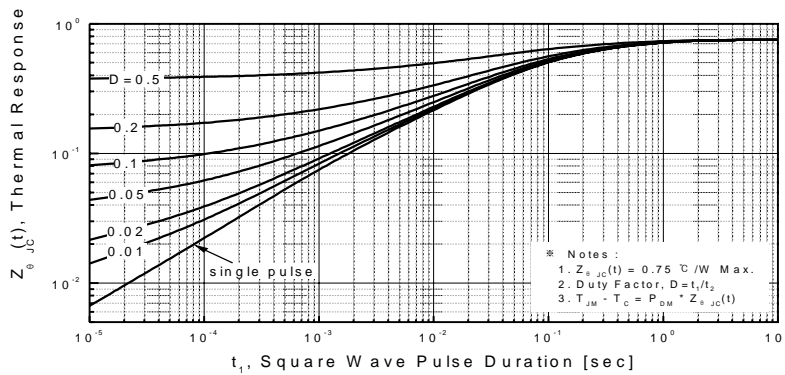


Figure 11. Thermal Response

typical performance characteristics (control part)

(These characteristic graphs are normalized at $T_a = 25^\circ\text{C}$)

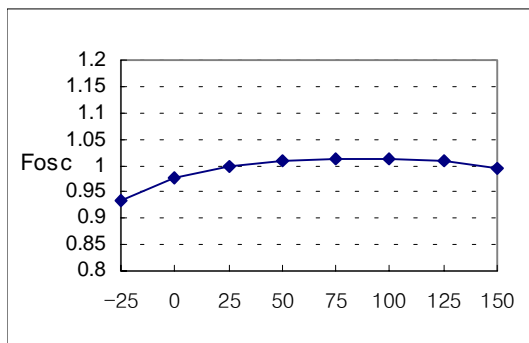


Figure 1. Operating Frequency

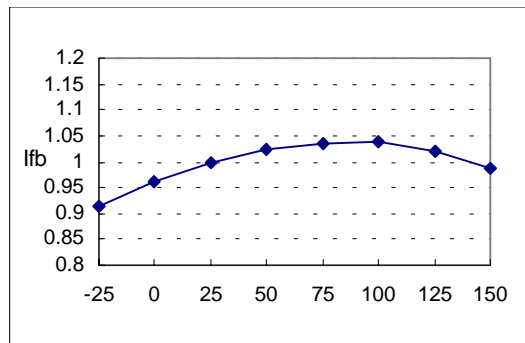


Figure 2. Feedback Source Current

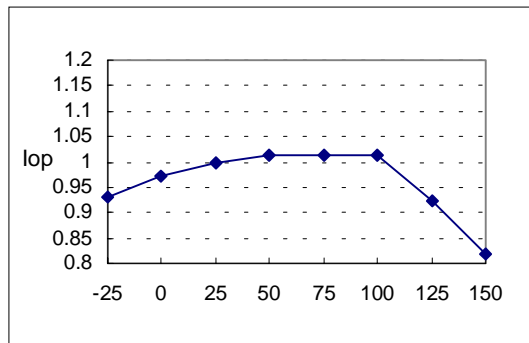


Figure 3. Operating Supply Current

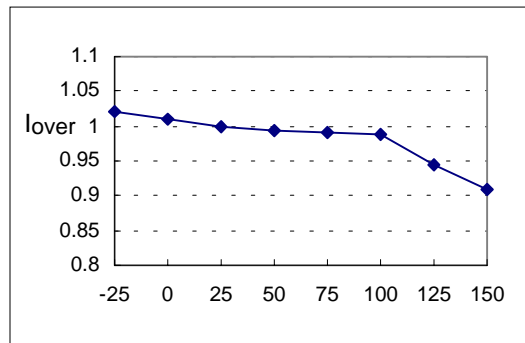


Figure 4. Peak Current Limit

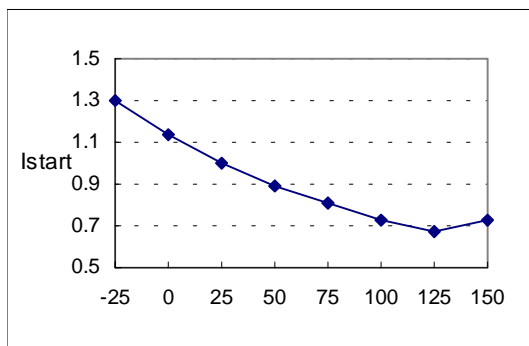


Figure 5. Start up Current

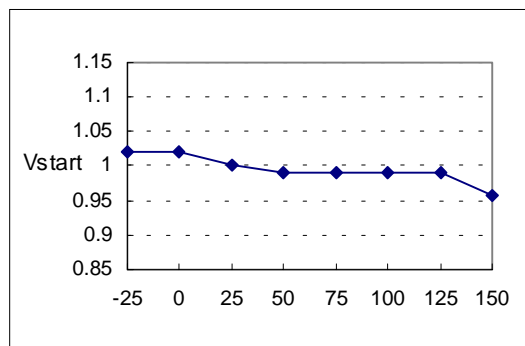


Figure 6. Start Threshold Voltage

typical performance characteristics (continued)

(These characteristic graphs are normalized at $T_a = 25^\circ\text{C}$)

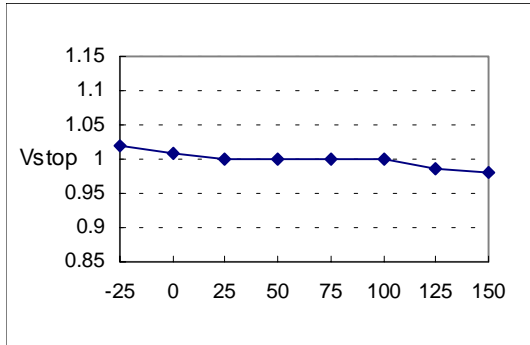


Figure 7. Stop Threshold Voltage

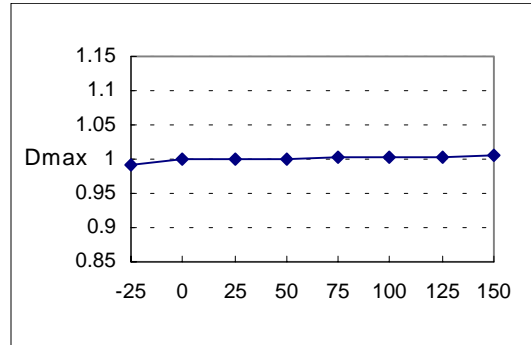


Figure 8. Maximum Duty Cycle

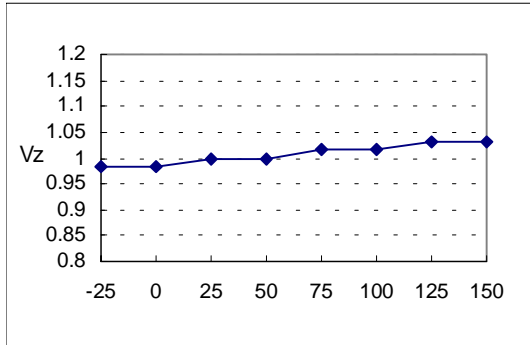


Figure 9. VCC Zener Voltage

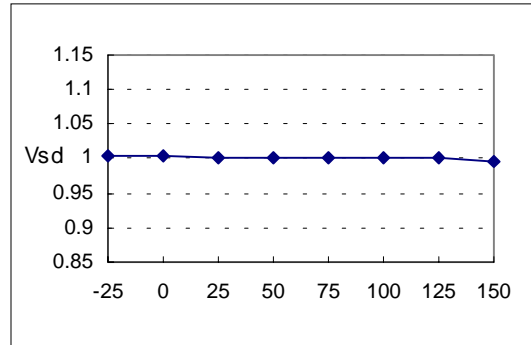


Figure 10. Shutdown Feedback Voltage

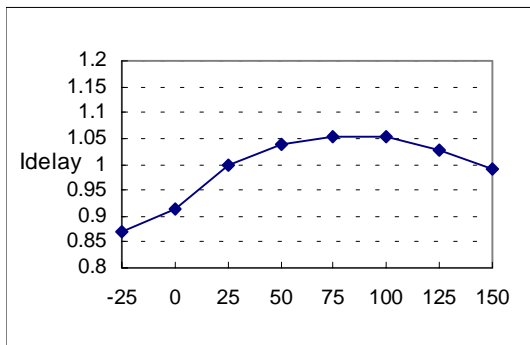


Figure 11. Shutdown Delay Current

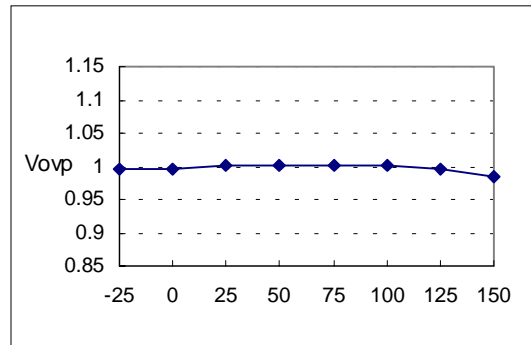


Figure 12. Over Voltage Protection

typical performance characteristics (continued)

(These characteristic graphs are normalized at $T_a = 25^\circ\text{C}$)

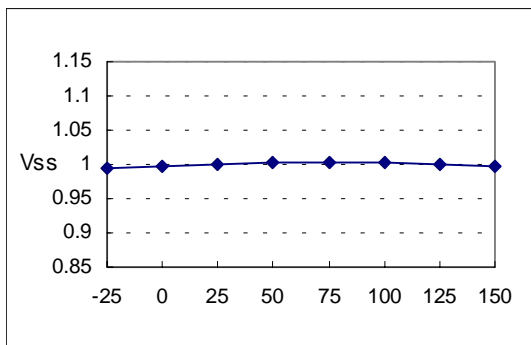


Figure13. Soft Start Voltage

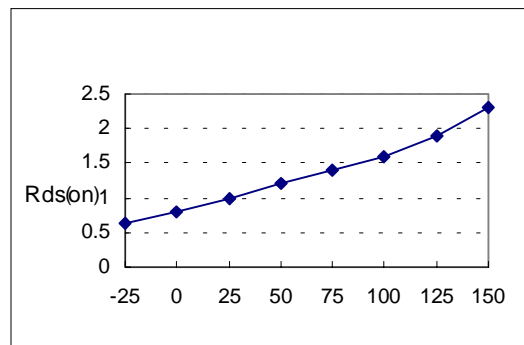
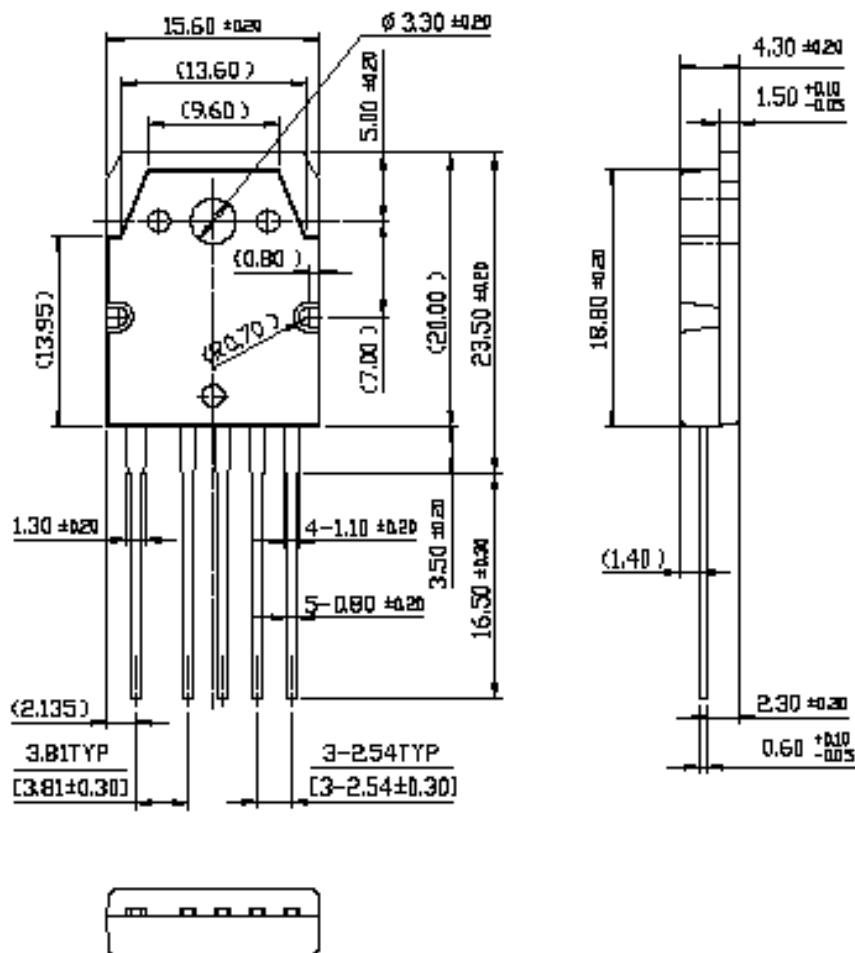


Figure 14. Static Drain-Source on Resistance

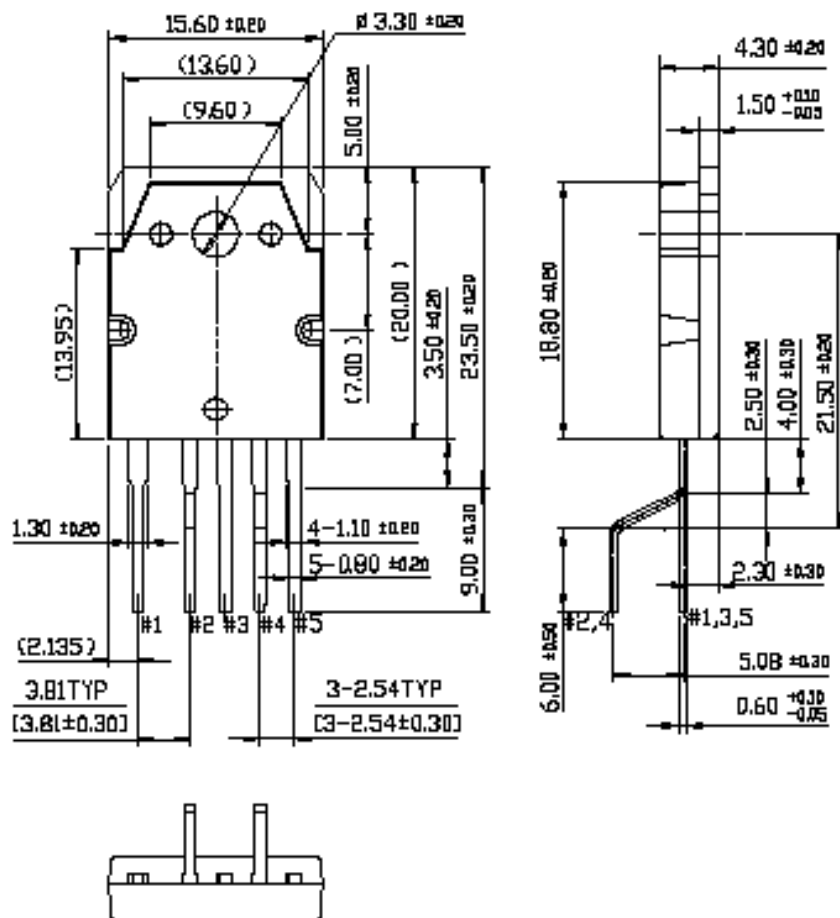
Package Dimensions

TO-3P-5L



Package Dimensions (Continued)

TO-3P-5L (Forming)



Ordering Information

| Product Number | Package | Rating | Operating Temperature |
|-----------------------|-------------------|---------------|------------------------------|
| KA5M0965Q-TU | TO-3P-5L | 650V, 9A | -25°C to +85°C |
| KA5M0965Q-YDTU | TO-3P-5L(Forming) | | |

TU : Non Forming Type

YDTU : Forming Type

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.