IL34262

Power Factor Controllers

The are active power factor controllers specifically designed for use as a preconverter in electronic ballast and in off-line power converter applications. These integrated circuits feature an internal startup timer for stand-alone applications, a one quadrant multiplier for near unity power factor, zero current detector to ensure critical conduction operation, transconductance error amplifier, quickstart circuit for enhanced startup, trimmed internal bandgap reference, current sensing comparator, and a totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of an overvoltage comparator to eliminate runaway output voltage due to load removal, input undervoltage lockout with hysteresis, cycle-by-cycle current limiting, multiplier output clamp that limits maximum peak switch current, an RS latch for single pulse metering, and a drive output high state clamp for MOSFET gate protection. These devices are available in dual-in-line and surface mount plastic packages.

Features

- Overvoltage Comparator Eliminates Runaway Output Voltage
- Internal Startup Timer
- One Quadrant Multiplier
- Zero Current Detector
- Trimmed 2% Internal Bandgap Reference
- Totem Pole Output with High State Clamp
- Undervoltage Lockout with 6.0 V of Hysteresis
- Low Startup and Operating Current
- Supersedes Functionality of SG3561 andTDA4817

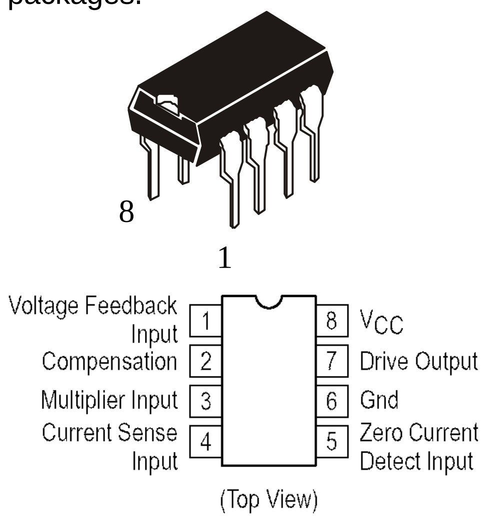

Figure 1. Package and pin connection

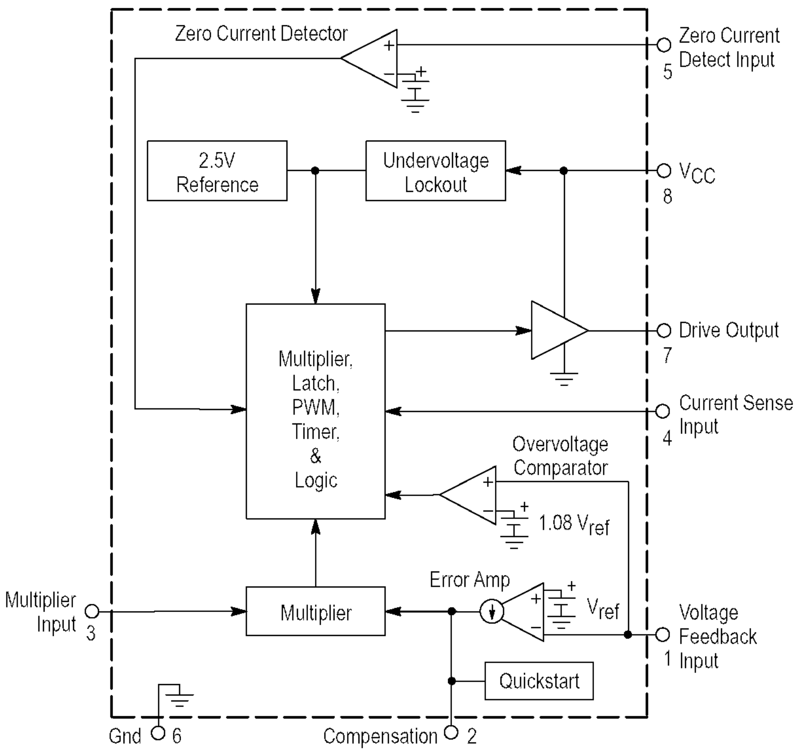

Figure 2. Simplified Block Diagram

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	(Icc + Iz)	30	mA
Output Current, Source or Sink	Io	500	mA
Current Sense, Multiplier, and Voltage Feedback Inputs	Vin	-1.0 to +10	V
Zero Current Detect Input High State Forward Current Low State Reverse Current	hn	50 -10	mA
Power Dissipation and Thermal Characteristics P Suffix, Plastic Package, Case 626 Maximum Power Dissipation @ TA = 70°C Thermal Resistance, Junction-to-Air D Suffix, Plastic Package, Case 751 Maximum Power Dissipation @ TA = 70°C Thermal Resistance, Junction-to-Air	 PD $R_{\theta JA}$ PD $R_{\theta JA}$	 800 100 450 178	 mW °C/W mW ^{0}C/W
Operating Junction Temperature	TJ	+150	°C
Operating Ambient Temperature	TA	0 to + 85	°C
Storage Temperature	Tstg	-65 to +150	°C

ELECTRICAL CHARACTERISTICS (Vcc =12 V, for typical values TA = 25°C, for min/max values TA is the operating ambient temperature range that applies unless otherwise noted.)

	Test list Position #	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER						
Voltage Feedback Input Threshold TA=25°C TA = Tlow to Thigh (Vcc = 12 V to 28 V)	 2 3	 VFB	 2.465 2.44	 2.5 —	 2.535 2.54	V
Line Regulation (VCC = 12 V to 28 V, TA = 25°C)	35	Reg_{line}	—	1.0	10	mV
Input Bias Current (VFB = 0 V)	4	IIB	—	-0.1	-0.5	µA
Transconductance (TA = 25°C)	36	g_m	80	100	130	µmho
Output Current Source (VFB = 2.3 V) Sink (VFB = 2.7 V)	 25 26	 Io	 — —	 10 10	 — —	µA
Output Voltage Swing High State (VFB = 2.3 V) Low State (VFB = 2.7 V)	 7 8	 V_{OH}(ea) V_{OL}(ea)	 5.8 —	 6.4 1.7	 — 2.4	V
OVERVOLTAGE COMPARATOR						
Voltage Feedback Input Threshold	9	V_{FB}(OV)	1.065VFB	1.08VFB	1.095VFB	V
MULTIPLIER						
Input Bias Current, Pin 3 (VFB = 0 V)	5	IIB	—	-0.1	-0.5	µA
Input Threshold, Pin 2	14	Vth(M)	1.05$V_{OL(EA)}$	1.2$V_{OL(EA)}$	—	V
Dynamic Input Voltage Range Multiplier Input (Pin 3) Compensation (Pin 2)	 33 34	 Vpin3 Vpin2	 0 to 2.5 Vth(M) to (Vth(M)+1.0)	 0 to 3.5 Vth(M) to (Vth(M)+ 1.5	 — —	V

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Multiplier Gain (Vpin 3 = 0.5 V, Vpin 2 = Vth(M) + 1.0 V) (Note 4)	15	K	0.43	0.65	0.87	1/V

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ELECTRICAL CHARACTERISTICS

	Test list Position #	Symbol	Min	Typ	Max	Unit
ZERO CURRENT DETECTOR						
Input Threshold Voltage (Vjn Increasing)	10	Vth	1.33	1.6	1.87	V
Hysteresis (Vin Decreasing)	11	V_H	100	200	300	mV
Input Clamp Voltage High State (I_{DET} = + 3.0 mA) High State (I_{DET} = - 3.0 mA)	 16 17	 V_{IH} V_{IL}	 6.1 0.3	 6.7 0.7	 — 1.0	V
CURRENT SENSE COMPARATOR						
Input Bias Current (Vpin 4 = 0 V)	6	I_{IB}	—	-0.15	-1.0	? A
Input Offset Voltage (Vpm 2 = 1.1 V, Vpm 3 = 0 V)	12	V_{IO}	—	9.0	25	mV
Maximum Current Sense Input Threshold (Note 5)	13	$V_{th(max)}$	1.3	1.5	1.8	V
Delay to Output	38	$t_{PHL(in/out)}$	—	200	400	ns
DRIVE OUTPUT						
Output Voltage (V_{CC} = 12 V) Low State (I_{sink} = 20 mA) (I_{sink} = 200 mA) High State (I_{source} = 20 mA) (I_{source} = 200 mA)	 27 28 29 30	 V_{OL} V_{OH} 	 — — 9.8 7.8	 0.3 2.4 10.3 8.4	 — — 0.8 3.3	V
Output Voltage (V_{CC} = 30 V) High State (I_{source} = 20 mA, C_L = 15 pF)	31	$V_{O(max)}$	14	16	18	V
Output Voltage Rise Time (C_L 1.0 nF)	41	t_r	—	50	120	ns
Output Voltage Fall Time (C_L 1.0 nF)	39	t_f	—	50	120	ns
Output Voltage with UVLO Activated (Vcc = 7.0 V,I_{Sink}= 1.0mA)	32	$V_{O(UVLO)}$	—	0.1	0.5	V
RESTART TIMER						
Restart Time Delay	40	t_{DLY}	200	620	—	µs
UNDERVOLTAGE LOCKOUT						
Startup Threshold (v_{CC} Increasing)	19	$V_{th(on)}$	11.5	13	14.5	V
Minimum Operating Voltage After Turn-On (V_{CC} Decreasing)	20	$V_{Shutdown}$	7.0	8.0	9.0	V
Hysteresis	21	V_H	3.8	5.0	6.2	V
TOTAL DEVICE						
Power Supply Current Startup (Vcc = 7.0 V) Operating Dynamic Operating (50 kHz, C_L = 1.0 nF)	 22 23 37	 I_{CC}	 —	 0.25 6.5 9.0	 0.4 12 20	 mA
Power Supply Zener Voltage (Ice = 25 mA)	24	V_Z	30	36	—	V

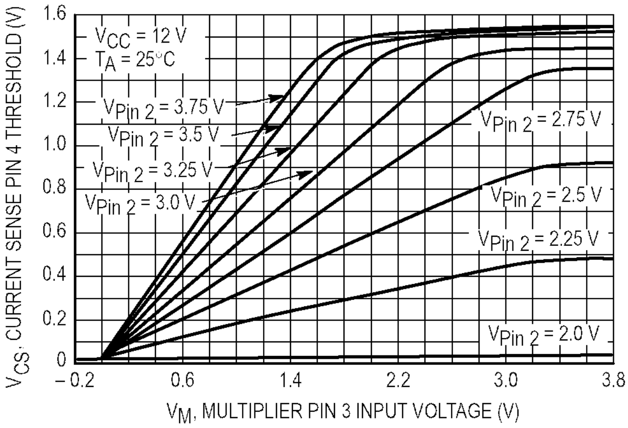

Figure 3. Current Sense Input Threshold versus Multiplier Input.

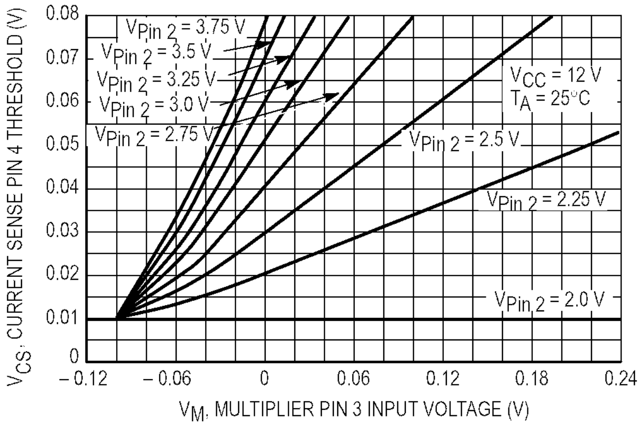

Figure 4. Current Sense Input Threshold versus Multiplier Input, Expanded View

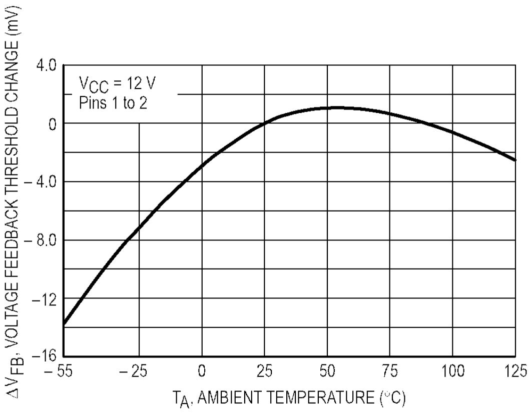

Figure 5. Voltage Feedback Input Threshold Change versus Temperature.

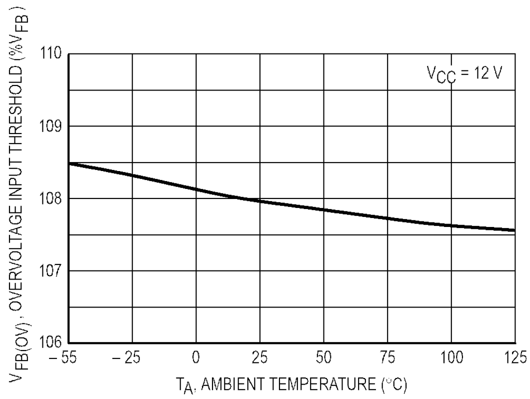

Figure 4. Overvoltage Comparator Input Threshold versus Temperature.

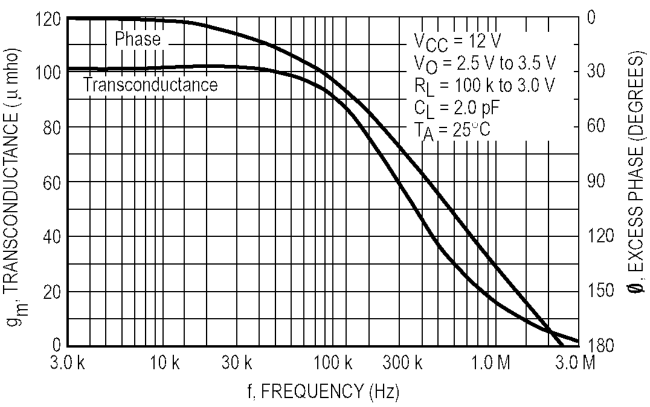

Figure 7. Error Amp Transconductance and Phase versus Frequency

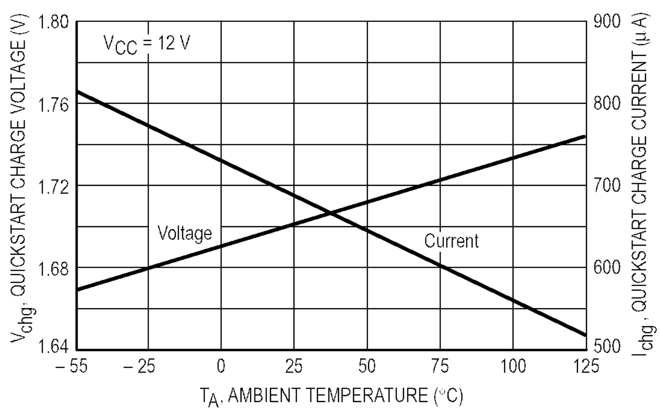

Figure 8. Quickstart Charge Current versus Temperature

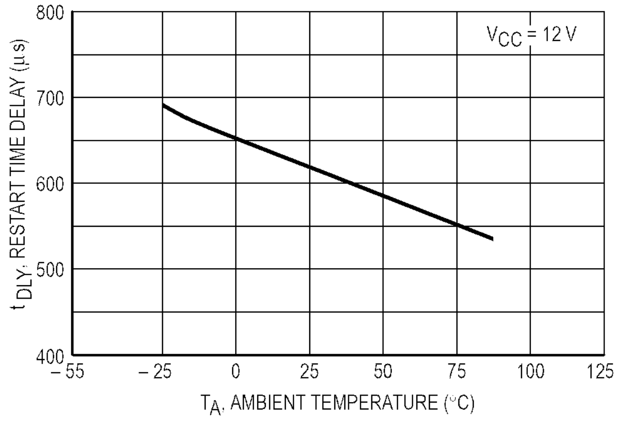

Figure 9. Restart Timer Delay versus Temperature

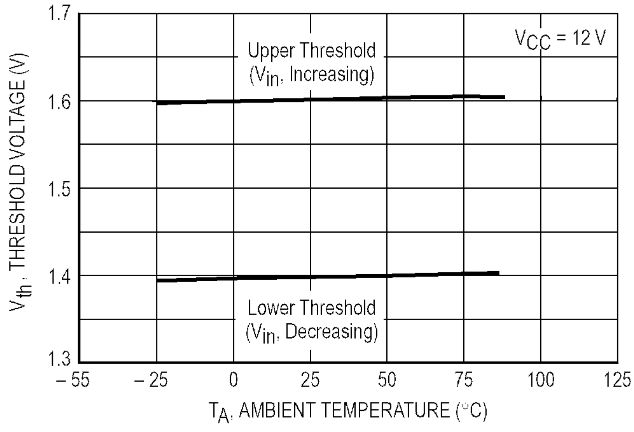

Figure 10. Zero Current Detector Input Threshold Voltage versus Temperature

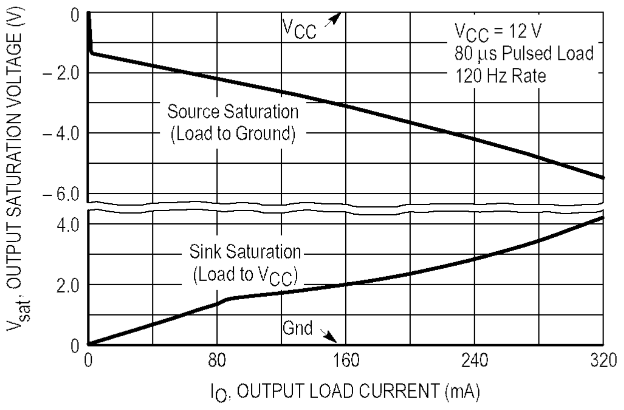

Figure 11. Output Saturation Voltage versus Load Current

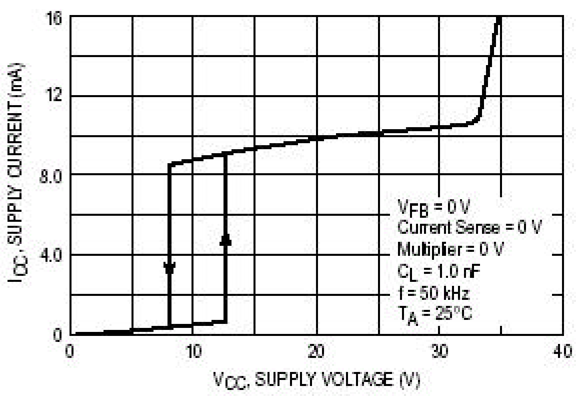

Figure 12. Supply Current versus Supply Voltage

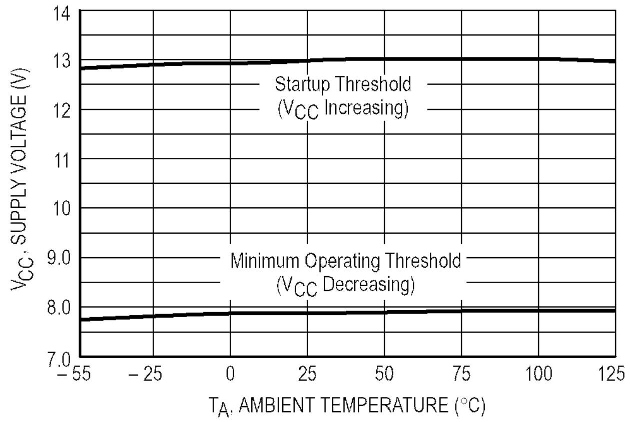

Figure 13. Undervoltage Lockout Thresholds versus Temperature

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APPLICATIONS INFORMATION

The application circuits shown in Figures 14, 15 and 16 reveal that few external components are required for a complete power factor preconverter. Each circuit is a peak detecting current–mode boost converter that operates in critical conduction mode with a fixed on–time and variable off–time. A major benefit of critical conduction operation is that the current loop is inherently stable, thus eliminating the need for ramp compensation. The application in Figure 14 operates over an input voltage range of 90 Vac to 138 Vac and provides an output power of 80 W (230 V at 350 mA) with an associated power factor of approximately 0.998 at
nominal line. Figures 15 and 16 are universal input preconverter examples that operate over a continuous input voltage range of 90 Vac to 268 Vac. Figure 15 provides an output power of 175 W (400 V at 440 mA) while Figure 16 provides 450 W (400 V at 1.125 A). Both circuits have an observed worst–case power factor of approximately 0.989.

Table 3. Design Equations

Notes	Calculation	Formula
Calculate the maximum required output power.	Required Converter Output Power	$P_O = V_O I_O$
Calculated at the minimum required ac line voltage for output regulation. Let the efficiency ? = 0.92 for low line operation.	Peak Inductor Current	$I_{L(pk)} = \dfrac{2\sqrt{2}P_O}{\eta V_{ac(LL)}}$
Let the switching cycle t = 40 ?s for universal input (85 to 265 Vac) operation and 20 ?s for fixed input (92 to 138 Vac, or 184 to 276 Vac) operation.	Inductance	$L_p = \dfrac{t\left(\dfrac{V_O}{\sqrt{2}} - V_{ac(LL)}\right)\eta\, V_{ac(LL)}^{2}}{\sqrt{2}V_O P_O}$
In theory the on–time ton is constant. In practice ton tends to increase at the ac line zero crossings due to the charge on capacitor C_5. Let Vac = Vac($_{LL}$) for initial ton and toff calculations.	Switch On–Time	$t_{on} = \dfrac{2P_O L_p}{\eta V_{ac}^2}$
The off–time t_{off} is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (?) represents the angle of the ac line voltage.	Switch Off–Time	$t_{off} = \dfrac{t_{on}}{\dfrac{V_O}{\sqrt{2}\,V_{ac}\,\lvert\sin\theta\rvert} - 1}$
The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, toff approaches zero producing an increase in switching frequency.	Switching Frequency	$f = \dfrac{1}{t_{on} + t_{off}}$
Set the current sense threshold V_{CS} to 1.0 V for universal input (85 Vac to 265 Vac) operation and to 0.5 V for fixed input (92 Vac to 138 Vac, or 184 Vac to 276 Vac) operation. Note that V_{CS} must be <1.4 V.	Peak Switch Current	$R7 = \dfrac{V_{CS}}{I_{L(pk)}}$
Set the multiplier input voltage V_M to 3.0 V at High line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.	Multiplier Input Voltage	$V_M = \dfrac{V_{ac}\sqrt{2}}{\left(\dfrac{R5}{R3}+1\right)}$
The I_{IB} R_1 error term can be minimized with a divider current in excess of 50 ?A.	Converter Output Voltage	$V_O = V_{ref}\left(\dfrac{R2}{R1}+1\right) - I_{IB}R1$
The calculated peak–to–peak ripple must be less than 16% of the average dc output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator text. ESR is the equivalent series resistance of C_3	Converter Output Peak to Peak Ripple Voltage	$\Delta V_{O(P-P)} = I_O\sqrt{\left(\dfrac{1}{2\pi f_{ac} C3}\right)^2 + ESR^2}$
The bandwidth is typically set to 20 Hz. When operating at high ac line, the value of C_1 may need to be increased. (See Figure 17)	Error Amplifier Bandwidth	$BW = \dfrac{g_m}{2\pi\ C1}$

The following converter characteristics must be chosen:

V_O — Desired output voltage   Vac — AC RMS line voltage
I_O — Desired output current $Vac_{(LL)}$ — AC RMS low line voltage
? V_O — Converter output peak–to–peak ripple voltage

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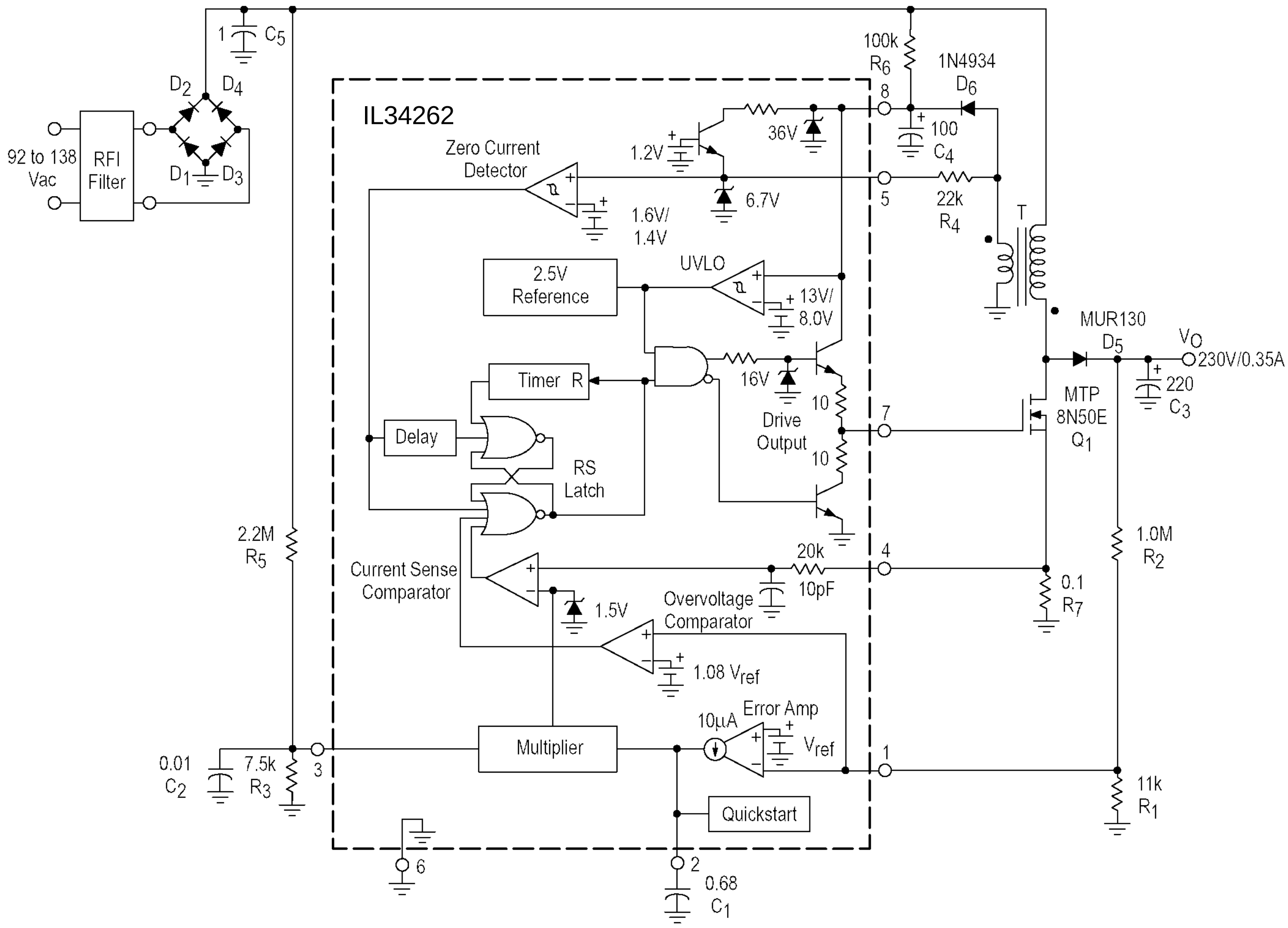

Figure 14. 80 W Power Factor Controller

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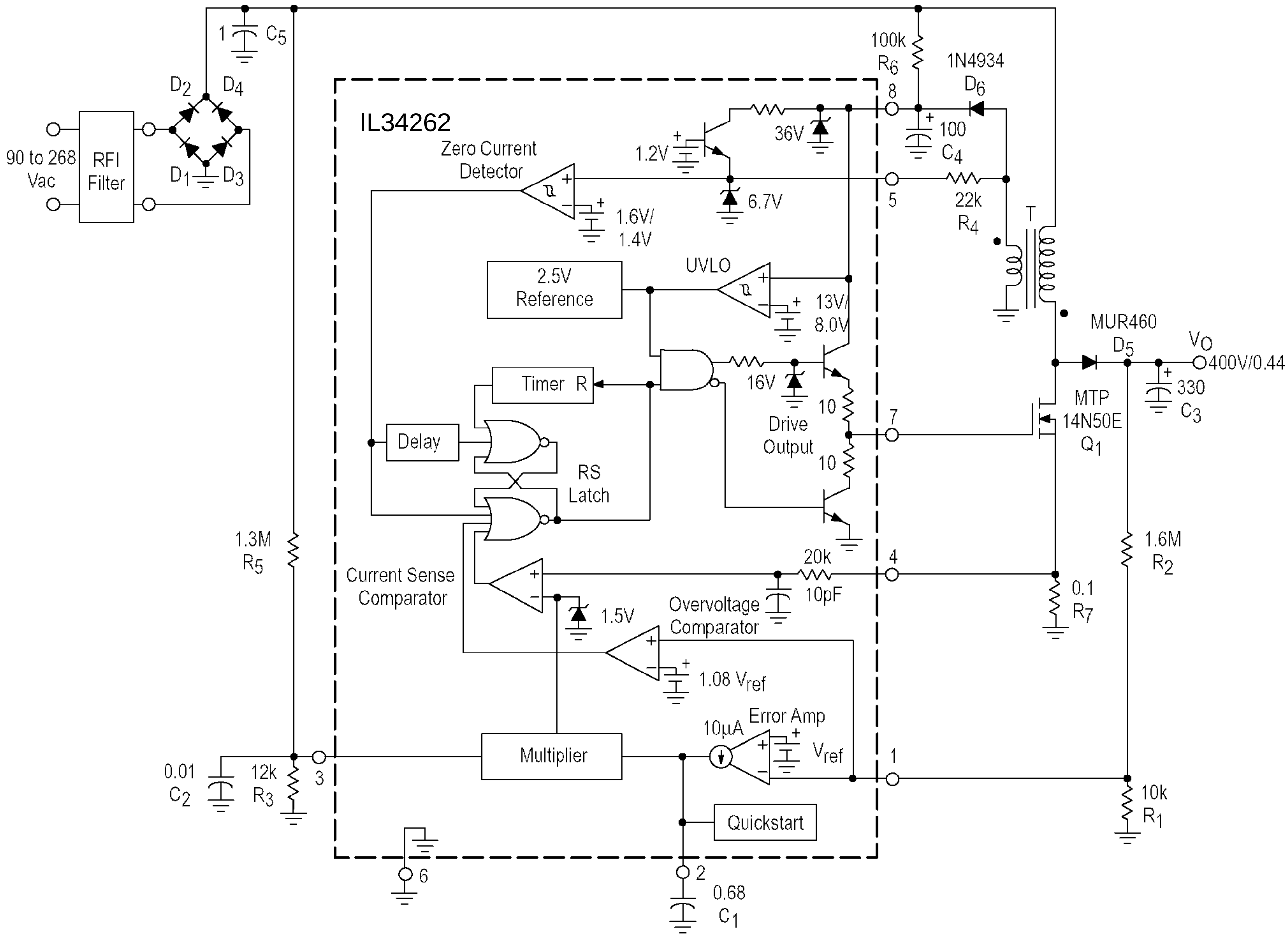

Figure 15. 175 W Universal Input Power Factor Controller

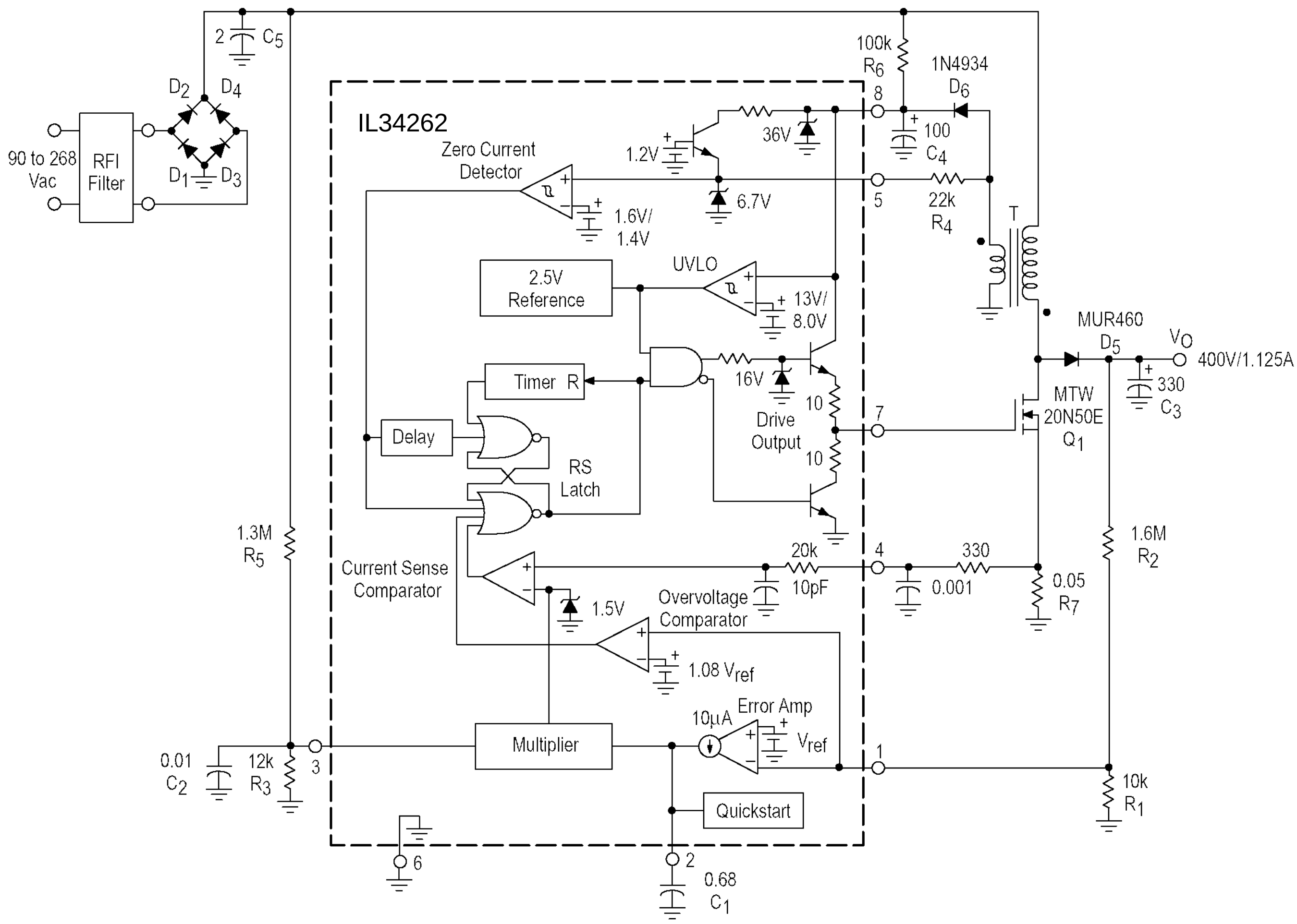

Figure 16. 450 W Universal Input Power Factor Controller

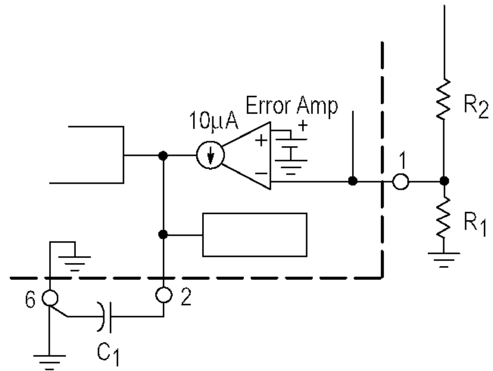

Figure 17. Error Amp Compensation

The Error Amp output is a high impedance node and is susceptible to noise pickup. To minimize pickup, compensation capacitor C_1 must be connected as close to Pin 2 as possible with a short, heavy ground returning directly to Pin 6. When operating at high ac line, the voltage at Pin 2 may approach the lower threshold of the Multiplier, ? 2.0 V. If there is excessive ripple on Pin 2, the Multiplier will be driven into cut–off causing circuit instability, high distortion and poor power factor. This problem can be eliminated by increasing the value of C_1.

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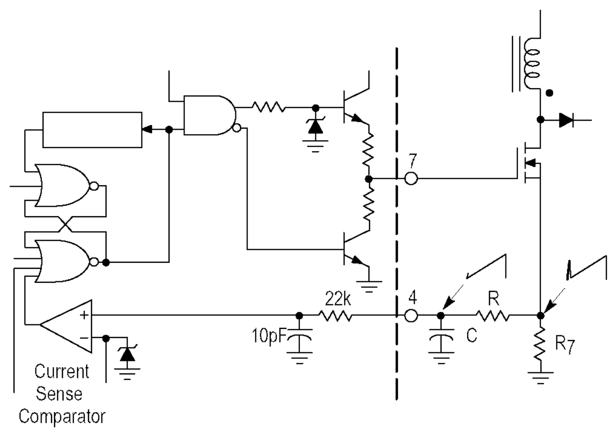

Figure 18. Current Waveform Spike Suppression

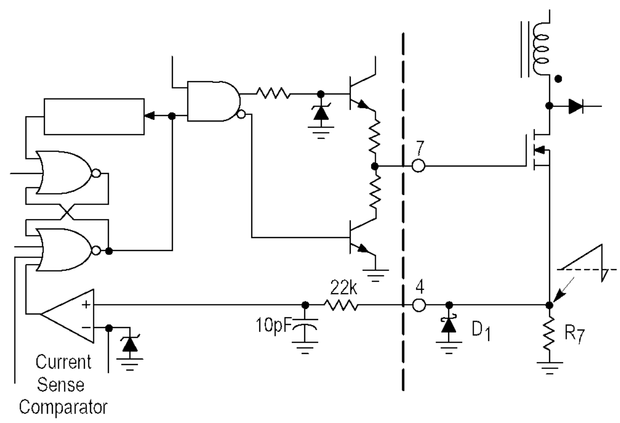

Figure 19. Negative Current Waveform Spike Suppression

A narrow turn–on spike is usually present on the leading edge of the current waveform and can cause circuit instability. The IL34262 provides an internal RC filter with a time constant of 220 ns. An additional external RC filter may be required in universal input applications that are above 200 W. It is suggested that the external filter be placed directly at the Current Sense Input and have a time constant that approximates the spike duration.

A negative turn–off spike can be observed on the trailing edge of the current waveform. This spike is due to the parasitic inductance of resistor R_7, and if it is excessive, it can cause circuit instability. The addition of Shottky diode D_1 can effectively clamp the negative spike. The addition of the external RC filter shown in Figure 18 may provide sufficient spike attenuation.

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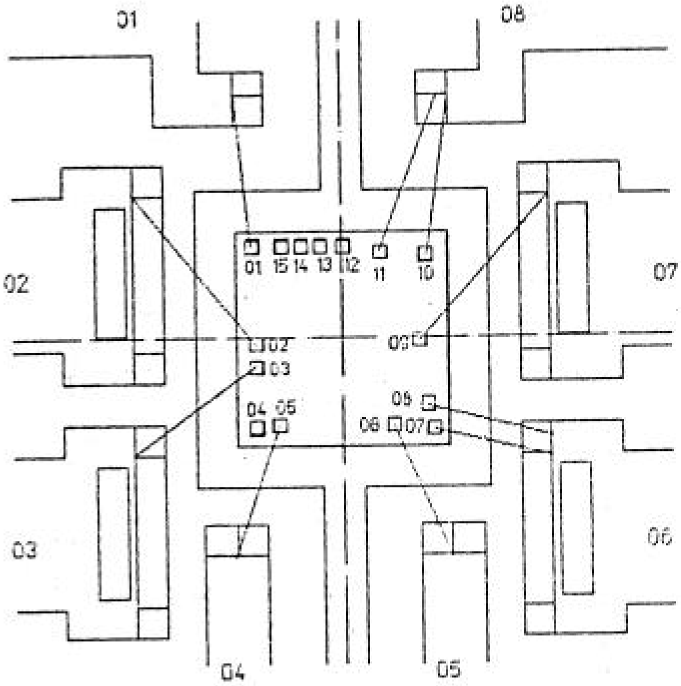

Figure 20. Bonding diagram of Il34262

Chip size 2,1x2,1mm^2
Chip holder size 2,9x2,9mm^2
Chip contact pads 04, 12, 13, 14, 15 are not to be wired.

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