Data Sheet

10-bit digital to analogue converter IC 3410

RS stock number 631-389

The 3410 is a 10-bit multiplying digital to analogue converter IC Complete 10-bit accuracy is achieved without laser trimming and monotonicity is guaranteed over the operating temperature range. This device when used in conjunction with an output buffer amplifier and reference performs the full 10-bit conversion.

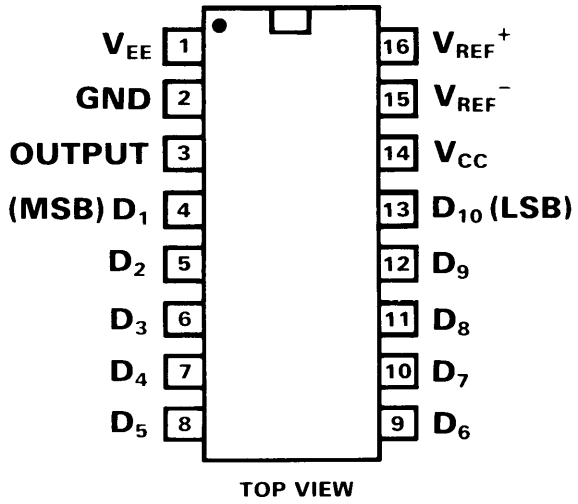
Absolute maximum ratings

V_{CC} Supply voltage _____ +7V
V_{EE} Supply voltage _____ -18V
V_I Digital input voltage _____ +15V
V_O Applied output voltage _____ 0.5, -5.0V
I_{REF} Reference current _____ 2.5mA
V_{REF} Reference amplifier inputs _____ V_{CC}, V_{EE}
V_{REF} (D) Reference amplifier differential inputs _____ 0.7V
Operating temperature range _____ 0°C to +70°C
Junction temperature _____ +150°C

Features

- 10-bit resolution and accuracy
- Guaranteed monotonicity over full temperature range
- Fast settling time 250ns typ.
- TTL and CMOS compatible digital inputs
- Reference amplifier internally compensated.

Pin connections



Electrical characteristics V_{CC} = +5.0V dc, V_{EE} = -15V dc, $\frac{V_{REF}}{R16}$ = 2.0mA, all digital inputs at high logic level T_A = 0° to +70°C, unless otherwise noted.

Symbol and parameter		Test conditions	Min	Typ	Max	Unit
E_r	Relative accuracy (Error relative to full scale I_O)	T_A = 25°C			±0.05	%
					1/4	LSB
TCE_r	Relative accuracy drift (Relative to full scale I_O)			2.5		p.p.m./°C
	Monotonicity	Over temperature	10			Bits
t_S	Settling time to within ± ½ LSB (all bits low to high)	T_A = 25°C		250		ns
t_{PLH} t_{PHL}	Propagation delay time	T_A = 25°C		35 20		ns
TCI_O	Output full scale current drift				60	p.p.m./°C
V_{IH}	Digital input logic levels (All bits) High level, logic '1' Low level, logic '0'		2.0		 0.8	Vdc
I_{IH} I_{IL}	Digital input current (All bits) High level, V_{IH} = 5.5V Low level, V_{IL} = 0.8V			 -0.05	+0.4 -0.4	mA
$I_{REF(15)}$	Reference input bias current (Pin 15)			-1.0	-5.0	µA
I_{OR}	Output current range			4.0	5.0	mA
I_{OH}	Output current (All bits high)	V_{REF} = 2.000V, R_{16} = 1000Ω	3.8	3.996	4.2	mA
I_{OL}	Output current (All bits low)	T_A = 25°C		0	2.0	µA
V_O	Output voltage compliance	T_A = 25°C			-2.5 +0.2	Vdc
SR I_{REF}	Reference amplifier slew rate			20		mA/µs
ST I_{REF}	Reference amplifier settling time	0 to 4.0mA, ± 0.1%		2.0		µs
PSRR(-)	Output current power supply sensitivity			0.003	0.01	%/%
C_O	Output capacitance	V_O = 0		25		pF
C_I	Digital input capacitance (All bits high)			4.0		pF
I_{CC} I_{EE}	Power supply current (All bits low)			 -11.4	+18 -20	mA
V_{CC} V_{EE}	Power supply voltage range	T_A = 25°C	+4.75 -14.25	+5.0 -15	+5.25 -15.75	Vdc
	Power consumption (All bits low) (All bits high)			 220 200	 380	mW

Performance characteristics

Figure 1 Output current vs. output compliance voltage

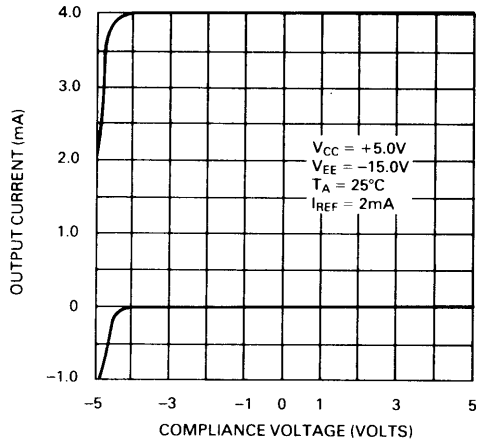


Figure 2 Maximum output compliance voltage vs. temperature

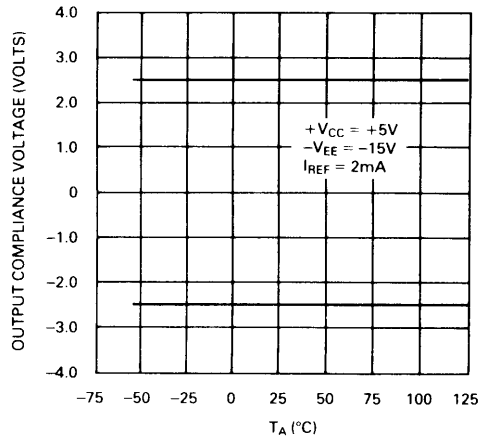


Figure 3 Power supply current vs. temperature

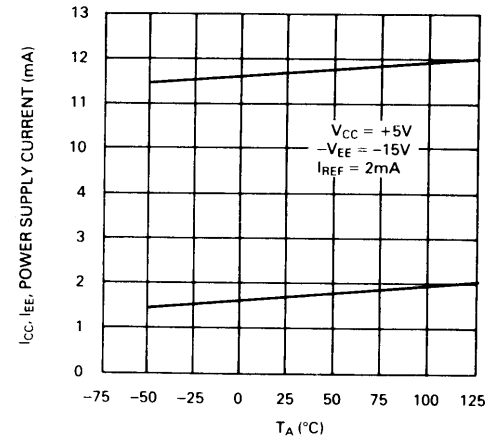


Figure 4 Reference amplifier frequency response

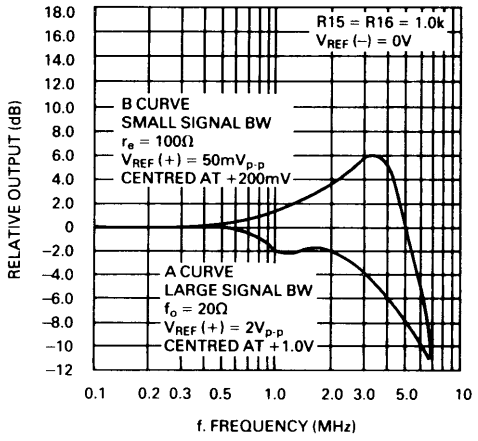
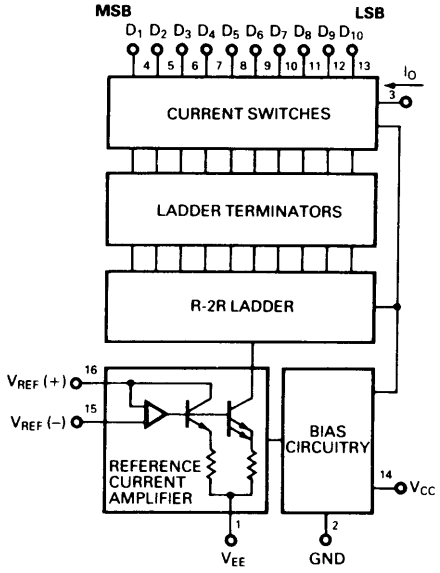


Figure 5 Block diagram



Circuit description

The 3410 consists of four segment current sources which generate the 2 Most Significant Bits (MSBs), and an R/2R DAC implemented with ion implanted resistors for scaling the remaining 8 Least Significant Bits (LSBs). (Figure 6.) This approach provides complete 10-bit accuracy without trimming.

The individual bit currents are switched ON or OFF by fully differential current switches. The switches use current steering for speed.

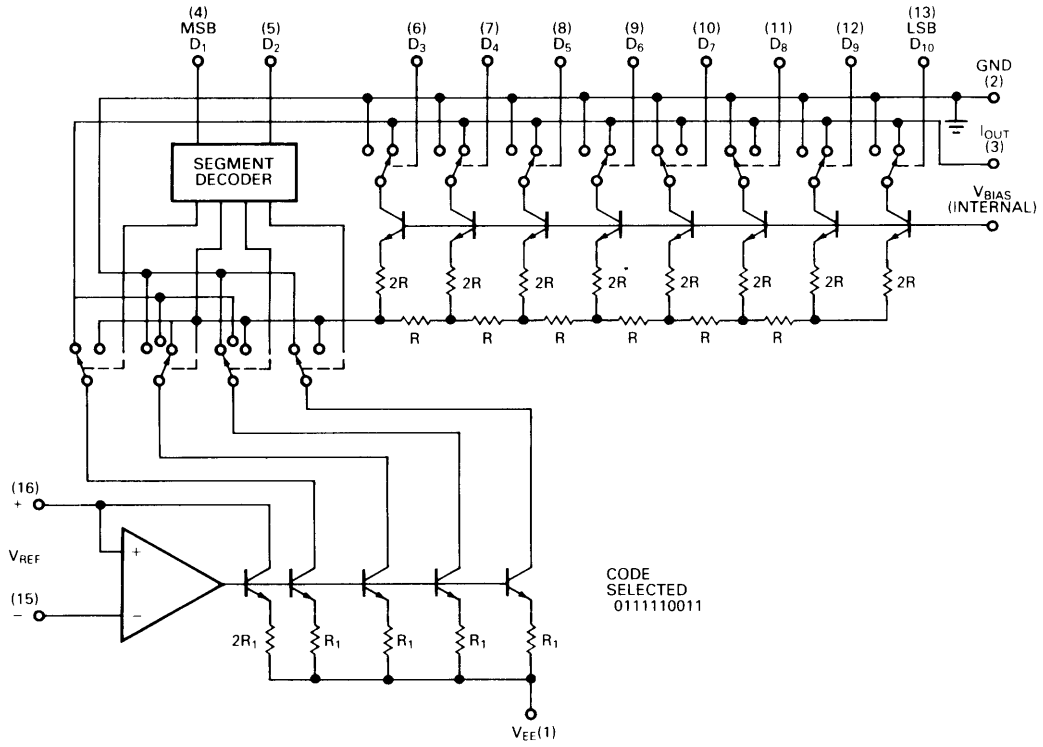
An on-chip high-slew reference current amplifier drives the R/2R ladder and segment decoder. The currents are scaled in such a way that, with all bits on, the maximum output current is two times 1023/1024 of the reference amplifier current, or nominally 3.996mA for a 2.000mA reference input current. The reference amplifier allows the user to provide a voltage input. Out-board resistor R16 (Figure 7) converts this voltage to a usable current. A current mirror doubles this reference current and feeds it to the segment decoder and resistor ladder. Thus, for a reference voltage of 2.0 volts and a 1kΩ resistor tied to Pin 16, the full scale

current is approximately 4.0mA. This relationship will remain regardless of the reference voltage polarity.

Connections for a positive reference voltage are shown in Figure 7a. For negative reference voltage inputs, or for bipolar reference voltage inputs in the multiplying mode., R15 can be tied to a negative voltage corresponding to the minimum input level. For a negative reference input, R16 should be grounded (Figure 7b). In addition, the negative voltage reference must be at least 3V above the V_{EE} supply voltage for best operation. Bipolar input signals may be handled by connecting R16 to a positive voltage equal to the peak positive input level at Pin 15.

When a dc reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5.0V supply, which drives logic, is to be used as the reference, R16 should be decoupled by connecting it to the +5.0V logic supply through another resistor and bypassing the junction of the two resistors with a 0.1µF capacitor to ground.

Figure 6 **3410 equivalent circuit**



The reference amplifier is internally compensated with a 10pF feed-forward capacitor, which gives it its high slew rate and fast settling time. Proper phase margin is maintained with all possible values of R16 and reference voltages which supply 2.0mA reference current into Pin 16. The reference current can also be supplied by a high impedance current source of 2.0mA. As R16 increases, the bandwidth of the amplifier decreases slightly and settling time increases. For a current source with a dynamic output impedance of 1.0MΩ, the bandwidth of the reference amplifier is approximately half what it is in the case of R16 = 1.0kΩ, and settling time is ≈ 10µs. The reference amplifier phase margin decreases as the current source value decreases in the case of a current source reference, so that the minimum reference current supplied from a current source is 0.5mA for stability.

Output voltage compliance

The output voltage compliance ranges from -2.5 to +0.2V. As shown in Figure 2, this compliance range is nearly constant over temperature. At the temperature extremes, however, the compliance voltage may be reduced if V_{EE} > -15V.

Accuracy

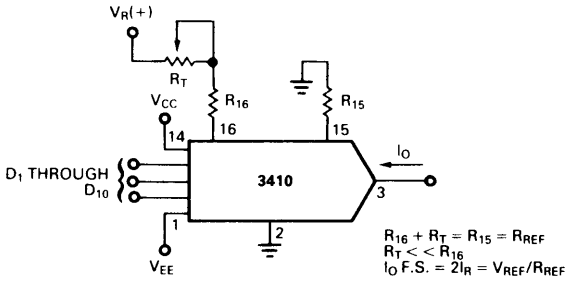
Absolute accuracy is a measure of each output current level with respect to its intended value. It is dependent upon relative accuracy and full scale current drift. Relative accuracy, or linearity, is the measure of each output current with respect to its intended fraction of the full scale current. The relative accuracy of the 3410 is fairly constant over temperature due to the excellent temperature tracking, of the implanted resistors. The full scale current from the reference amplifier may drift with temperature causing a change in the absolute accuracy. However, the 3410 has a low full scale current drift with temperature.

The 3410 is accurate to within ±.05% at 25°C with a reference current of 2.0mA on Pin 16.

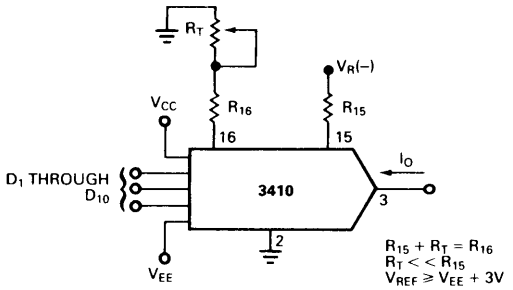
Monotonicity

The 3410 is guaranteed monotonic over temperature. This means that for every increase in the input digital code, the output current either remains the same or increases but never decreases. In the multiplying mode, where reference input current will vary, monotonicity can be assured if the reference input current remains above 0.5mA.

Figure 7 Basic connections



a) Positive reference voltage



b) Negative reference voltage

Settling time

The worst case switching condition occurs when all bits are switched 'on', which corresponds to a low-to-high transition for all bits. This time is typically 250ns for the output to settle to within ±1/2 LSB for 10-bit accuracy, and 200ns for 8-bit accuracy. The turn-off time is typically 120ns. These times apply when the output swing is limited to a small (<0.7 volt) swing and the external output capacitance is under 25pF.

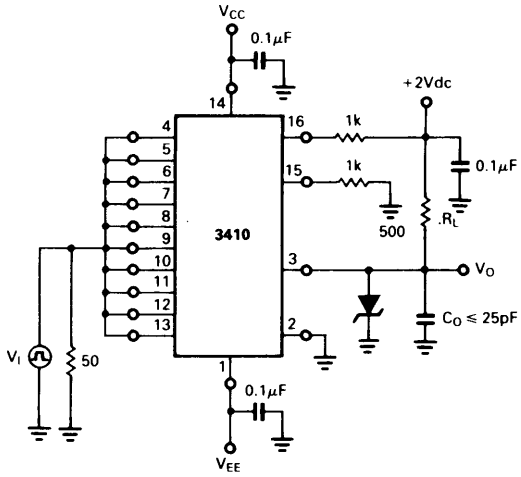
The major carry (MSB off-to-on, all others on-to-off) settles in approximately the same time as when all bits are switched off-to-on.

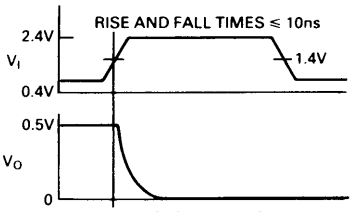
If a load resistor of 625 ohms is connected to ground, allowing the output to swing to -2.5 volts, the settling time increases to 1.5µs.

Extra care must be taken in board layout as this is usually the dominant factor in satisfactory test results when measuring time. Short leads, 100µF supply bypassing, and minimum scope lead length are all necessary.

A typical test set-up for measuring settling time is shown in Figure 8. The same set-up for the most part can be used to measure the slew rate of the reference amplifier (Figure 10) by typing all data bits high, pulsing the voltage reference input between 0 and 2V, and using a 500Ω load resistor R_L.

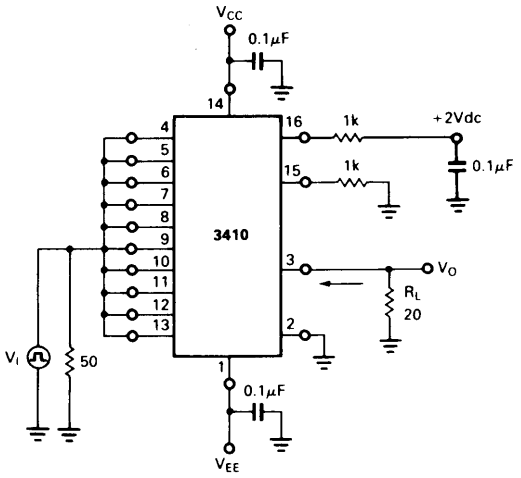
Figure 8 Settling time

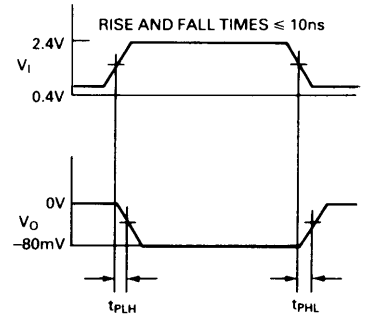




t_S - 250 ns TYPICAL
TO ± 1.2 LSB
USE R_L TO GND FOR TURN-OFF MEASUREMENT
FOR SETTLING TIME
MEASUREMENT.
(ALL BIT SWITCHED
LOW TO HIGH)

Figure 9 Propagation delay time





FOR PROPAGATION
DELAY TIME