275V, 64-Channel Serial to Parallel Converter with High Voltage Push-Pull Outputs

Ordering Information

Device	Recommended Operating V_{PP} Max	Package Options
		80-Lead Quad Plastic Gullwing
HV3527	275V	HV3527PG

Features

- ☐ HVCMOS® technology
- ☐ Output voltages up to 275V
- ☐ Low power level shifting
- ☐ Shift register speed 6MHz @ V_{DD} 5V
- ☐ Latched data outputs
- ☐ Output polarity and blanking
- ☐ CMOS compatible inputs
- ☐ Forward and reverse shifting options

General Description

(Not recommended for new designs. Please use HV507 with improved performance.)

The HV35 is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a printer driver for electrostatic applications. It can also be used in any application requiring multiple output high voltage, low current sourcing and sinking capabilities.

The device consists of a 64-bit shift register, 64 latches, and control logic to perform the polarity select and blanking of the outputs. A DIR pin controls the direction of data shift through the device. With DIR grounded, D_{IOA} is Data-In and D_{IOB} is Data-Out; data is shifted from $HV_{OUT}64$ to $HV_{OUT}1$. When DIR is at logic high, D_{IOB} is Data-In and D_{IOA} is Data-Out: data is then shifted from $HV_{OUT}1$ to $HV_{OUT}64$. Data is shifted through the shift register on the low to high transition of the clock. Data output buffers are provided for cascading devices. Operation of the shift register is not affected by the $\overline{LE}$ (latch enable), $\overline{BL}$ (blanking), or the $\overline{POL}$ (polarity) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ (latch enable) is high. The data in the latch is stored during $\overline{LE}$ transition from high to low.

A bias pin is used to ensure that the device operates at full V_{PP} voltage.

Absolute Maximum Ratings[1]

Supply voltage, V_{DD}	-0.5V to +6V
Supply voltage, V_{PP}	V_{DD} to 300V
Logic input levels	-0.5V to V_{DD} +0.5V
Ground current[2]	1.5A
High voltage supply current[2]	1.3A
Continuous total power dissipation[3]	1200mW
Operating temperature range	0°C to +70°C
Storage temperature range	-65°C to +150°C

Notes:

1. All voltages are referenced to GND.
2. Connection to all power and ground pads is required. Duty cycle is limited by the total power dissipated in the package.
3. For operation above 25°C ambient derate linearly to 85°C at 15mW/°C.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Typ	Max	Units	Conditions
I_{DD}	V_{DD} Supply Current				25	mA	f_{CLK} = 6MHz, f_{DATA} = 3MHz $\overline{LE}$ = LOW
I_{DDQ}	Quiescent V_{DD} Supply Current				200	µA	All V_{IN} = 0V or V_{DD}
I_{PP}	High Voltage Supply Current				0.50	mA	V_{PP} = 275V All outputs high
					0.50	mA	V_{PP} = 275V All outputs low
I_{IH}	High-Level Logic Input Current				10	µA	$V_{IH} = V_{DD}$
I_{IL}	Low-Level Logic Input Current				-10	µA	V_{IL} = 0V
V_{OH}	High-Level Output	HV_{OUT}	200			V	V_{PP} = 275V, IHV_{OUT} = -1mA
		Data Out	V_{DD} -1V			V	ID_{OUT} = -100µA
V_{OL}	Low-Level Output	HV_{OUT}			10	V	IHV_{OUT} = 1mA, V_{DD} = 5V
		Data Out			1.0	V	ID_{OUT} = 100µA
V_{OC}	HV_{OUT} Clamp Voltage				V_{PP} +1.5	V	I_{OL} = +5mA
					-1.5	V	I_{OL} = -5mA

AC Characteristics[1,2] (For V_{DD} = 5V; V_{PP} = 275V, T_A = 25°C)

Symbol	Parameter		Min	Typ	Max	Units	Conditions
f_{CLK}	Clock Frequency				6	MHz	
t_W	Clock Width High and Low	High	83			ns	
t_{SU}	Data Setup Time Before Clock Rises		35			ns	
t_H	Data Hold Time After Clock Rises		30			ns	
t_{WLE}	Width of Latch Enable Pulse		80			ns	
t_{DLE}	LE Delay Time Rising Edge of Clock		35			ns	
t_{SLE}	$\overline{LE}$ Setup Time Before Rising Edge of Clock		40			ns	
t_{ON}, t_{OFF}	$\overline{Time}$ from Latch Enable to HV_{OUT}				1.5	µs	C_L = 20pF
t_{DHL}	Delay Time Clock to Data High to Low				110	ns	C_L = 20pF
t_{DLH}	Delay Time Clock to Data Low to High				160	ns	C_L = 20pF
t_r, t_f	All Logic Inputs				5	ns	

Notes:
1. Shift register speed can be as low as DC as long as Data Set-up and Hold Time meet the spec.
2. AC Characteristics are guaranteed only under V_{DD} = 5V.

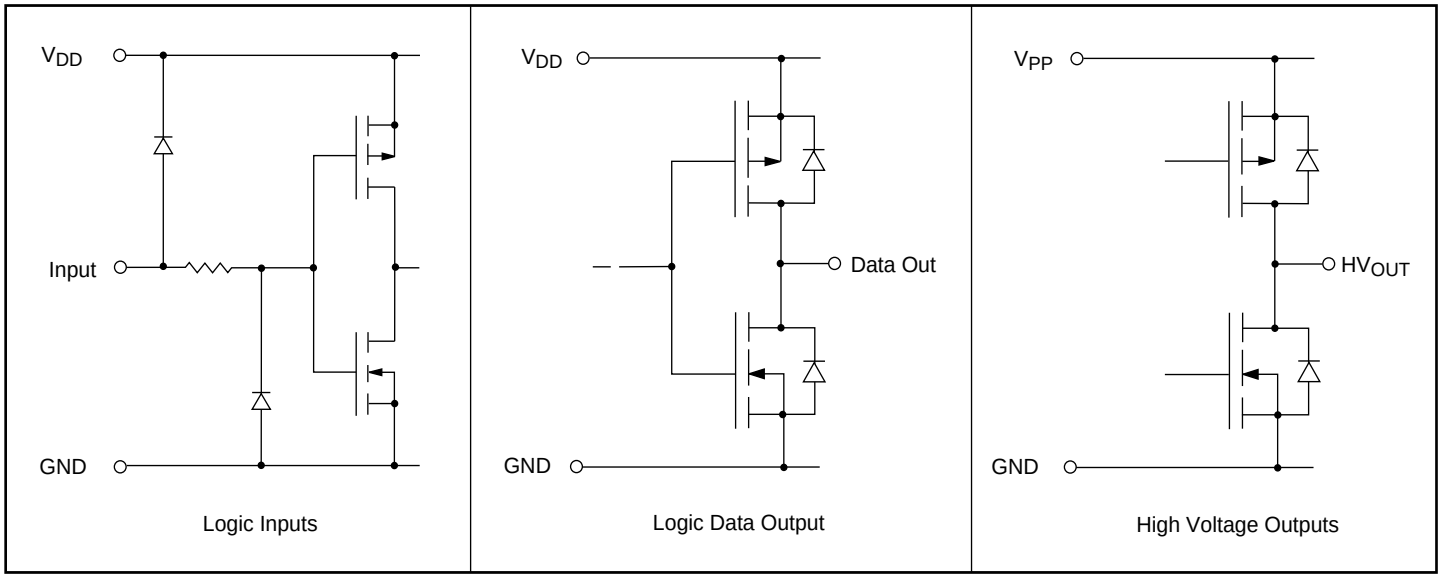
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Logic supply voltage	4.5	5.0	5.5	V
V_{PP}	High voltage supply	60		275	V
V_{IH}	High-level input voltage	V_{DD} -0.9		V_{DD}	V
V_{IL}	Low-level input voltage	0		0.9	V
T_A	Operating free-air temperature	0		+70	°C

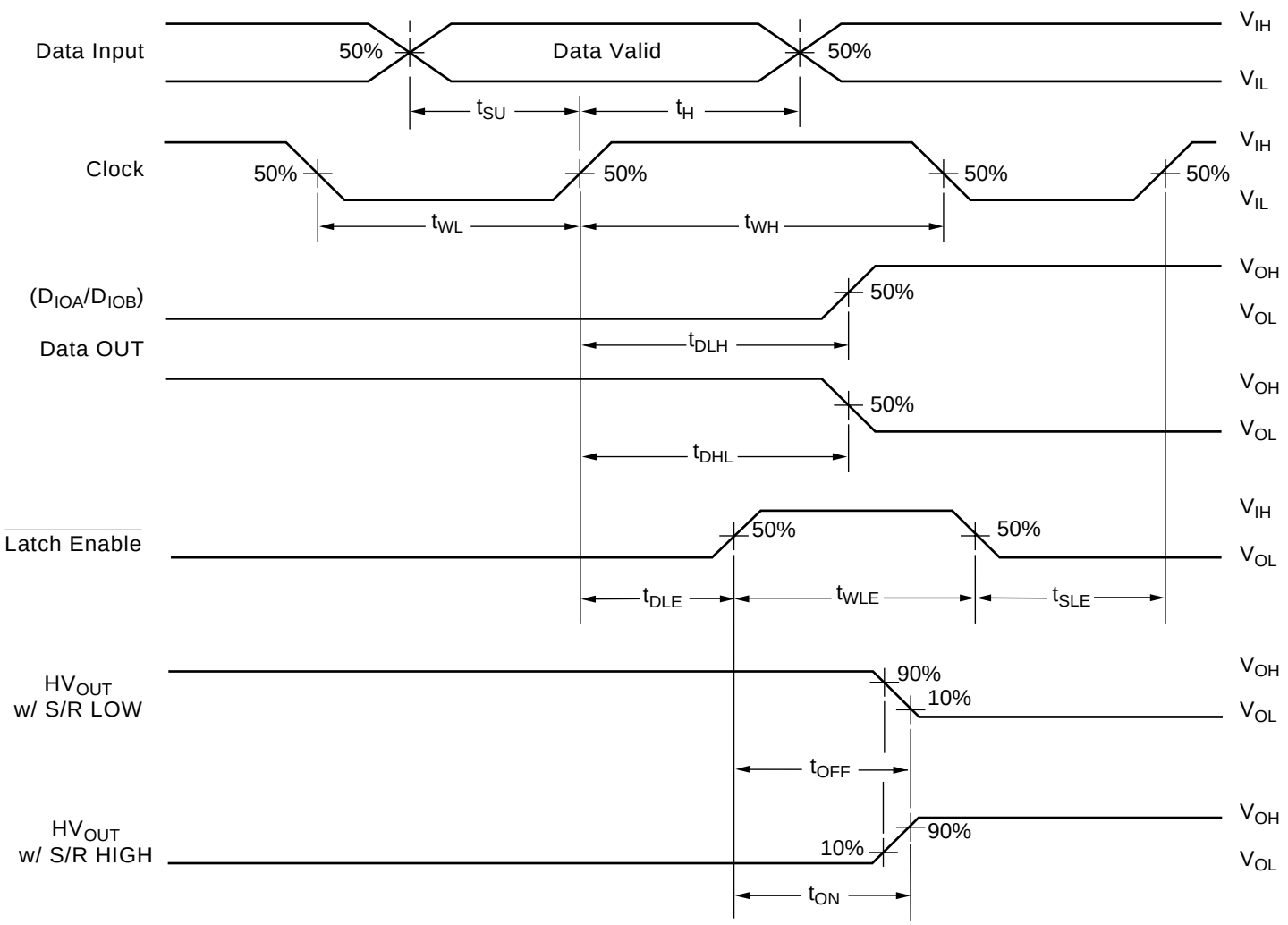
Notes:
Power-up sequence should be the following:
1. Connect ground.
2. Apply V_{DD}.
3. Set all inputs (Data, CLK, Enable, etc.) to a known state.
4. Apply V_{PP}.

Power-down sequence should be the reverse of the above.

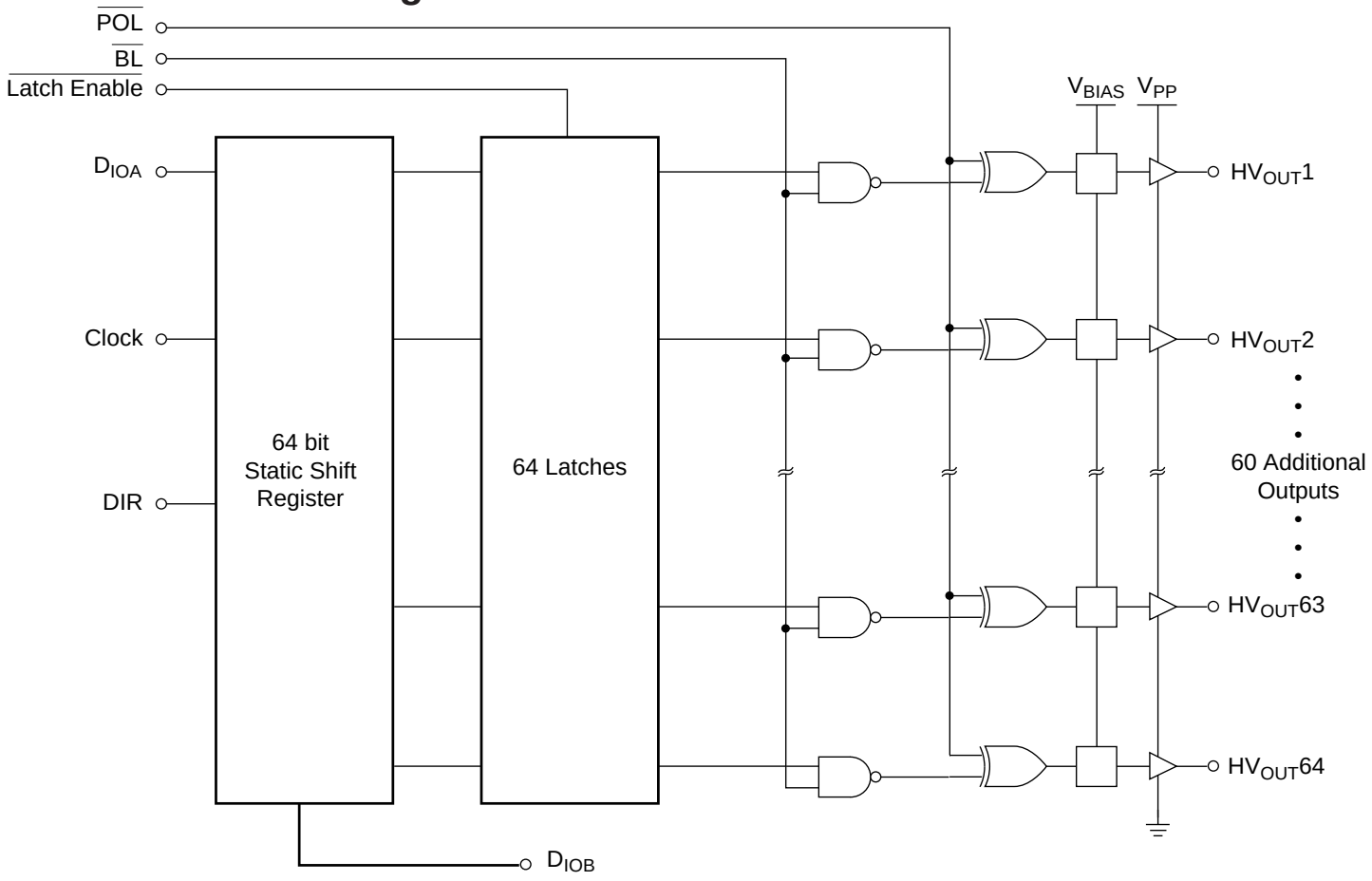
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



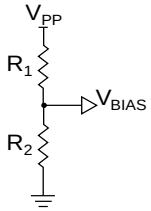
Function Table

Function	Inputs						Outputs				
	Data	CLK	$\overline{LE}$	$\overline{BL}$	$\overline{POL}$	DIR	Shift Reg 1	Shift Reg 2…64	HV Outputs 1	HV Outputs 2…64	Data Out *
All on	X	X	X	L	L	X	*	*…*	H	H…H	*
All off	X	X	X	L	H	X	*	*…*	L	L…L	*
Invert mode	X	X	L	H	L	X	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Load S/R	H or L	↑	L	H	H	X	H or L	*…*	*	*…*	*
Load/Store Data in Latches	X	X	↓	H	H	X	*	*…*	*	*…*	*
	X	X	↓	H	L	X	*	*…*	$\overline{*}$	$\overline{*…*}$	*
Transparent Latch mode	L	↑	H	H	H	X	L	*…*	L	*…*	*
	H	↑	H	H	H	X	H	*…*	H	*…*	*
I/O Relation	D_{IOA}	↑	X	X	X	L	Q_n→	Q_{n-1}	—		D_{IOB}
	D_{IOB}	↑	X	X	X	H	Q_n→	Q_{n+1}	—		D_{IOA}

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition, ↓ = high-to-low transition.
* = dependent on previous stage's state before the last CLK or last $\overline{LE}$ high.

V_{BIAS} Table

V_{BIAS} Voltage	V_{PP} Operating Voltage
V_{BIAS} = 0V or V_{PP}	V_{PP} = 200V
$V_{BIAS} = \frac{V_{PP}}{2}V$	V_{PP} = 275V



V_{PP} can be used with a voltage divider to get V_{BIAS} or a separate voltage supply can be used for V_{BIAS}.

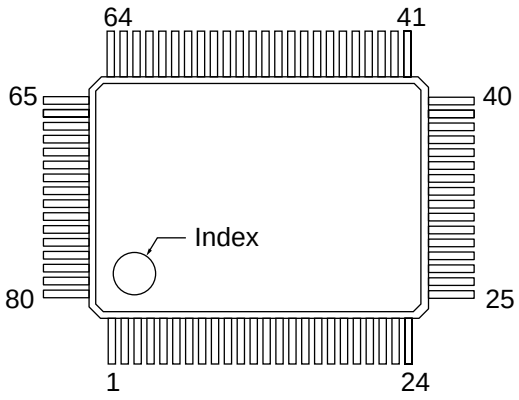
Pin Configurations

HV35

Pin	Function	Pin	Function
1	HV_{OUT} 41/24	41	HV_{OUT} 1/64
2	HV_{OUT} 42/23	42	HV_{OUT} 2/63
3	HV_{OUT} 43/22	43	HV_{OUT} 3/62
4	HV_{OUT} 44/21	44	HV_{OUT} 4/61
5	HV_{OUT} 45/20	45	HV_{OUT} 5/60
6	HV_{OUT} 46/19	46	HV_{OUT} 6/59
7	HV_{OUT} 47/18	47	HV_{OUT} 7/58
8	HV_{OUT} 48/17	48	HV_{OUT} 8/57
9	HV_{OUT} 49/16	49	HV_{OUT} 9/56
10	HV_{OUT} 50/15	50	HV_{OUT} 10/55
11	HV_{OUT} 51/14	51	HV_{OUT} 11/54
12	HV_{OUT} 52/13	52	HV_{OUT} 12/53
13	HV_{OUT} 53/12	53	HV_{OUT} 13/52
14	HV_{OUT} 54/11	54	HV_{OUT} 14/51
15	HV_{OUT} 55/10	55	HV_{OUT} 15/50
16	HV_{OUT} 56/9	56	HV_{OUT} 16/49
17	HV_{OUT} 57/8	57	HV_{OUT} 17/48
18	HV_{OUT} 58/7	58	HV_{OUT} 18/47
19	HV_{OUT} 59/6	59	HV_{OUT} 19/46
20	HV_{OUT} 60/5	60	HV_{OUT} 20/45
21	HV_{OUT} 61/4	61	HV_{OUT} 21/44
22	HV_{OUT} 62/3	62	HV_{OUT} 22/43
23	HV_{OUT} 63/2	63	HV_{OUT} 23/42
24	HV_{OUT} 64/1	64	HV_{OUT} 24/41
25	V_{PP}	65	HV_{OUT} 25/40
26	D_{IOA}	66	HV_{OUT} 26/39
27	N/C	67	HV_{OUT} 27/38
28	N/C	68	HV_{OUT} 28/37
29	$\overline{BL}$	69	HV_{OUT} 29/36
30	$\overline{POL}$	70	HV_{OUT} 30/35
31	V_{DD}	71	HV_{OUT} 31/34
32	DIR	72	HV_{OUT} 32/33
33	V_{BIAS}	73	HV_{OUT} 33/32
34	GND	74	HV_{OUT} 34/31
35	N/C	75	HV_{OUT} 35/30
36	N/C	76	HV_{OUT} 36/29
37	$\overline{CLK}$	77	HV_{OUT} 37/28
38	$\overline{LE}$	78	HV_{OUT} 38/27
39	D_{IOB}	79	HV_{OUT} 39/26
40	V_{PP}	80	HV_{OUT} 40/25

Note:
Pin designation for DIR = H/L
Example: for DIR = H, Pin 1 is HV_{OUT}41
for DIR = L, Pin 1 is HV_{OUT}24

Package Outline



top view

80-pin Gullwing Package