FLASH-ROM MODULE 8MByte (2M x 32-Bit), 80pin-SIMM, 5V
Part No. HF08-CS2501

GENERAL DESCRIPTION

The HF08-CS2501 is a high-speed flash read only memory (FROM) module containing 2,097,152 words organized in a x32bit configuration. The module consists of four 2M x 8bit FROM mounted on a 80-pin, single-sided, FR4-printed circuit board.

Commands are written to the command register using standard microprocessor write timings.

Register contents serve as input to an internal state-machine, which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Output enable (/OE) and write enable (/WE) can set the memory input and output.

When FROM module is disable condition the module is becoming power standby mode, system designer can get low -power design. All module components may be powered from a single +5V DC power supply and all inputs and outputs are TTL -compatible.

FEATURES

- Access time : 75, 90 and 120ns
- High-density 8MByte design
- High-reliability, low-power design
- Single + 5V ± 0.5V power supply
- Easy memory expansion
- All inputs and outputs are TTL-compatible
- FR4-PCB design
- Low profile 72-pin SIMM
- Minimum 1,000,000 write/erase cycle
- Sectors erase architecture
- Sector group protection
- Temporary sector group unprotection
- The used device is Am29F016B

OPTIONS MARKING

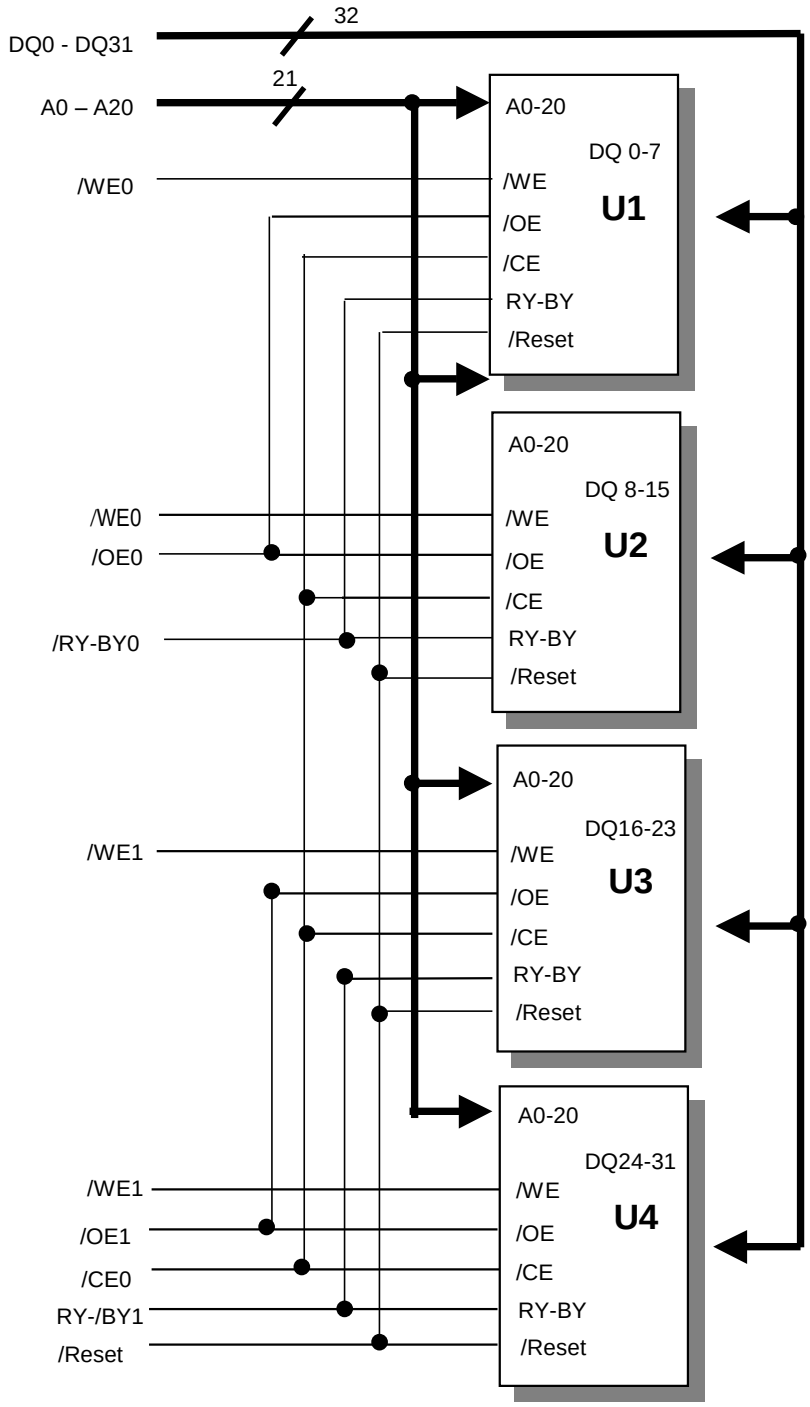
- Timing
  - 90ns access -90
- Packages
  - 80-pin SIMM M

PIN ASSIGNMENT

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	VSS	28	DQ14	55	A17
2	VCC	29	DQ13	56	A18
3	NC	30	DQ12	57	A19
4	A3	31	DQ11	58	A20
5	A2	32	DQ10	59	/CE1
6	A1	33	DQ9	60	/WE1
7	A0	34	DQ8	61	/OE1
8	DQ0	35	/CE0	62	VSS
9	DQ1	36	VCC	63	DQ24
10	DQ2	37	PD5	64	DQ25
11	DQ3	38	A11	65	DQ26
12	VSS	39	A12	66	DQ27
13	DQ4	40	A13	67	DQ28
14	DQ5	41	A14	68	DQ29
15	DQ6	42	A15	69	DQ30
16	DQ7	43	VSS	70	DQ31
17	/OE0	44	DQ16	71	NC
18	/WE0	45	DQ17	72	VCC
19	A4	46	DQ18	73	NC
20	A5	47	DQ19	74	NC
21	A6	48	DQ20	75	PD1
22	A7	49	DQ21	76	PD2
23	A8	50	DQ22	77	PD3
24	A9	51	DQ23	78	VSS
25	VSS	52	NC	79	PD4
26	A10	53	A16	80	VSS
27	DQ15	54	VSS		

80-PIN SIMM
TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	/OE	/CE	/WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
READ	L	L	H	Q	ACTIVE
WRITE or ERASE	X	L	L	D	ACTIVE

NOTE: X means don't care

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING
Voltage with respect to ground all other pins	$V_{IN,OUT}$	-2.0V to +7.0V
Voltage with respect to ground Vcc	V_{CC}	-2.0V to +7.0V
Storage Temperature	T_{STG}	-65°C to +125°C
Operating Temperature	T_A	-55°C to +125°C
Power Dissipation	P_D	4W

w Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP.	MAX
Vcc for ± 10% device Supply Voltages	Vcc	4.5V		5.5V
Ground	V_{SS}	0	0	0

DC AND OPERATING CHARACTERISTICS ($0°C \le T_A \le 70°C$; Vcc = 5V ± 0.5V)

PARAMETER	TEST CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	Vcc=Vcc max, V_{IN}= GND to Vcc	I_{L1}		±1.0	µA
Output Leakage Current	Vcc=Vcc max, VOUT= GND to Vcc	I_{L0}		±1.0	µA
Output High Voltage	I_{OH} = -2.5mA, Vcc = Vcc min	V_{OH}	2.4		V
Output Low Voltage	I_{OL} = 12mA, Vcc =Vcc min	V_{OL}		0.45	V
Vcc Active Current for Read(1)	/CE = V_{IL}, /OE=V_{IH},	I_{CC1}		40	mA
Vcc Active Current for Program or Erase(2)	/CE = V_{IL}, /OE=V_{IH}	I_{CC2}		60	mA
Vcc Standby Current	/CE= V_{IH}	I_{CC3}		1.0	mA
Low Vcc Lock-Out Voltage		V_{LKO}	3.2	4.2	V

Notes:

1. The Icc current listed is typically less than 2mA/MHz, with /OE at V_{IH}.
2. Icc active while embedded algorithm (program or erase) is in progress
3. Maximum Icc current specifications are tested with Vcc=Vcc max

ERASE AND PROGRAMMING PERFORMANCE

PARAMETER	LIMITS			UNIT	COMMENTS
	MIN.	TYP.	MAX.		
Sector Erase Time	-	1	8	sec	Excludes 00H programming prior to erasure
Byte Programming Time	-	7	300	µs	Excludes system-level overhead
Chip Programming Time	-	14.4	43.2	sec	Excludes system-level overhead

TSOP CAPACITANCE

PARAMETER SYMBOL	PARAMETER DESCRIPTION	TEST SETUP	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes : Test conditions T_A = 25° C, f=1.0 MHz.

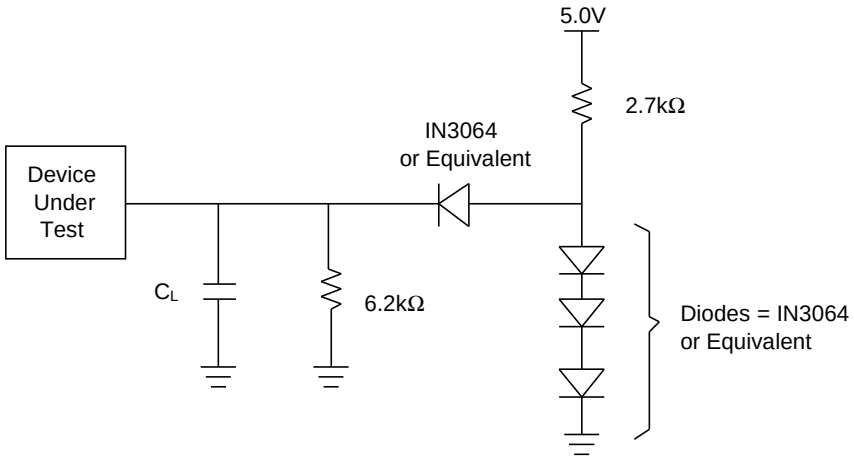
AC CHARACTERISTICS

u Read Only Operations Characteristics

PARAMETER SYMBOLS		DESCRIPTION	TEST SETUP		-75	-90	UNIT
JEDEC	STANDARD						
t_{AVAV}	t_{RC}	Read Cycle Time		Min	70	90	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	/CE = V_{IL} /OE = V_{IL}	Max	70	90	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	/OE = V_{IL}	Max	70	90	ns
t_{GLQV}	t_{OE}	Chip Enable to Output Delay		Max	40	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High-Z		Max	20	20	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High-Z		Max	20	20	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, /CE or /OE, Whichever Occurs First		Min	0	0	ns

TEST SPECIFICATIONS

TEST CONDITION	ALL SPEED OPTIONS	UNIT
Output load	1TTL gate	
Output load capacitance, C_L (Including jig capacitance)	100	pF
Input rise and full times	20	ns
Input pulse levels	0.45-2.4	V
Input timing measurement reference levels	0.8	V
Output timing measurement reference levels	2.0	V



Note : C_L = 100pF including jig capacitance

Erase/Program Operations

PARAMETER SYMBOLS		DESCRIPTION		-75	-90	UNIT
JEDEC	STANDARD					
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0	0	ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	7	7	μs

t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	1	1	sec
	t_{VCS}	Vcc set up time	Min	50	50	µs

Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

u Erase/Program Operations

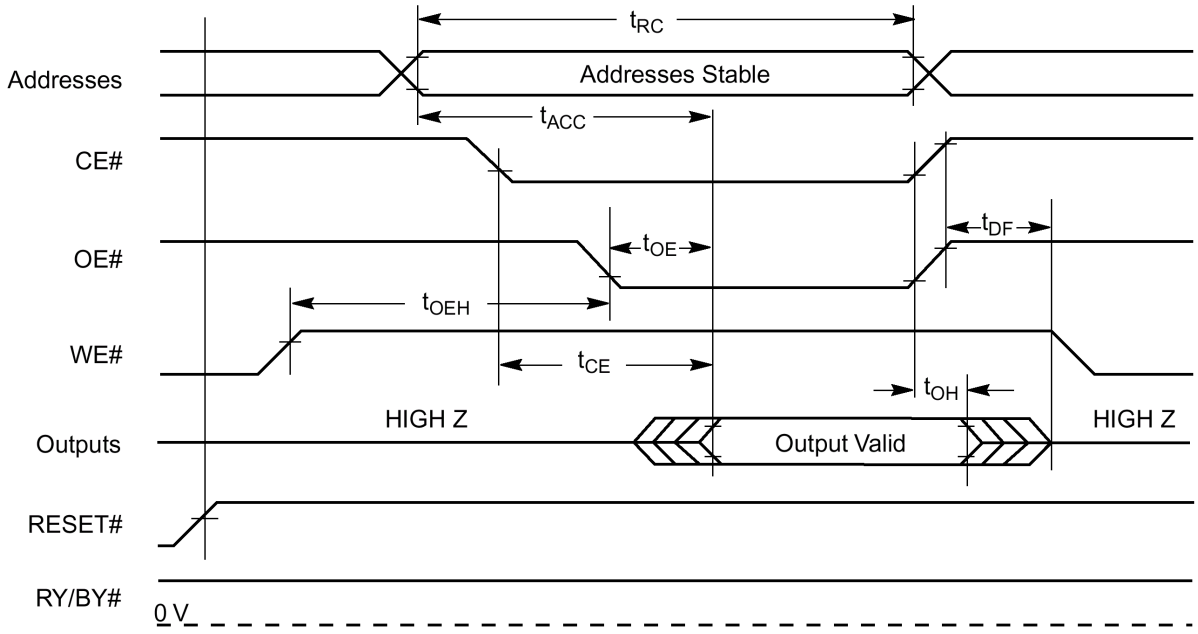
Alternate /CE Controlled Writes

PARAMETER SYMBOLS		DESCRIPTION		-75	-90	UNIT
JEDEC	STANDARD					
t_{AVAV}	t_{WC}	Write Cycle Time	Min	70	90	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	40	45	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	40	45	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	ns
t_{ELWL}	t_{CS}	/CE Setup Time	Min	0	0	ns
t_{WHEH}	t_{CH}	/CE Hold Time	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	40	45	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Typ	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note1)	Typ	1	1	sec

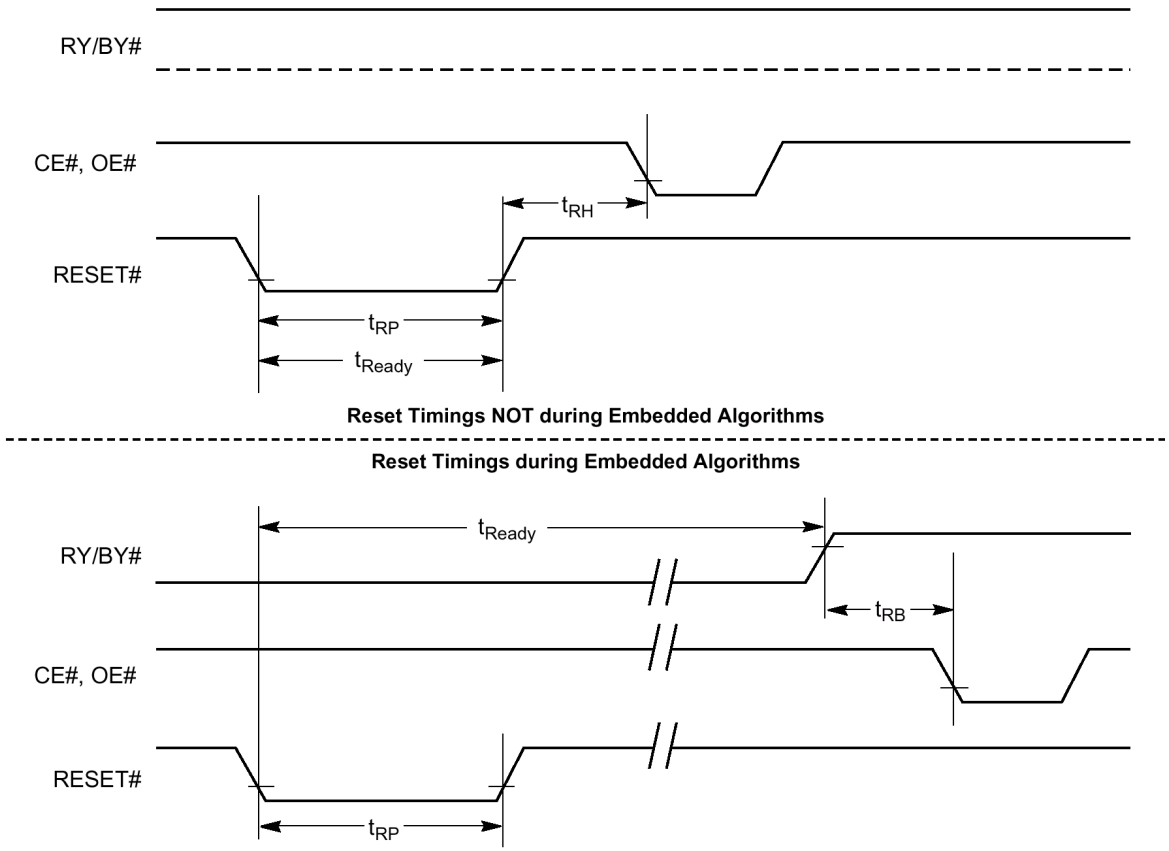
Notes :

1. This does not include the preprogramming time
2. This timing is only for Sector Protect operations

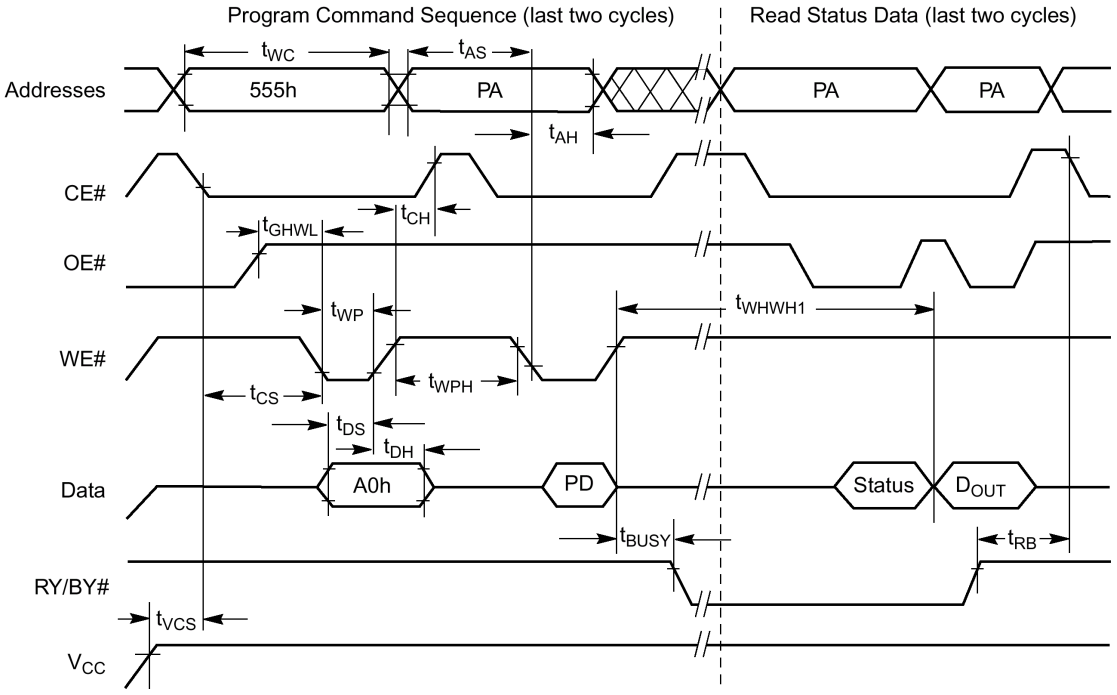
u READ OPERATIONS TIMING



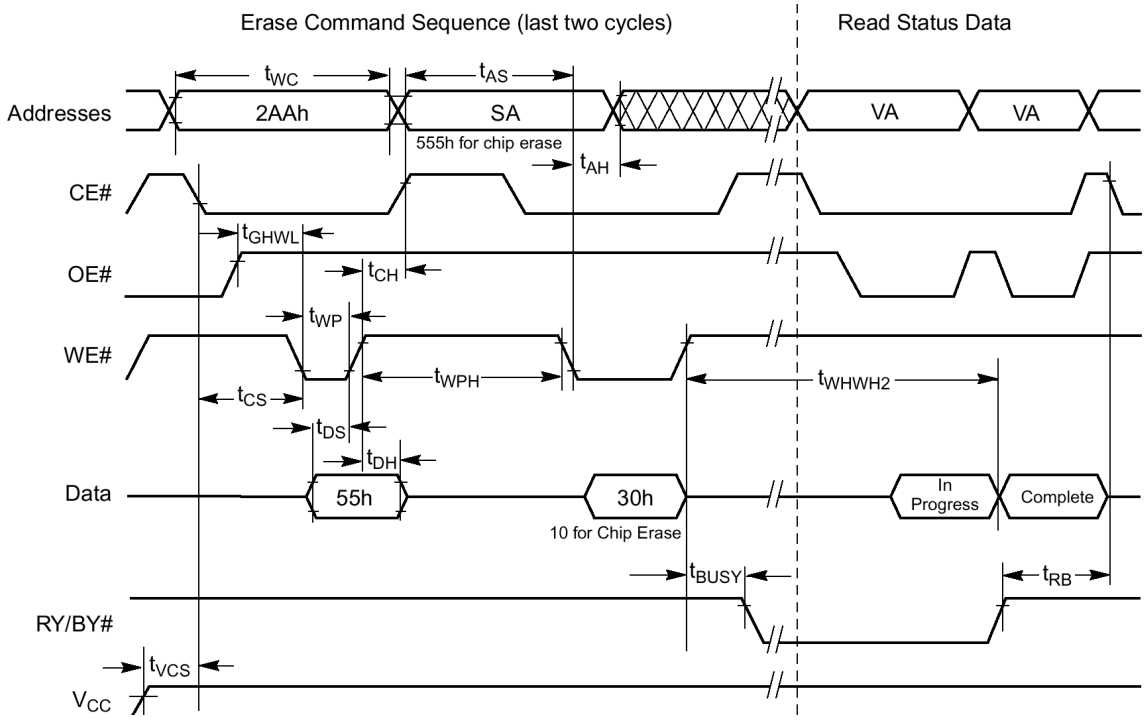
u RESET TIMING



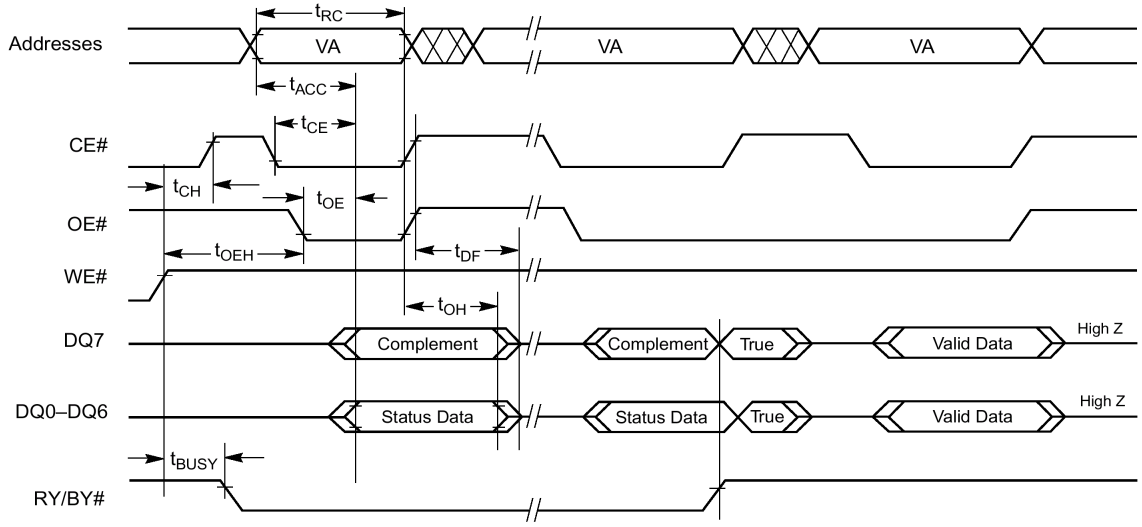
u PROGRAM OPERATIONS TIMING



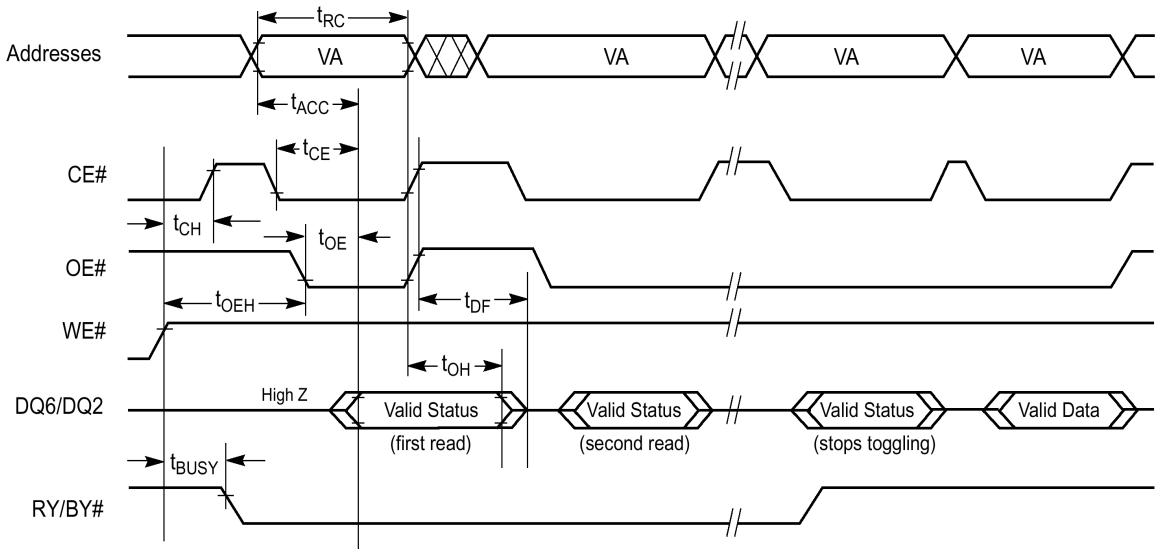
u CHIP/SECTOR ERASE OPERATION TIMINGS



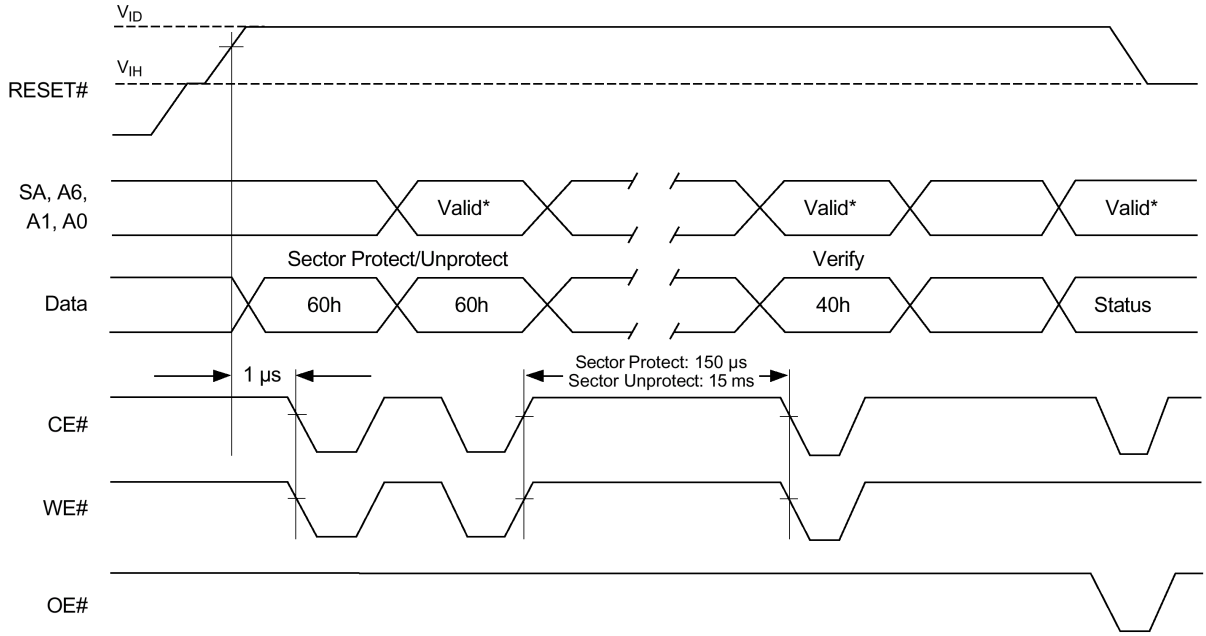
u DATA# POLLING TIMES(DURING EMBEDDED ALGORITHMS)



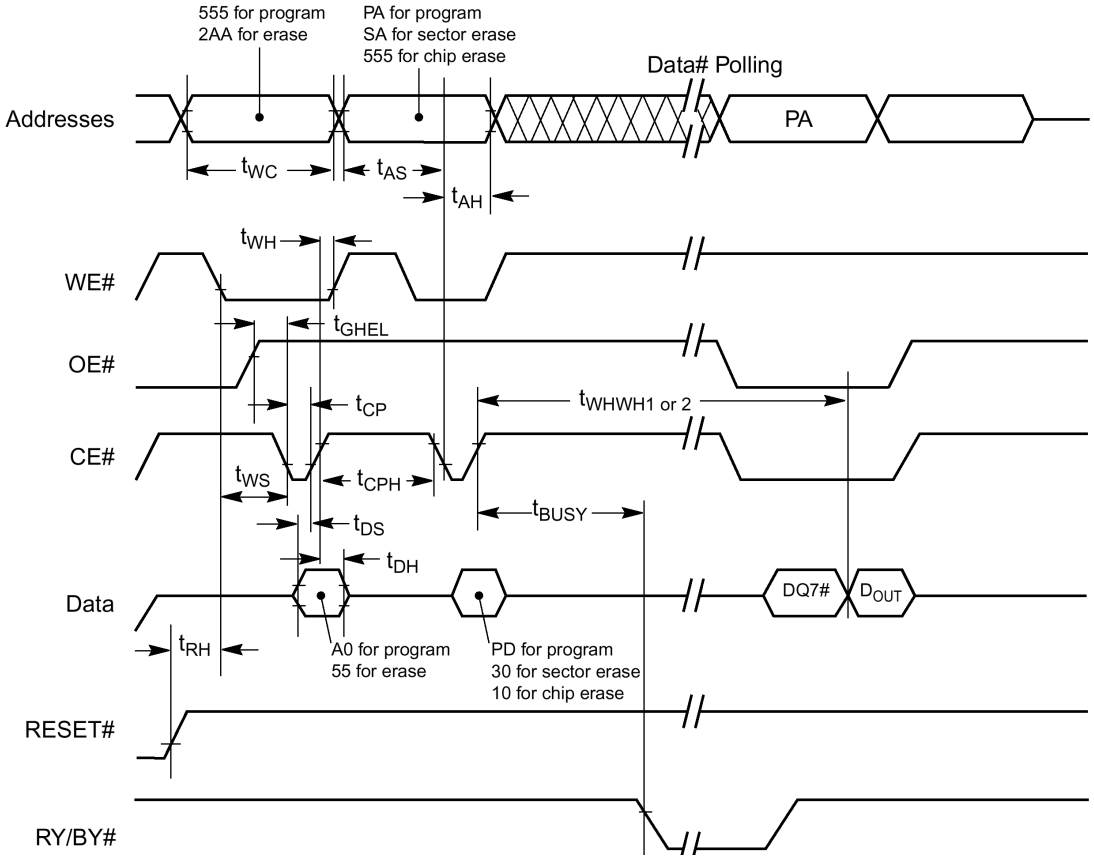
u TOGGLE# BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



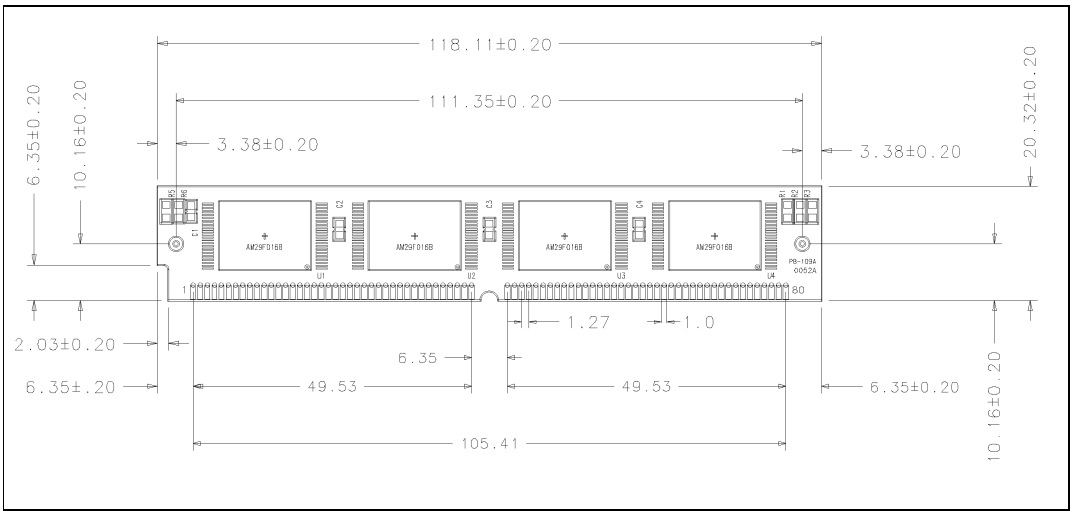
u SECTOR PROTECT UNPROTECT TIMEING DIAGRAM



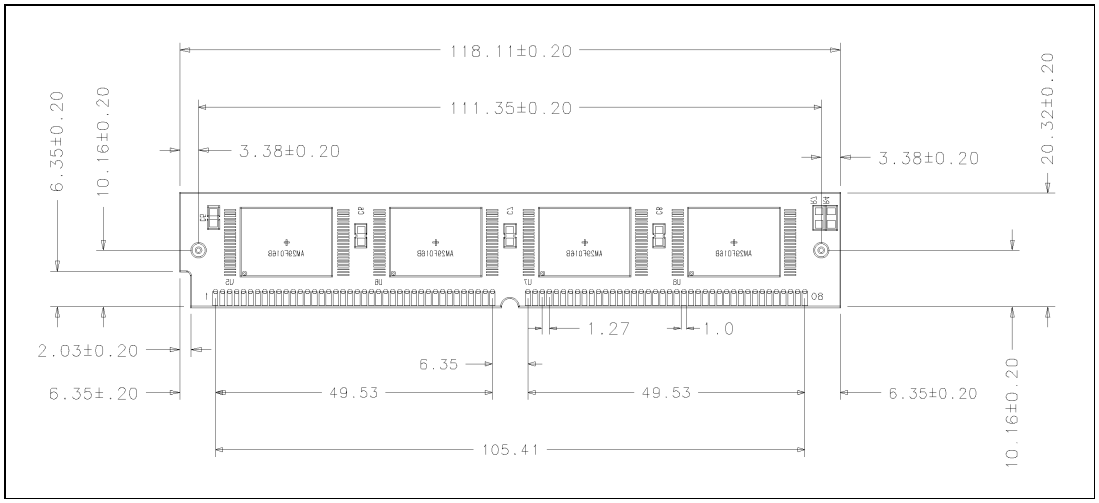
u ALTERNATE CE# CONTROLLED WRITE OPERATING TIMINGS



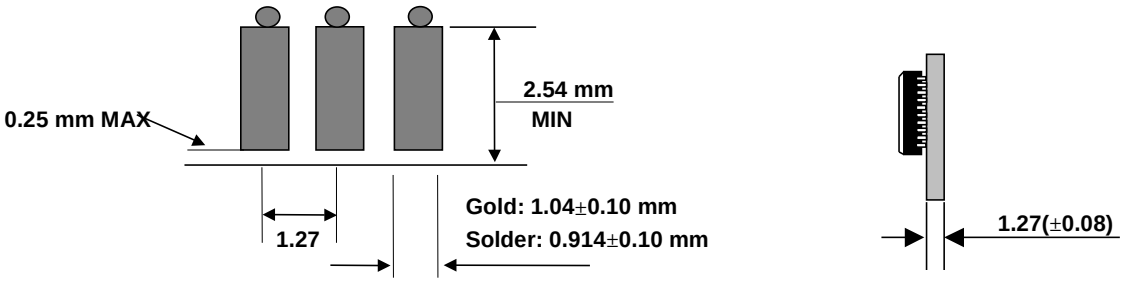
PACKAGE DIMENSIONS



<FRONT SIDE>



<REAR SIDE>



(Solder & Gold Plating)

ORDERING INFORMATION

Part Number	Density	Org.	Package	Component Number	Vcc	SPEED
HF08-CS2501	8MByte	2M×32bit	80Pin-SIMM	4EA	5.0V	90ns