GTL2008; GTL2107

12-bit GTL to LVTTL translator with power good control and high-impedance LVTTL and GTL outputs

Rev. 02 — 26 September 2006 Product data sheet

1. General description

The GTL2008/GTL2107 is a customized translator between dual Xeon processors, Platform Health Management, South Bridge and Power Supply LVTTL and GTL signals.

Functionally and footprint identical to the GTL2007, the GTL2008/GTL2107 LVTTL and GTL outputs were changed to put them into a high-impedance state when EN1 and EN2 are LOW, with the exception of 11BO because its normal state is LOW, so it is forced LOW. EN1 and EN2 will remain LOW until V_{CC} is at normal voltage, the other inputs are in valid states and VREF is at its proper voltage to assure that the outputs will remain high-impedance through power-up.

Both the GTL2008/GTL2107 and the GTL2007 are derived from the GTL2006. They add an enable function that disables the error output to the monitoring agent for platforms that monitor the individual error conditions from each processor. This enable function can be used so that false error conditions are not passed to the monitoring agent when the system is unexpectedly powered down. This unexpected power-down could be from a power supply overload, a CPU thermal trip, or some other event of which the monitoring agent is unaware.

A typical implementation would be to connect each enable line to the system power good signal or the individual enables to the VRD power good for each processor.

Typically Xeon processors specify a V_{TT} of 1.1 V to 1.2 V, as well as a nominal V_{ref} of 0.73 V to 0.76 V. To allow for future voltage level changes that may extend V_{ref} to 0.63 of V_{TT} (minimum of 0.693 V with V_{TT} of 1.1 V) the GTL2008/GTL2107 allows a minimum V_{ref} of 0.66 V. Characterization results show that there is little DC or AC performance variation between these levels.

The GTL2008 is the companion chip to the GTL2009 3-bit GTL Front-Side Bus frequency comparator that is used in dual-processor Xeon applications.

The GTL2107 is the Intel designation for the GTL2008.

2. Features

- Operates as a GTL to LVTTL sampling receiver or LVTTL to GTL driver
- EN1 and EN2 disable error output
- All LVTTL and GTL outputs are put in a high-impedance state when EN1 and EN2 are LOW
- 3.0 V to 3.6 V operation
- LVTTL I/O not 5 V tolerant

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- Series termination on the LVTTL outputs of 30 Ω
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115, and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 Class II, Level A which exceeds 500 mA
- Package offered: TSSOP28

3. Quick reference data

Table 1. Quick reference data

T_{amb} = 25 °C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{io}	input/output capacitance	A port; V_O = 3.0 V or 0 V	-	2.5	3.5	pF
		B port; V_O = V_{TT} or 0 V	-	1.5	2.5	pF
V_{ref} = 0.73 V; V_{TT} = 1.1 V						
t_{PLH}	LOW-to-HIGH propagation delay	nA to nBI; see Figure 4	1	4	8	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14	2	13	18	ns
t_{PHL}	HIGH-to-LOW propagation delay	nA to nBI; see Figure 4	2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14	2	4	10	ns
V_{ref} = 0.76 V; V_{TT} = 1.2 V						
t_{PLH}	LOW-to-HIGH propagation delay	nA to nBI; see Figure 4	1	4	8	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14	2	13	18	ns
t_{PHL}	HIGH-to-LOW propagation delay	nA to nBI; see Figure 4	2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14	2	4	10	ns

4. Ordering information

Table 2. Ordering information

T_{amb} = −40 °C to +85 °C

Type number	Topside mark	Package		
		Name	Description	Version
GTL2008PW	GTL2008	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1
GTL2107PW	GTL2107	TSSOP28	plastic thin shrink small outline package; 28 leads; body width 4.4 mm	SOT361-1

The GTL2107 is the Intel designation for the GTL2008 and is identical to the GTL2008 except for the type number and the topside markings.

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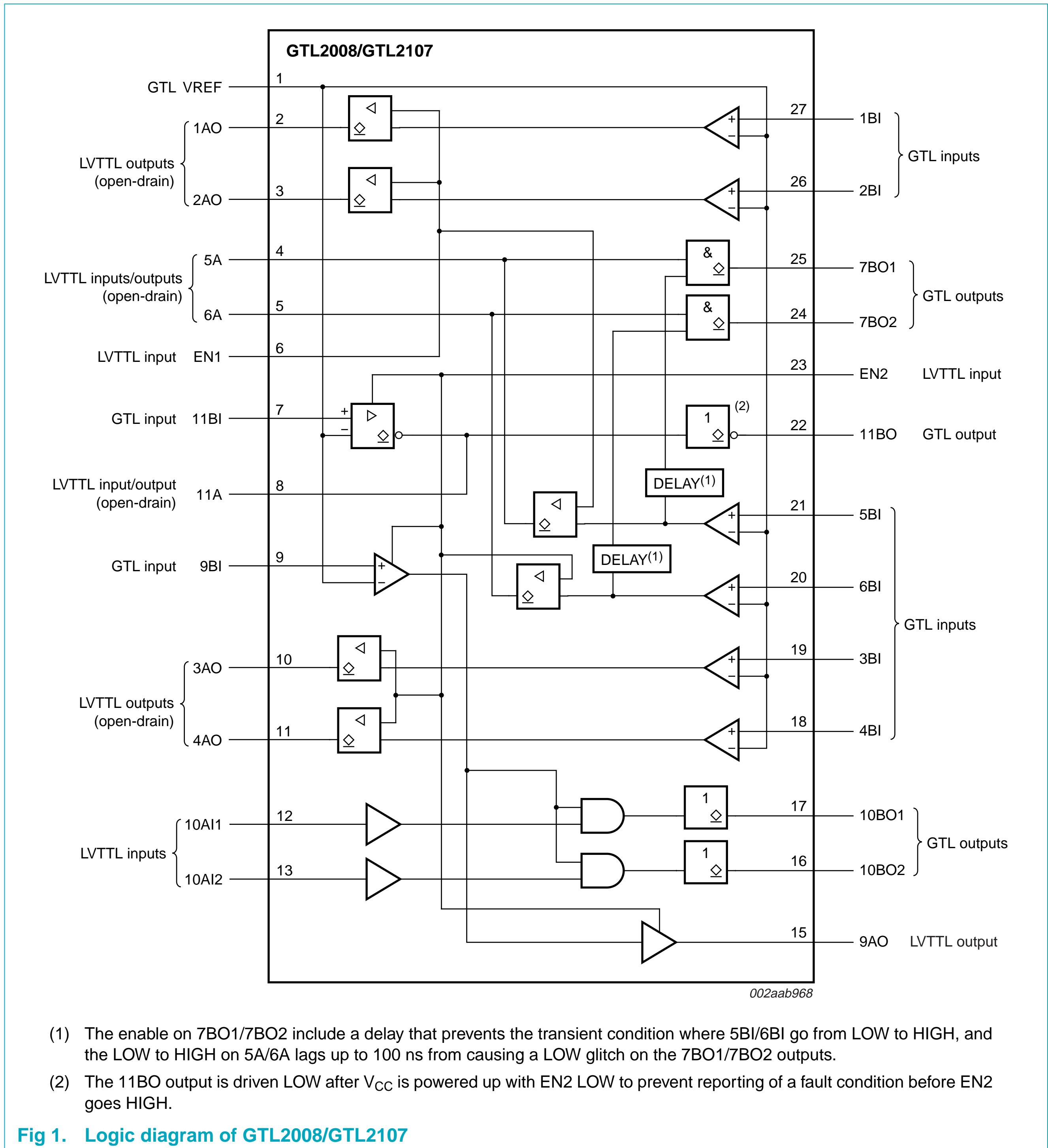
5. Functional diagram



(1) The enable on 7BO1/7BO2 include a delay that prevents the transient condition where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns from causing a LOW glitch on the 7BO1/7BO2 outputs.

(2) The 11BO output is driven LOW after V_{CC} is powered up with EN2 LOW to prevent reporting of a fault condition before EN2 goes HIGH.

Fig 1. Logic diagram of GTL2008/GTL2107

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6. Pinning information

6.1 Pinning

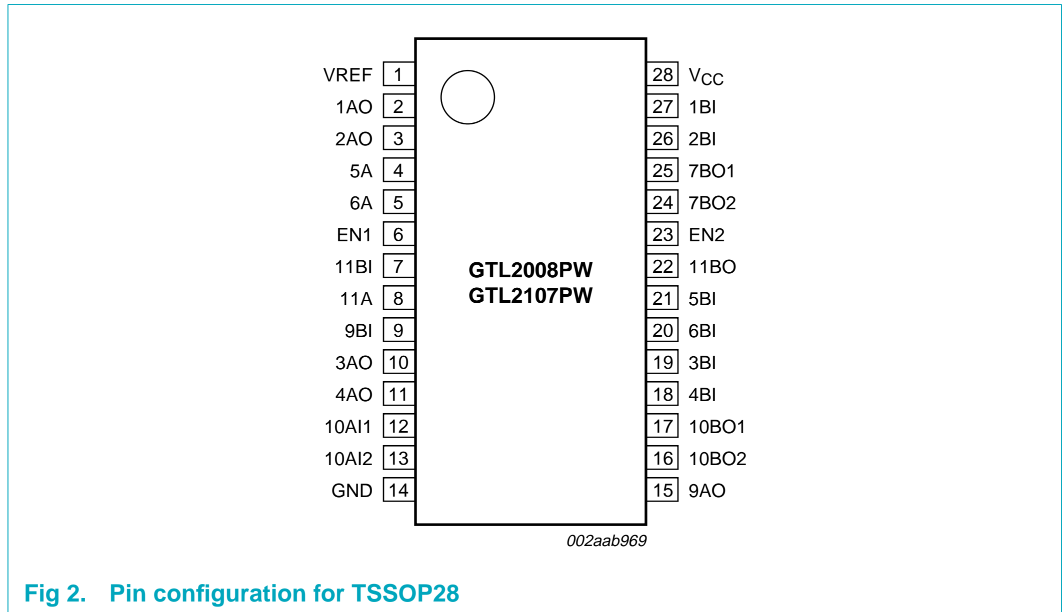

Fig 2. Pin configuration for TSSOP28

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VREF	1	GTL reference voltage
1AO	2	data output (LVTTL), open-drain
2AO	3	data output (LVTTL), open-drain
5A	4	data input/output (LVTTL), open-drain
6A	5	data input/output (LVTTL), open-drain
EN1	6	enable input (LVTTL)
11BI	7	data input (GTL)
11A	8	data input/output (LVTTL), open-drain
9BI	9	data input (GTL)
3AO	10	data output (LVTTL), open-drain
4AO	11	data output (LVTTL), open-drain
10AI1	12	data input (LVTTL)
10AI2	13	data input (LVTTL)
GND	14	ground (0 V)
9AO	15	data output (LVTTL), 3-state
10BO2	16	data output (GTL)
10BO1	17	data output (GTL)
4BI	18	data input (GTL)
3BI	19	data input (GTL)

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Table 3. Pin description *…continued*

Symbol	Pin	Description
6BI	20	data input (GTL)
5BI	21	data input (GTL)
11BO	22	data output (GTL)
EN2	23	enable input (LVTTL)
7BO2	24	data output (GTL)
7BO1	25	data output (GTL)
2BI	26	data input (GTL)
1BI	27	data input (GTL)
V_{CC}	28	positive supply voltage

7. Functional description

Refer to Figure 1 “Logic diagram of GTL2008/GTL2107”.

7.1 Function tables

Table 4. GTL input signals

H = HIGH voltage level; L = LOW voltage level.

Input	Output[1]
1BI/2BI/3BI/4BI/9BI	**1AO/2AO/3AO/4AO/9AO**
L	L
H	H

[1] 1AO, 2AO, 3AO, 4AO and 5A/6A condition changed by ENn power good signal as described in Table 5 and Table 6.

Table 5. EN1 power good signal

H = HIGH voltage level; L = LOW voltage level.

EN1	1AO and 2AO	5A
L	1BI and 2BI disconnected (high-Z)	5BI disconnected
H	follows BI	5BI connected

Table 6. EN2 power good signal

H = HIGH voltage level; L = LOW voltage level.

EN2	3AO and 4AO	6A
L	3BI and 4BI disconnected (high-Z)	6BI disconnected
H	follows BI	6BI connected

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Table 7. SMI signals
H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs			Output
10AI1/10AI2	EN2	9BI	10BO1/10BO2
L	H	L	L
L	H	H	L
H	H	L	L
H	H	H	H
L	L	X	L
H	L	X	H

Table 8. PROCHOT signals
H = HIGH voltage level; L = LOW voltage level.

Input	Input/output	Output
5BI/6BI	5A/6A (open-drain)	7BO1/7BO2
L	L	H[1]
H	L[2]	L
H	H	H

[1] The enable on 7BO1/7BO2 includes a delay that prevents the transient condition where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns from causing a low glitch on the 7BO1/7BO2 outputs.

[2] Open-drain input/output terminal is driven to logic LOW state by other driver.

Table 9. NMI signals
H = HIGH voltage level; L = LOW voltage level; X = Don't care.

Inputs		Input/output	Output
11BI	EN2	11A (open-drain)	11BO
L	H	H	L
L	H	L[1]	H
H	H	L	H
X	L	H	L
X	L	L[1]	H

[1] Open-drain input/output terminal is driven to logic LOW state by other driver.

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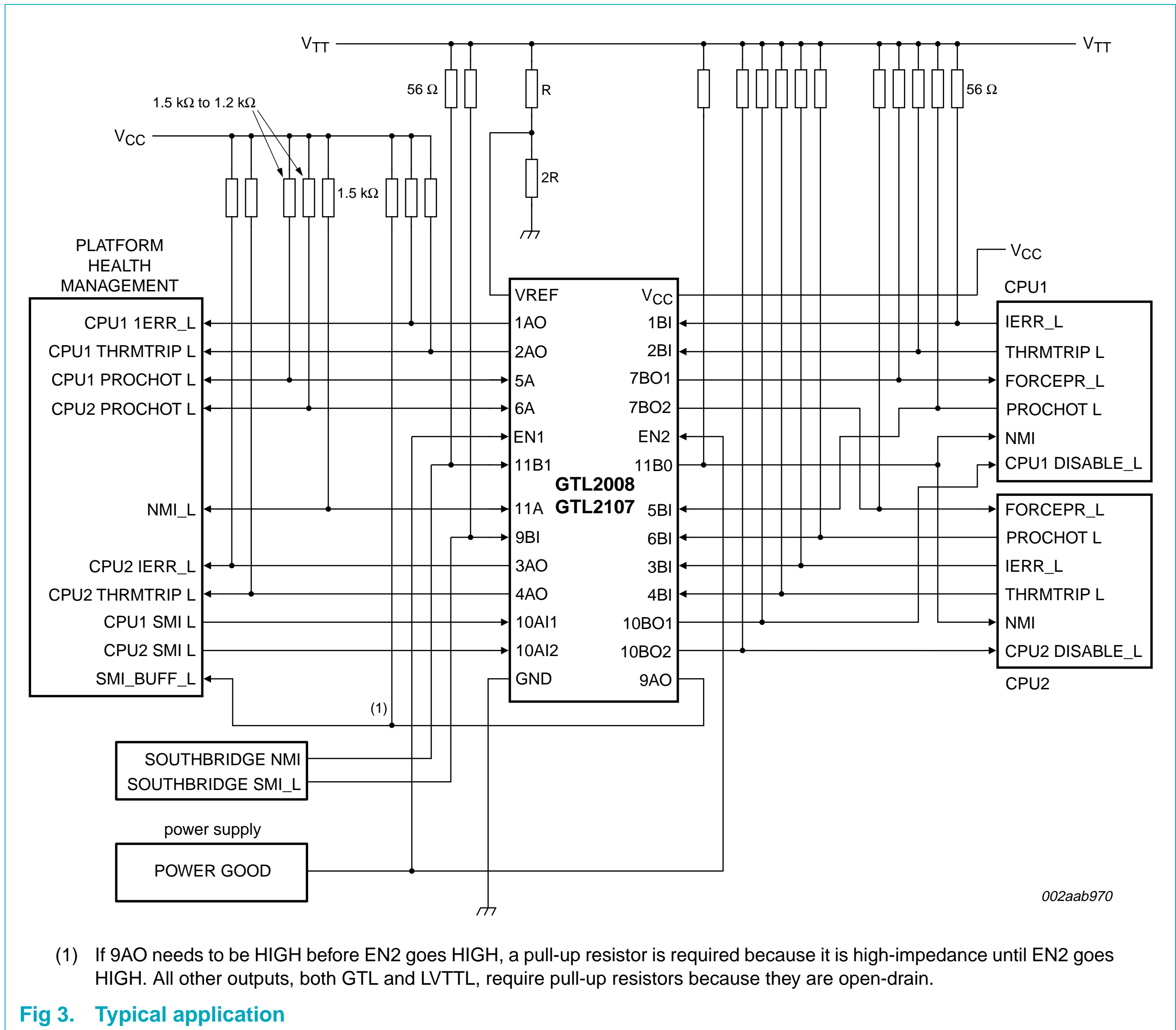
8. Application design-in information



(1) If 9AO needs to be HIGH before EN2 goes HIGH, a pull-up resistor is required because it is high-impedance until EN2 goes HIGH. All other outputs, both GTL and LVTTL, require pull-up resistors because they are open-drain.

Fig 3. Typical application

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9. Limiting values

Table 10. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		–0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-	–50	mA
V_I	input voltage	A port (LVTTL)	–0.5[1]	+4.6	V
		B port (GTL)	–0.5[1]	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-	–50	mA
V_O	output voltage	output in OFF or HIGH state; A port	–0.5[1]	+4.6	V
		output in OFF or HIGH state; B port	–0.5[1]	+4.6	V
I_{OL}	LOW-level output current[2]	A port	-	32	mA
		B port	-	30	mA
I_{OH}	HIGH-level output current[3]	A port	-	–32	mA
T_{stg}	storage temperature		–60	+150	°C
$T_{j(max)}$	maximum junction temperature	[4]	-	+125	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] Current into any output in the LOW state.

[3] Current into any output in the HIGH state.

[4] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

10. Recommended operating conditions

Table 11. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		3.0	3.3	3.6	V
V_{TT}	termination voltage	GTL	-	1.2	-	V
V_{ref}	reference voltage	GTL	0.64	0.8	1.1	V
V_I	input voltage	A port	0	3.3	3.6	V
		B port	0	V_{TT}	3.6	V
V_{IH}	HIGH-level input voltage	A port and ENn	2	-	-	V
		B port	V_{ref} + 0.050	-	-	V
V_{IL}	LOW-level input voltage	A port and ENn	-	-	0.8	V
		B port	-	-	V_{ref} – 0.050	V
I_{OH}	HIGH-level output current	A port	-	-	–16	mA
I_{OL}	LOW-level output current	A port	-	-	16	mA
		B port	-	-	15	mA
T_{amb}	ambient temperature	operating in free-air	–40	-	+85	°C

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11. Static characteristics

Table 12. Static characteristics

Recommended operating conditions; voltages are referenced to GND (ground = 0 V). T_{amb} = −40 °C to +85 °C

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{OH}	HIGH-level output voltage	9AO; V_{CC} = 3.0 V to 3.6 V; I_{OH} = −100 μA	[2]	V_{CC} − 0.2	3.0	-	V
		9AO; V_{CC} = 3.0 V; I_{OH} = −16 mA	[2]	2.1	2.3	-	V
V_{OL}	LOW-level output voltage	A port; V_{CC} = 3.0 V; I_{OL} = 4 mA	[2]	-	0.15	0.4	V
		A port; V_{CC} = 3.0 V; I_{OL} = 8 mA	[2]	-	0.3	0.55	V
		A port; V_{CC} = 3.0 V; I_{OL} = 16 mA	[2]	-	0.6	0.8	V
		B port; V_{CC} = 3.0 V; I_{OL} = 15 mA	[2]	-	0.13	0.4	V
I_{OH}	HIGH-level output current	open-drain outputs; A port other than 9AO; V_O = V_{CC}; V_{CC} = 3.6 V		-	-	±1	μA
I_I	input current	A port; V_{CC} = 3.6 V; V_I = V_{CC}		-	-	±1	μA
		A port; V_{CC} = 3.6 V; V_I = 0 V		-	-	±1	μA
		B port; V_{CC} = 3.6 V; V_I = V_{TT} or GND		-	-	±1	μA
I_{CC}	supply current	A or B port; V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 mA		-	8	12	mA
ΔI_{CC}[3]	additional supply current	per input; A port or control inputs; V_{CC} = 3.6 V; V_I = V_{CC} − 0.6 V		-	-	500	μA
C_{io}	input/output capacitance	A port; V_O = 3.0 V or 0 V		-	2.5	3.5	pF
		B port; V_O = V_{TT} or 0 V		-	1.5	2.5	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[3] This is the increase in supply current for each input that is at the specified LVTTL voltage level rather than V_{CC} or GND.

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12. Dynamic characteristics

Table 13. Dynamic characteristics

V_{CC} = 3.3 V ± 0.3 V

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{ref} = 0.73 V; V_{TT} = 1.1 V							
t_{PLH}	LOW-to-HIGH propagation delay	nA to nBI; see Figure 4		1	4	8	ns
		9BI to 9AO; see Figure 5		2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14		2	13	18	ns
		9BI to 10BOn		2	6	11	ns
		11A to 11BO; see Figure 10		1	4	8	ns
		11BI to 11A; see Figure 9		2	7.5	11	ns
		11BI to 11BO		2	8	13	ns
		5BI to 7BO1 or 6BI to 7BO2; see Figure 7		4	7	12	ns
t_{PHL}	HIGH-to-LOW propagation delay	nA to nBI; see Figure 4		2	5.5	10	ns
		9BI to 9AO; see Figure 5		2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14		2	4	10	ns
		9BI to 10BOn		2	6	11	ns
		11A to 11BO; see Figure 10		1	5.5	10	ns
		11BI to 11A; see Figure 9		2	8.5	13	ns
		11BI to 11BO	[2]	2	14	21	ns
		5BI to 7BO1 or 6BI to 7BO2; see Figure 7		100	205	350	ns
t_{PLZ}	LOW to OFF-state propagation delay	EN1 to nAO or EN2 to nAO; see Figure 8		1	3	10	ns
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see Figure 8		1	3	7	ns
t_{PZL}	OFF-state to LOW propagation delay	EN1 to nAO or EN2 to nAO; see Figure 8		2	7	10	ns
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see Figure 8		2	7	10	ns
t_{PHZ}	HIGH to OFF-state propagation delay	EN2 to 9AO; see Figure 11		2	5	10	ns
t_{PZH}	OFF-state to HIGH propagation delay	EN2 to 9AO; see Figure 11		1	4	10	ns

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Table 13. Dynamic characteristics *…continued*

V_{CC} = 3.3 V ± 0.3 V

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
V_{ref} = 0.76 V; V_{TT} = 1.2 V							
t_{PLH}	LOW-to-HIGH propagation delay	nA to nBI; see Figure 4		1	4	8	ns
		9BI to 9AO; see Figure 5		2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14		2	13	18	ns
		9BI to 10BOn		2	6	11	ns
		11A to 11BO; see Figure 10		1	4	8	ns
		11BI to 11A; see Figure 9		2	7.5	11	ns
		11BI to 11BO		2	8	13	ns
		5BI to 7BO1 or 6BI to 7BO2; see Figure 7		4	7	12	ns
t_{PHL}	HIGH-to-LOW propagation delay	nA to nBI; see Figure 4		2	5.5	10	ns
		9BI to 9AO; see Figure 5		2	5.5	10	ns
		nBI to nA or nAO (open-drain outputs); see Figure 14		2	4	10	ns
		9BI to 10BOn		2	6	11	ns
		11A to 11BO; see Figure 10		1	5.5	10	ns
		11BI to 11A; see Figure 9		2	8.5	13	ns
		11BI to 11BO	[2]	2	14	21	ns
		5BI to 7BO1 or 6BI to 7BO2; see Figure 7		100	205	350	ns
t_{PLZ}	LOW to OFF-state propagation delay	EN1 to nAO or EN2 to nAO; see Figure 8		1	3	10	ns
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see Figure 8		1	3	7	ns
t_{PZL}	OFF-state to LOW propagation delay	EN1 to nAO or EN2 to nAO; see Figure 8		2	7	10	ns
		EN1 to 5A (I/O) or EN2 to 6A (I/O); see Figure 8		2	7	10	ns
t_{PHZ}	HIGH to OFF-state propagation delay	EN2 to 9AO; see Figure 11		2	5	10	ns
t_{PZH}	OFF-state to HIGH propagation delay	EN2 to 9AO; see Figure 11		2	4	10	ns

[1] All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] Includes ~7.6 ns RC rise time of test load pull-up on 11A, 1.5 kΩ pull-up and 21 pF load on 11A has about 23 ns RC rise time.

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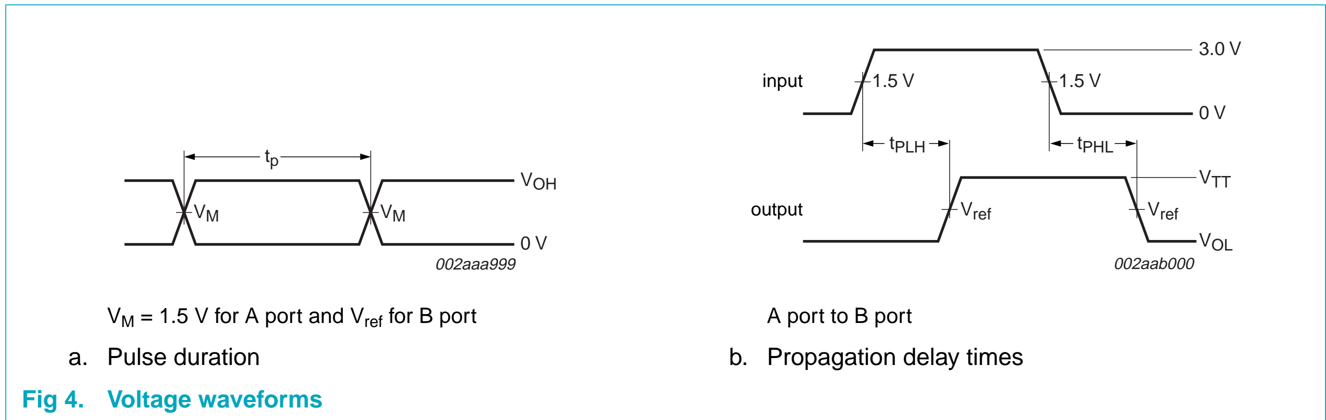
12.1 Waveforms

V_M = 1.5 V at V_{CC} ≥ 3.0 V for A ports; V_M = V_{ref} for B ports.



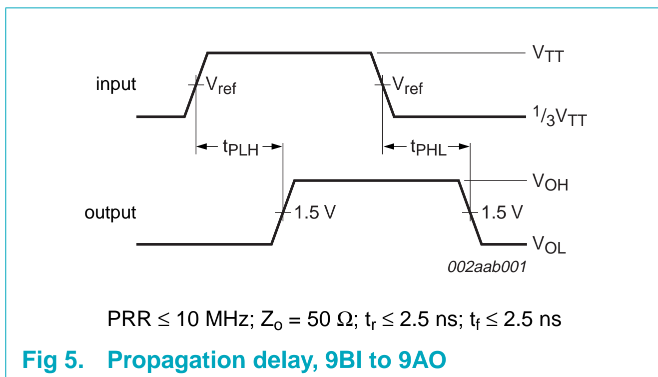
V_M = 1.5 V for A port and V_{ref} for B port

a. Pulse duration

A port to B port

b. Propagation delay times

Fig 4. Voltage waveforms



PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns

Fig 5. Propagation delay, 9BI to 9AO

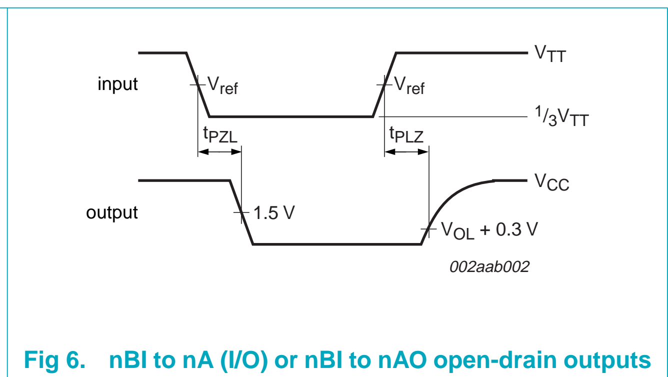


Fig 6. nBI to nA (I/O) or nBI to nAO open-drain outputs

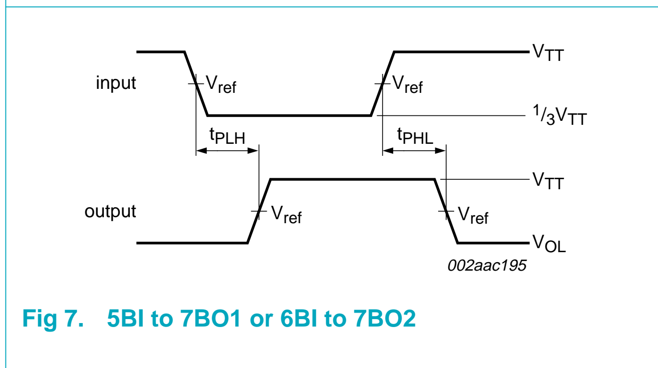


Fig 7. 5BI to 7BO1 or 6BI to 7BO2

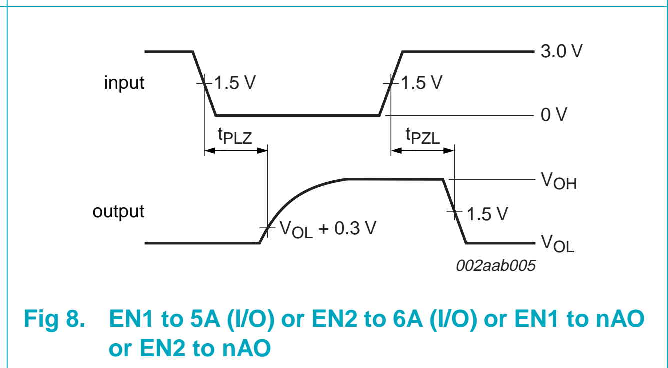


Fig 8. EN1 to 5A (I/O) or EN2 to 6A (I/O) or EN1 to nAO or EN2 to nAO

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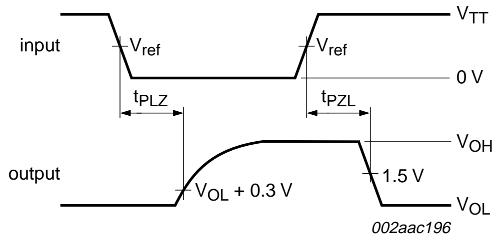

Fig 9. 11BI to 11A

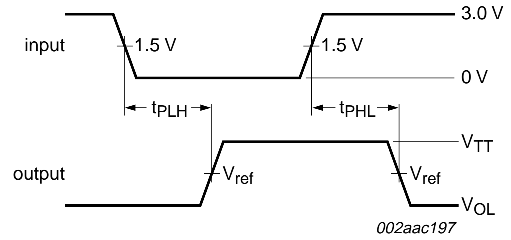

Fig 10. 11A to 11BO

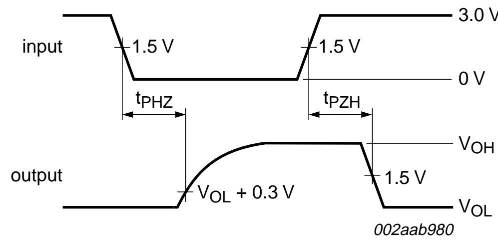

Fig 11. EN2 to 9AO

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13. Test information

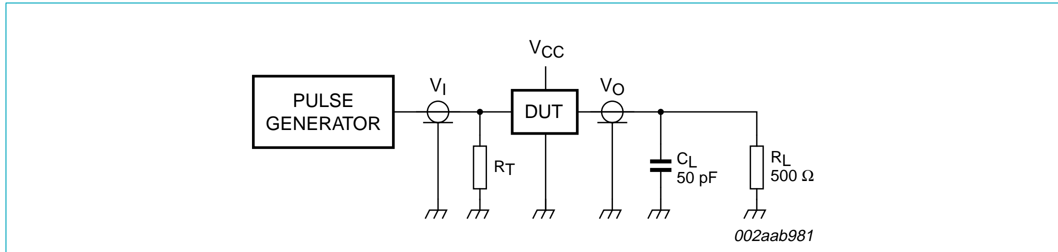

Fig 12. Load circuit for A outputs (9AO)

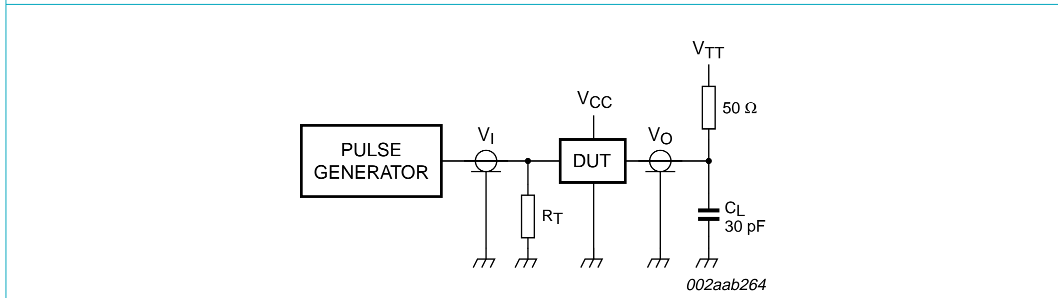

Fig 13. Load circuit for B outputs

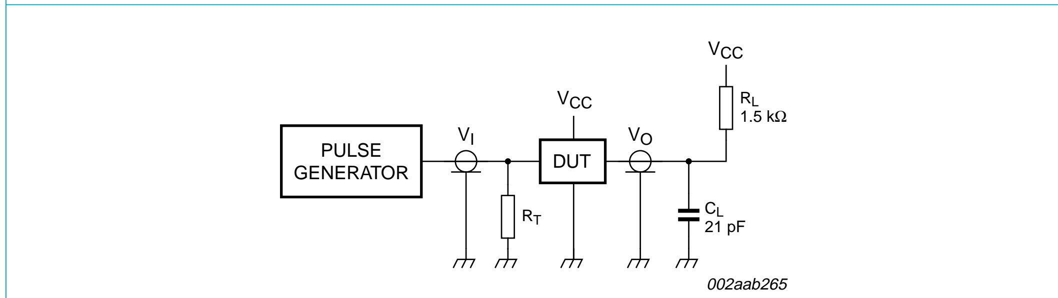

Fig 14. Load circuit for open-drain LVTTL I/O and open-drain outputs

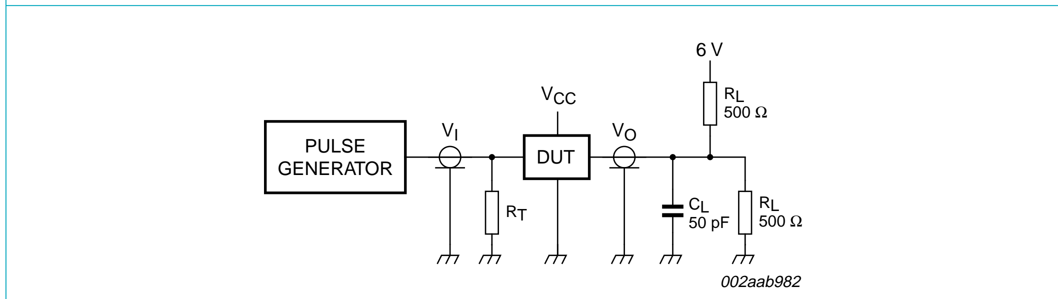

Fig 15. Load circuit for 9AO OFF-state to LOW and LOW to OFF-state

R_L — Load resistor

C_L — Load capacitance; includes jig and probe capacitance

R_T — Termination resistance; should be equal to Z_o of pulse generators.

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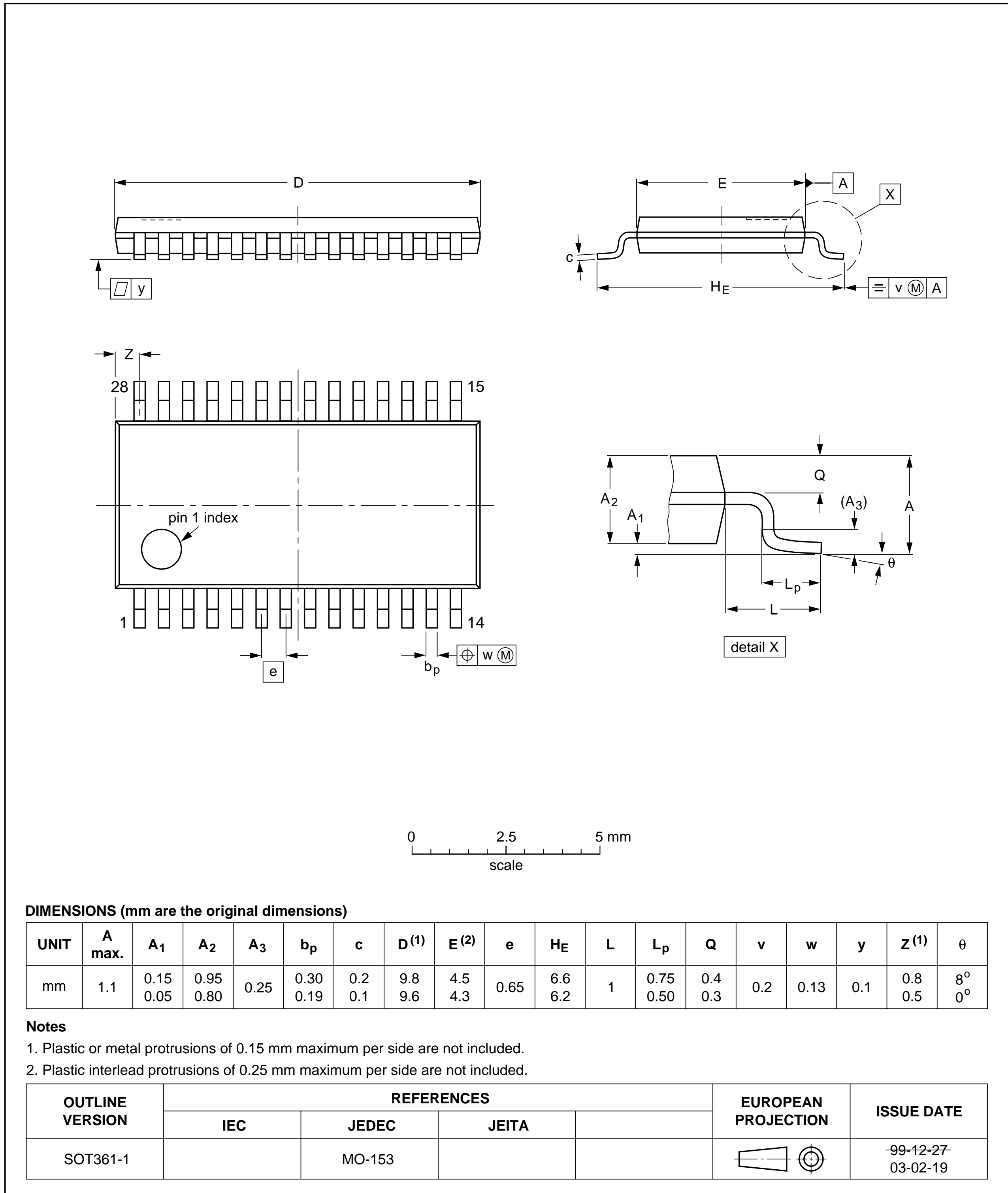
14. Package outline

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

Fig 16. Package outline SOT361-1 (TSSOP28)

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15. Soldering

15.1 Introduction to soldering surface mount packages

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

15.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow temperatures range from 215 °C to 260 °C depending on solder paste material. The peak top-surface temperature of the packages should be kept below:

Table 14. SnPb eutectic process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 ≥ 350
< 2.5 mm	240 °C + 0/–5 °C	225 °C + 0/–5 °C
≥ 2.5 mm	225 °C + 0/–5 °C	225 °C + 0/–5 °C

Table 15. Pb-free process - package peak reflow temperatures (from *J-STD-020C* July 2004)

Package thickness	Volume mm^3 < 350	Volume mm^3 350 to 2000	Volume mm^3 > 2000
< 1.6 mm	260 °C + 0 °C	260 °C + 0 °C	260 °C + 0 °C
1.6 mm to 2.5 mm	260 °C + 0 °C	250 °C + 0 °C	245 °C + 0 °C
≥ 2.5 mm	250 °C + 0 °C	245 °C + 0 °C	245 °C + 0 °C

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

15.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):

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  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

15.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

15.5 Package related soldering information

Table 16. Suitability of surface mount IC packages for wave and reflow soldering methods

Package[1]	Soldering method	
	Wave	Reflow[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

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[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

16. Abbreviations

Table 17. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DUT	Device Under Test
ESD	ElectroStatic Discharge
GTL	Gunning Transceiver Logic
HBM	Human Body Model
LVTTL	Low Voltage Transistor-Transistor Logic
MM	Machine Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic
VRD	Voltage Regulator Down

17. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
GTL2008_GTL2107_2	20060926	Product data sheet	-	GTL2008_1
Modifications:	• Added type number GTL2017 • Section 1 “General description”: added new 7th paragraph • Section 4 “Ordering information”: added type number GTL2107PW to Table 2 “Ordering information” and following paragraph • Table 10 “Limiting values”: removed (old) Table note 1 (information is now in Section 18 “Legal information”) • added “DUT” to Table 17 “Abbreviations”			
GTL2008_1	20060502	Product data sheet	-	-

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18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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