

May 2002 Revised October 2006

# FSTU16862 20-Bit Bus Switch with –2V Undershoot Protection

#### **General Description**

The Fairchild Switch FSTU16862 provides 20-bits of highspeed CMOS TTL-compatible bus switching. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 20-bit bus switch. When  $\overline{\text{OE}}_X$  is LOW, the switch is ON and Port A is connected to Port B. When  $\overline{\text{OE}}_X$  is HIGH, a high impedance state exists between the A and B Ports. The A and B Ports are protected against undershoot to support an extended range to 2.0V below ground. Fairchild's integrated Undershoot Hardened Circuit (UHC®TM) senses undershoot at the I/O and responds by preventing voltage differentials from developing and turning the switch on.

#### **Features**

- Undershoot hardened to -2V (A and B Ports)
- $\blacksquare$  4 $\Omega$  switch connection between two ports
- Minimal propagation delay through the switch
- Low lo
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- See Application Note AN-5008 for details on FSTU Undershoot Protected Fairchild Switch Family

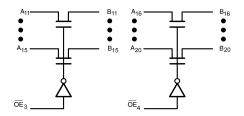
#### **Ordering Code:**

Order Number	Package Number	Package Description
FSTU16862QSP	MQA48A	48-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150" Wide
FSTU16862MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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# Logic Diagram



# **Pin Descriptions**

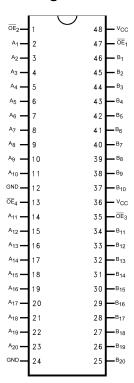
Pin Name	Description
<u></u> OE <sub>x</sub>	Bus Switch Enables
Α	Bus A
В	Bus B

# **Truth Table**

Inputs	Inputs/Outputs
<del>OE</del> <sub>x</sub>	A, B
L	A = B
Н	Z

- H = HIGH Voltage Level
  L = LOW Voltage Level
  Z = High Impedance

### **Connection Diagram**



#### **Absolute Maximum Ratings**(Note 1)

# Recommended Operating Conditions (Note 4)

 $\begin{array}{ll} \mbox{Power Supply Operating ($V_{CC}$)} & 4.0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Voltage ($V_{IN}$)} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Output Voltage ($V_{OUT}$)} & 0 \mbox{V to } 5.5 \mbox{V} \\ \end{array}$ 

Input Rise and Fall Time (t<sub>r</sub>, t<sub>f</sub>)

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2:  $\mathsf{V}_{\mathsf{S}}$  is the voltage observed/applied at either the A or B Ports across the switch.

**Note 3:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 4: Unused control inputs must be held HIGH or LOW. They may not float

### **DC Electrical Characteristics**

		V <sub>CC</sub>	TA	= -40 °C to +8	5 °C			
Symbol	Parameter	(V)	Min	Typ (Note 5)	Max	Units	Conditions	
V <sub>IK</sub>	Clamp Diode Voltage	4.5			-1.2	V	I <sub>IN</sub> = -18 mA	
V <sub>IH</sub>	HIGH Level Input Voltage	4.0-5.5	2.0			V		
V <sub>IL</sub>	LOW Level Input Voltage	4.0-5.5			0.8	V		
I	Input Leakage Current	5.5			±1.0	μА	$0 \leq V_{IN} \leq 5.5V$	
		0			10	μА	V <sub>IN</sub> = 5.5V	
loz	OFF-STATE Leakage Current	5.5			±1.0	μА	$0 \le A, B \le V_{CC}$	
R <sub>ON</sub>	Switch On Resistance	4.5		4	7	Ω	V <sub>IN</sub> = 0V, I <sub>IN</sub> = 64 mA	
	(Note 6)	4.5		4	7	Ω	$V_{IN} = 0V$ , $I_{IN} = 30 \text{ mA}$	
		4.5		8	14	Ω	$V_{IN}=2.4V$ , $I_{IN}=15\ mA$	
		4.0		11	20	Ω	$V_{IN} = 2.4V, I_{IN} = 15 \text{ mA}$	
I <sub>CC</sub>	Quiescent Supply Current	5.5			3	μА	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$	
ΔI <sub>CC</sub>	Increase in I <sub>CC</sub> per Input	5.5			2.5	mA	One Input at 3.4V	
	(Note 7)						Other Inputs at V <sub>CC</sub> or GND	
V <sub>IKU</sub>	Voltage Undershoot	5.5			-2.0	V	$\frac{0.0 \text{ mA} \ge I_{IN} \ge -50 \text{ mA}}{\overline{OE} = 5.5 \text{V}}$	

Note 5: Typical values are at  $V_{CC} = 5.0 V$  and  $T_A = +25 \, ^{\circ} C$ 

Note 6: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 7: Per TTL driven input, control pins only.

#### **AC Electrical Characteristics**

Symbol	Parameter	$T_A = -40$ °C to $+85$ °C, $C_L = 50$ pF, RU = RD = $500\Omega$				Units	Conditions	Figure
Oymboi		V <sub>CC</sub> = 4.5 - 5.5V		V <sub>CC</sub> = 4.0V		Onito	Conditions	Number
		Min	Max	Min	Max			
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus-to-Bus (Note 8)		0.25		0.25	ns	V <sub>I</sub> = OPEN	Figures 2, 3
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time	1.0	5.9		6.4	ns	$V_I = 7V$ for $t_{PZL}$ $V_I = OPEN$ for $t_{PZH}$	Figures 2, 3
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time	1.0	6.9		7.4	ns	$V_I = 7V$ for $t_{PLZ}$ $V_I = OPEN$ for $t_{PHZ}$	Figures 2, 3

Note 8: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On Resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

#### Capacitance (Note 9)

Symbol	ymbol Parameter		Max	Units	Conditions
C <sub>IN</sub>	Control Pin Input Capacitance	3		pF	$V_{CC} = 5.0V, V_{IN} = 0V$
C <sub>I/O</sub>	Input/Output Capacitance "OFF State"	6		pF	$V_{CC}$ , $\overline{OE} = 5.0V$ , $V_{IN} = 0V$

Note 9: T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

#### **Undershoot Characteristic** (Note 10)

Symbol	Parameter	Min	Тур	Max	Units	Conditions
V <sub>OUTU</sub>	Output Voltage During Undershoot	2.5	V <sub>OH</sub> - 0.3		V	Figure 1

Note 10: This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

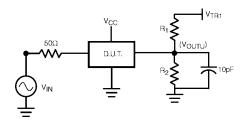
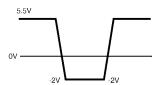


FIGURE 1.

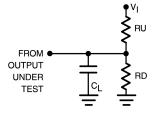
#### **Device Test Conditions**

Parameter	Value	Units
V <sub>IN</sub>	see Waveform	V
$R_1 = R_2$	100K	Ω
V <sub>TRI</sub>	11.0	V
V <sub>CC</sub>	5.5	V

# Transient Input Voltage (V<sub>IN</sub>) Waveform



# **AC Loading and Waveforms**



Note: Input driven by  $50\Omega$  source terminated in  $50\Omega$  Note:  $C_L$  includes load and stray capacitance Note: Input PRR = 1.0 MHz,  $t_W$  = 500 ns

FIGURE 2. AC Test Circuit

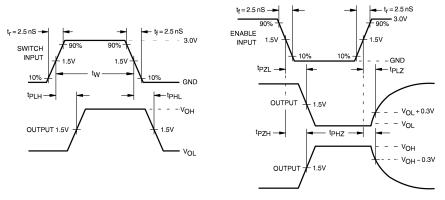
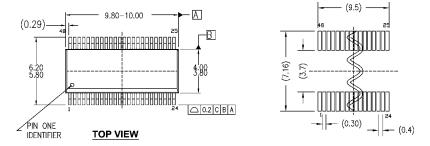
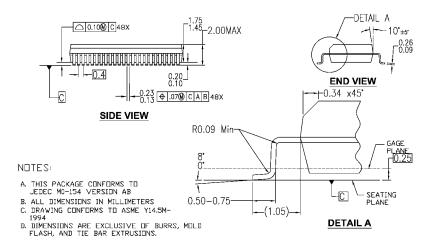


FIGURE 3. AC Waveforms

#### Physical Dimensions inches (millimeters) unless otherwise noted



# LAND PATTERN RECOMMENDATION



MQA48AREVA

48-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150" Wide Package Number MQA48A

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.40 TYP -B-8.10 4.05 O.2 C B A ALL LEAD TIPS PIN #1 IDENT. 0.50 LAND PATTERN RECOMMENDATION 0.1 C SEE DETAIL A 0.90+0.15 0.09-0.20 0.10±0.05 0.50 ⊕ 0.13@ A BS CS 12.00' TOP & BOTTON DIMENSIONS ARE IN MILLIMETERS R0.16 GAGE PLANE 0.25 A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION ED, DATE 4/97. B. DIMENSIONS ARE IN MILLIMETERS. SEATING PLANE 0.60±0.10-C. DIMENSIGNS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND THE BAR EXTRUSIONS. D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

DETAIL A

#### **Technology Description**

MTD48REVC

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384(FST3384) bus switch product.

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