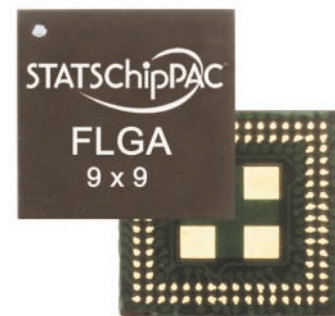


# FLGA

## Fine Pitch Land Grid Array

- Array molded, cost effective, space-saving packaging solution
- Available in 1.20mm (TFLGA), 1.00mm (VFLGA), and 0.80mm (WFLGA) maximum thickness
- Thinner than FBGA
- Exposed thermal/mechanical lands available
- Laminate substrate based enabling 2 and 4 layers of routing flexibility



### FEATURES

- Low profile
- Flexible body sizes range from 4 x 4mm to 13 x 13mm
- Flip chip and discrete passive options (SiP)
- Minimum 0.50mm pitch (array and peripheral land pads)
- Flexible land pattern arrangement
- Pb-free and halogen-free compatible materials available
- JEDEC standard compliant

### APPLICATIONS

- Handheld devices
- Wireless RF
- Analog
- ASIC
- Memory
- Simple PLDs

### DESCRIPTION

STATS ChipPAC's FLGA is a laminate substrate based package with plastic overmolded encapsulation. Unlike a standard FBGA, second level interconnect is achieved on the LGA by connecting "lands" on the package directly onto the PCB through solder re-flow. The elimination of solder balls brings better electrical performance and lower package profile without using the more expensive thinner BT core material. It also offers the flexibility of land pattern arrangement in the form of signal lands or heat spreader/ground pads to suit the thermal and electrical requirements of various devices. The FLGA package's reduced outline and thickness make it an ideal advanced technology packaging solution for high performance and/or portable applications. STATS ChipPAC's FLGA is available in a broad range of JEDEC standard body sizes including TFLGA (<1.20mm), VFLGA (<1.00mm) and WFLGA (<0.80mm) package thickness.

## Fine Pitch Land Grid Array

### SPECIFICATIONS

Die Thickness	75–300µm (3-12 mils)
Mold Cap Thickness	0.25-0.90mm
Marking	Laser
Packing Options	Tape & reel/JEDEC tray

### RELIABILITY

Moisture Sensitivity Level	JEDEC Level 2A, 260°C Reflow
Temperature Cycling	Condition C (–65°C to 150°C), 1000 cycles
High Temp Storage	150°C, 1000 hrs
Pressure Cooker Test	121°C/100%RH/2atm, 168 hrs
Temperature/Humidity Test	85°C/85% RH, 1000 hrs
Unbiased HAST	130°C/85% RH/2 atm, 96 hrs

### THERMAL PERFORMANCE, $\theta_{ja}$ (°C/W)

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and land configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size	PCB Vias	Thermal Performance $\theta_{ja}$ (°C/W)
VFLGA	9 x 9 (4L)	112	4.1 x 4.1	16	36.1

Note: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2.

### ELECTRICAL PERFORMANCE

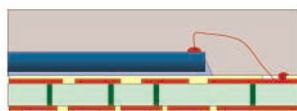
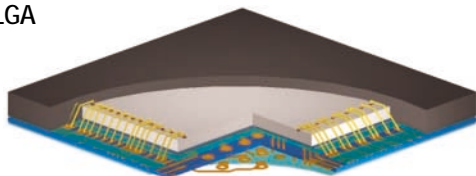
Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a frequency of 100MHz and assumes 1.0 mil gold bonding wire.

Conductor Component	Length (mm)	Resistance (mOhms)	Inductance (nH)	Inductance Mutual (nH)	Capacitance (pF)	Capacitance Mutual (pF)
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (2L)	2 - 7	25 - 110	1.10 - 4.35	0.25 - 2.27	0.20 - 0.90	0.05 - 0.41
Total (2L)	4 - 0	145 - 230	2.75 - 6.00	0.70 - 3.12	0.30 - 1.00	0.06 - 0.43
Wire	2	120	1.65	0.45 - 0.85	0.10	0.01 - 0.02
Net (4L)	2 - 7	25 - 110	0.70 - 2.95	0.17 - 1.57	0.30 - 1.05	0.05 - 0.41
Total (4L)	4 - 9	145 - 230	2.35 - 4.60	0.62 - 2.42	0.40 - 1.15	0.06 - 0.43

Note: Net = Total Trace Length + Via

### CROSS-SECTION

#### FLGA



### PACKAGE CONFIGURATIONS

Body Sizes (mm)	4x4 to 13x13
Terminal Count	8 to 200
Terminal Pitch (mm)	0.50 to 0.80
Typ. Pkg. Thickness	TFLGA: 1.20mm VFLGA: 1.00mm max. WFLGA: 0.80mm max.

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