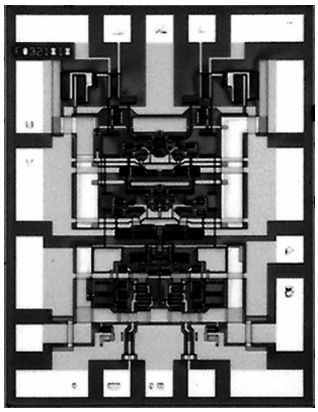
SUMITOMO ELECTRIC

02.04.24

F0321818B

2 GHz Bandwidth

Limiting Amplifier



♦ *Features*

- +5 or -5 V single power supply
- 20 dB typical gain
- 2.0 GHz typical -3 dB cutoff frequency
- On-chip matching to 50 Ω
- 55 mA typical operating current
- Differential input and output
- Differential ECL compatible input

♦ *Applications*

- Post-amplifier of an optical receiver circuit up to 2.5 Gb/s
- Logic gate buffer to interface between analog circuit and logic circuit

♦ *Functional Description*

The F0321818B is a stable GaAs integrated limiting amplifier for use in a post-amplifier of an optical receiver circuit up to 2.5 Gb/s. The F0321818B typically specifies a small signal gain of 20 dB (Rs=RL=50 Ω) with a 3 dB-cutoff-frequency of 2.0 GHz. It features single +5 or -5 V supply operation, excellent VSWR's of 1.1:1, and a typical dissipation current of 55 mA.

The F0321818B can be also used as interface circuits in sensing systems and measurement instruments. Emitter coupled logic (ECL) or source coupled FET logic (SCFL) circuits are the most popular IC's for high speed digital circuits; the F0321818B operating under a differential ECL compatible input condition is the best choice as the interface IC to join analog circuits to ECL circuits or conventional GaAs logic IC's.

♦ *Absolute Maximum Ratings*

T_a=25 °C, unless specified

Parameter	Symbol	Value	Units
Supply Voltage	V_{DD}	V_{SS}-0.5 to V_{SS}+7	V
Supply Current	I_{DD}	80	mA
Input Voltage Swing (AC)	V_{IN+} , V_{OUT-}	1	V
Output Voltage	V_{OUT+} , V_{OUT-}	V_{DD}-2.5 to V_{DD}	V
Ambient Operating Temperature	Ta	0 to +70	°C
Storage Temperature	Tstg	-55 to +125	°C

♦ *Recommended Operating Conditions*

V_{SS} = GND

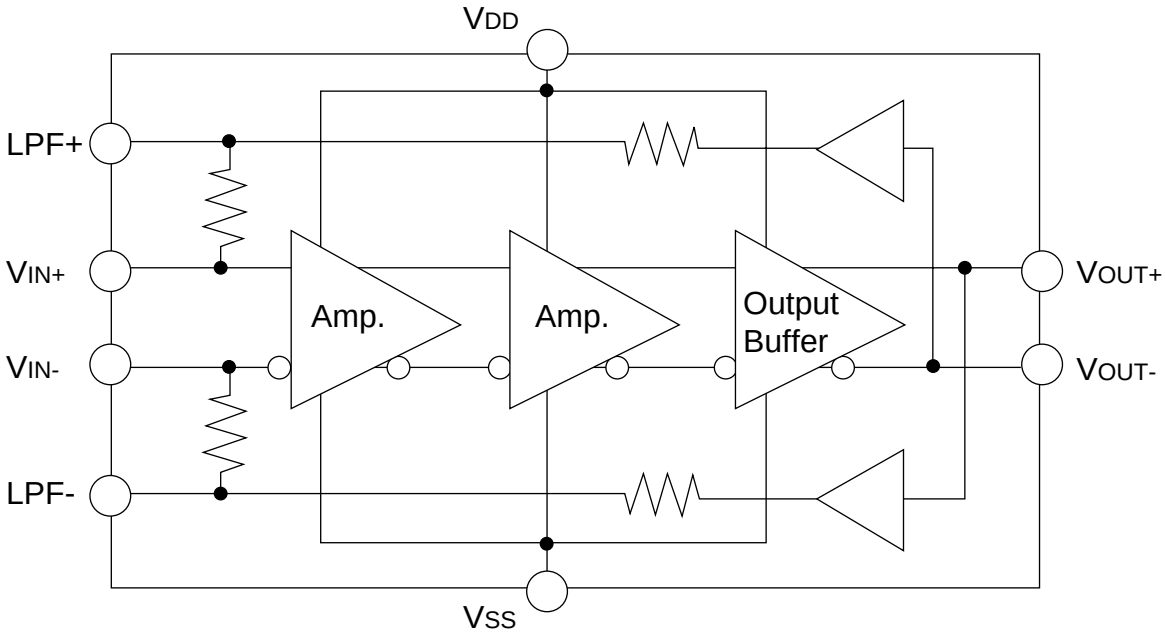
Parameter	Symbol	Value			Units
		Min.	Typ.	Max.	
Supply Voltage	V_{DD}	4.75	5	5.46	V
AC Coupled Load	RL	-	50	-	Ω
Ambient Operating Temperature	T_a	0	25	70	° C

♦ *Electrical Characteristics*

T_a = 25 °C, V_{DD} = +5 V, V_{SS} = GND, unless specified

Parameter	Symbol	Test Conditions	Value			Units
			Min.	Typ.	Max.	
Supply Current	I_{DD}	Pin=-40dBm	-	55	70	mA
Input Bias Point	V_{IN}		-	1.5	-	V
Output bias Point	V_{OUT}		-	3.5	-	V
VSWR (IN, OUT)	SWR	Pin=-40dBm f=1MHz	-	1.1	1.8	-
Gain	GV	Pin=-40dBm RL=50Ω f=1MHz	18	20	-	dB
-3dB High Frequency Cutoff	Fc	Pin=-40dBm RL=50Ω	-	2.0	-	GHz
Maximum Output Swing (single output)	Vom	RL=50Ω	0.4	0.6	0.8	V

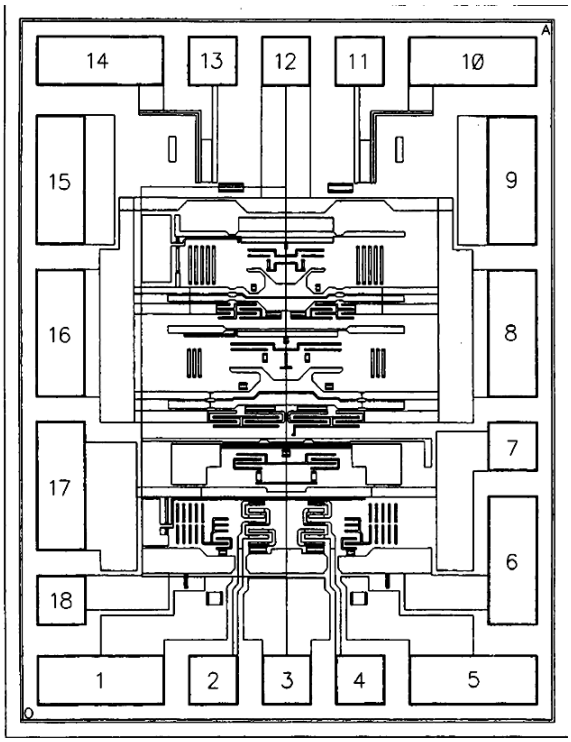
♦ *Block Diagram*



♦ *Dia Descriptions*

V_{IN+}	Input
LPF+	AC Ground
V_{IN-}	Input
LPF-	AC Ground
V_{OUT+}	Output
V_{OUT-}	Output
V_{SS1}	Supply Voltage
V_{SS2}	Supply Voltage
V_{DD}	Supply Voltage
V_{DD}	Supply Voltage

♦ *Dia Pad Assignments*

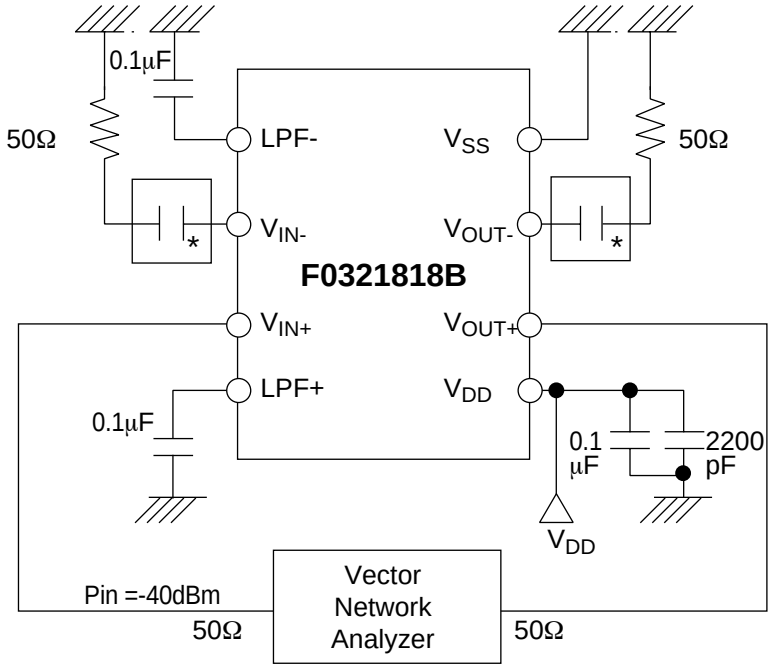


No.	Symbol	Center Coordinates(μm)	No.	Symbol	Center Coordinates(μm)
(1)	V_{DD2}	(160,80)	(11)	V_{IN-}	(690,1330)
(2)	V_{OUT+}	(390,80)	(12)	V_{DD1}	(540,1330)
(3)	V_{DD2}	(540,80)	(13)	V_{IN+}	(390,1330)
(4)	V_{OUT-}	(690,80)	(14)	LPF+	(160,1330)
(5)	V_{DD2}	(920,80)	(15)	V_{SS1}	(80,1090)
(6)	V_{SS2}	(1000,320)	(16)	V_{DD1}	(80,780)
(7)	V_{DD2}	(1000,550)	(17)	V_{DD2}	(80,470)
(8)	V_{DD1}	(1000,780)	(18)	V_{SS2}	(80,240)
(9)	V_{SS1}	(1000,1090)	O		(0,0)
(10)	LPF-	(920,1330)	A		(1080,1410)

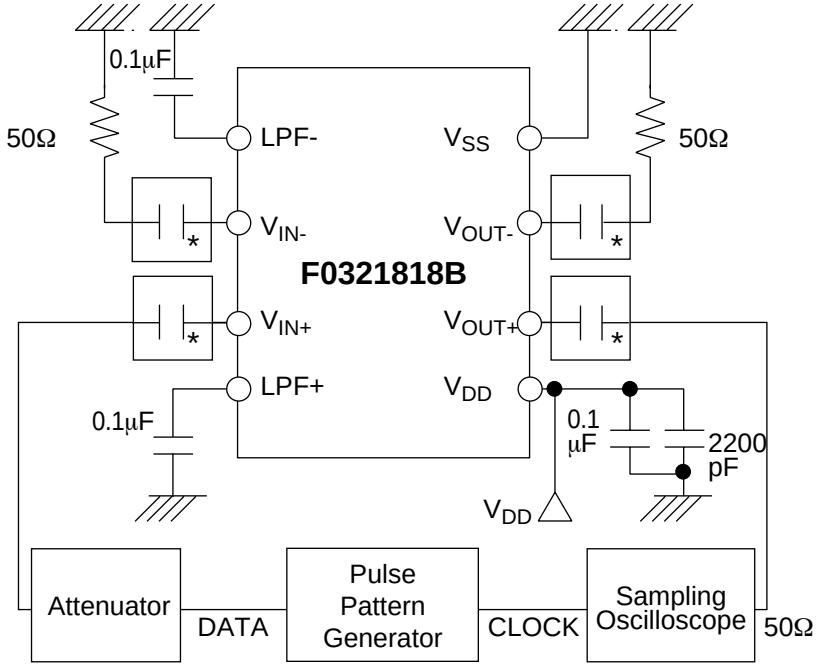
* V_{DD1} is not connected to V_{DD2} in the bare chip IC.
* V_{SS1} is not connected to V_{SS2} in the bare chip IC.
* For +5 V users, we recommended the Pads of No.16,17 are connected to power supply pads (+5 V) and the pads of No. 6, 9,15,18 are connected to GND pads.
* We recommend that unused input pin should be terminated to GND via coupling capacitor and 50 ohm load.
  Example : (unused input pin) → (coupling capacitor) → (50 ohm load) → (GND)
* On the back of the bare die, we mount it on GND but no problem for mounted on V_{SS}.

♦ *Test Circuits*

1) AC Characteristics



2) Limiting Characteristics

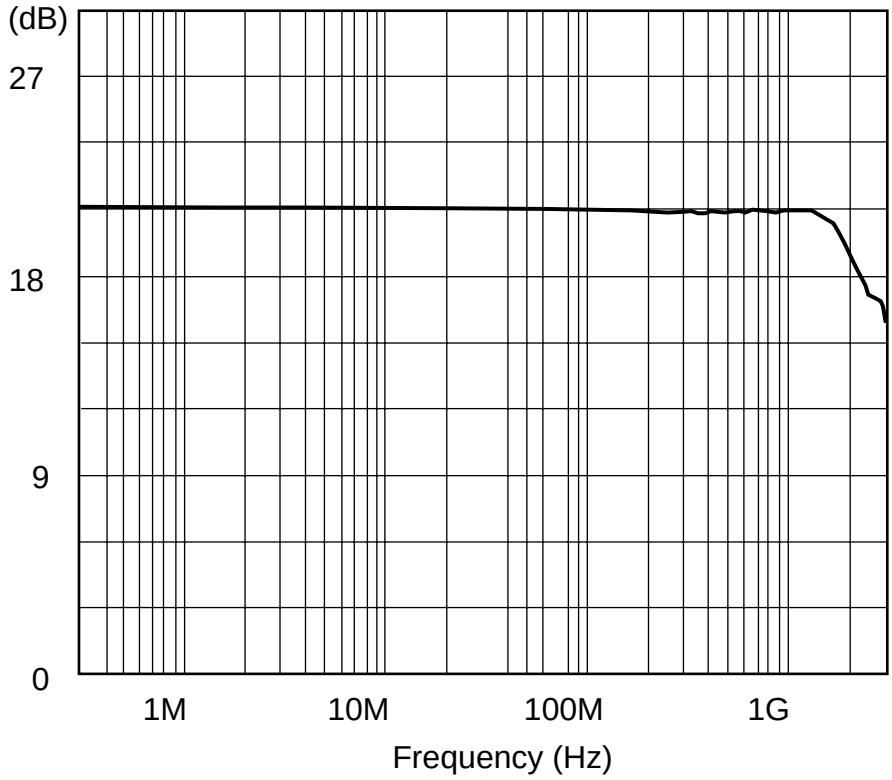


* DC BLOCK (PICOSECIND PULSE LABS, MODEL 5501)

♦ *Typical AC Characteristics*

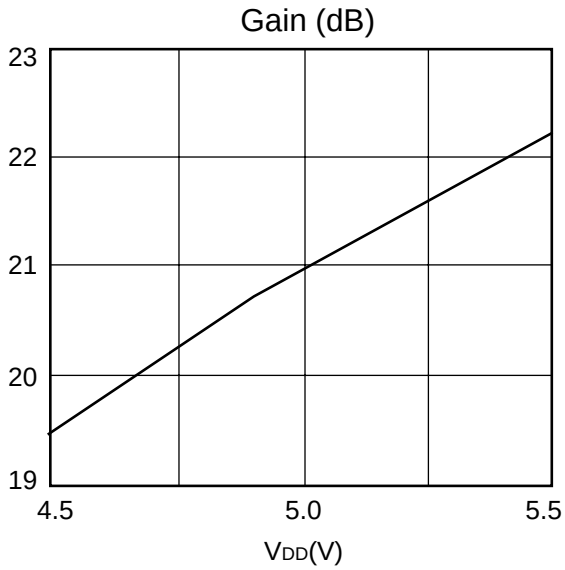
(1) Gain

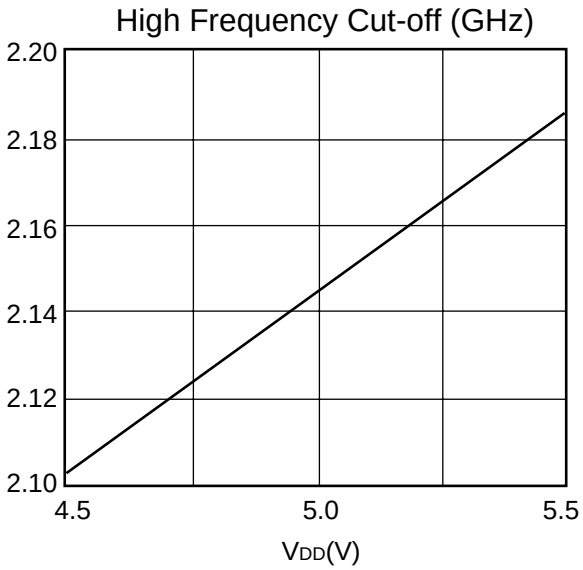
T_a =25 °C, V_{DD} =+5 V, V_{SS} =GND, Pin =-40 dBm, RL =50 Ω, 300 kHz-3 GHz



(2) Dependence of Gain and High Frequency Cutoff on Power Supply Variations

T_a =25 °C, V_{DD} =-5 V, V_{SS} =GND, Pin =-40 dBm, RL =50 Ω, 300 kHz-3 GHz

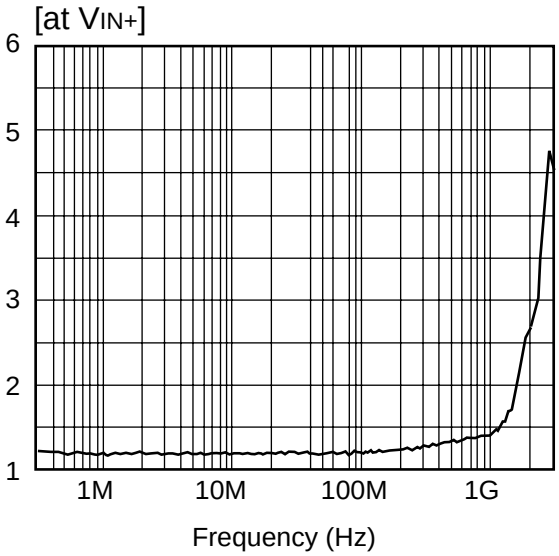




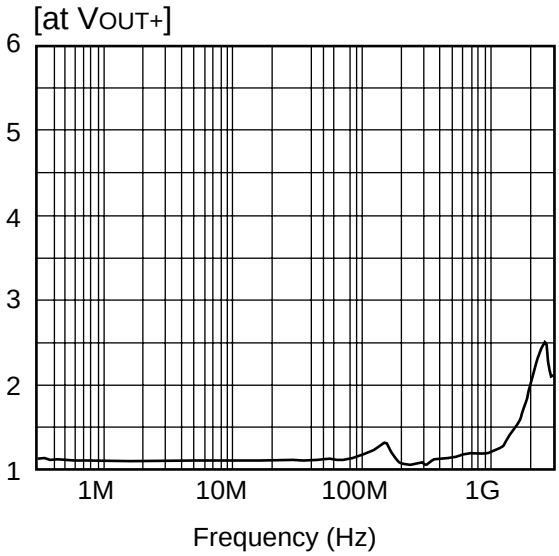
♦ *Typical AC Characteristics*

(3) VSWR's

T_a =25 °C, V_{DD} =+5 V, V_{SS} =GND, Pin =-40 dBm, RL =50 Ω, 300 kHz - 3 GHz



*Almost same characteristics is exhibited at V_{IN-}

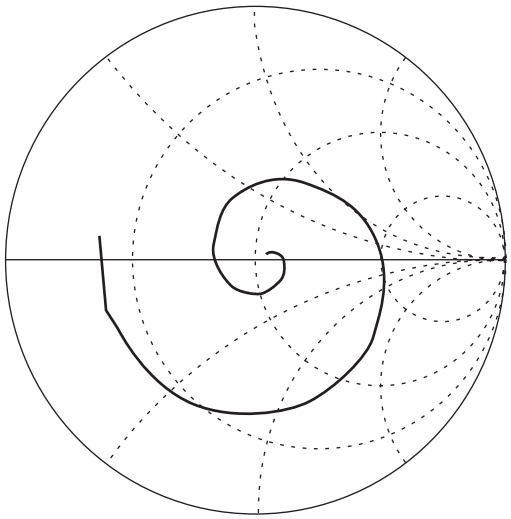


*Almost same characteristics is exhibited at V_{OUT-}

(4) S parameters on Smith Chart

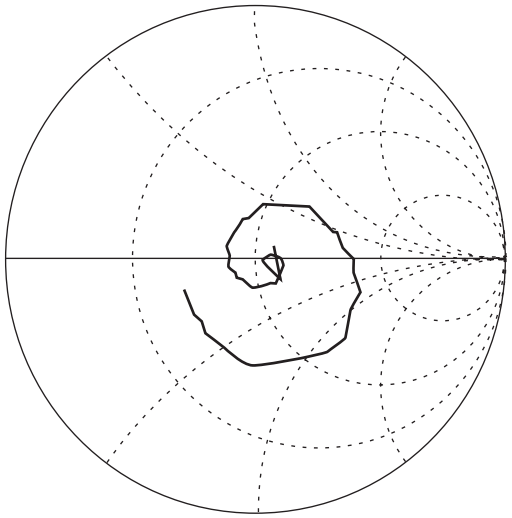
T_a =25 °C, V_{DD} =+5 V, V_{SS} =GND, Pin =-40 dBm, RL =50 Ω

S_{11} at V_{IN+}



START 100 MHz STOP 3 GHz

S_{22} at V_{OUT+}



START 100 MHz STOP 3 GHz

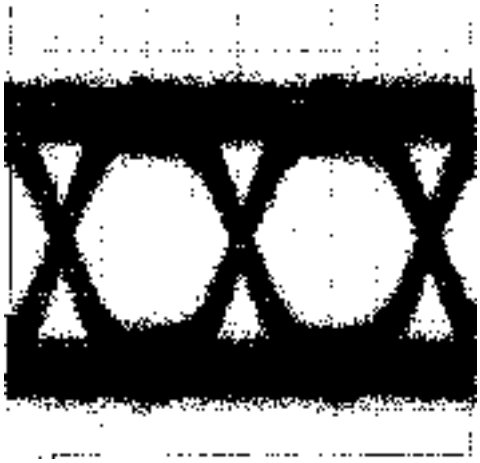
♦ *Typical Limiting Characteristics*

(1) Eye diagrams for 2.5 Gb/s NRZ Pseudo-random Data Response

2^{23}-1, T_a = 25 °C, V_{DD} =5 V, V_{SS} =GND, RL =50 Ω

(a) V_{IN+} = 5 mVp-p

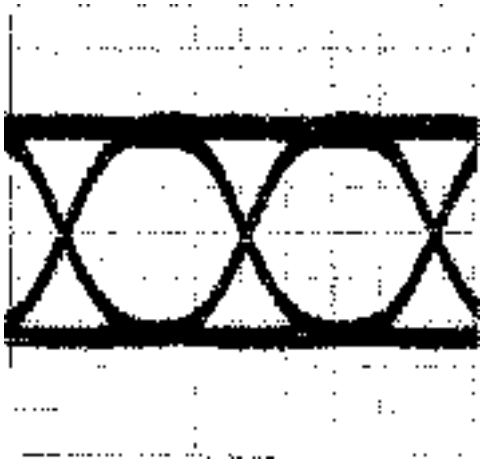
10 mV/div



100 psec/div

(b) V_{IN+} = 50 mVp-p

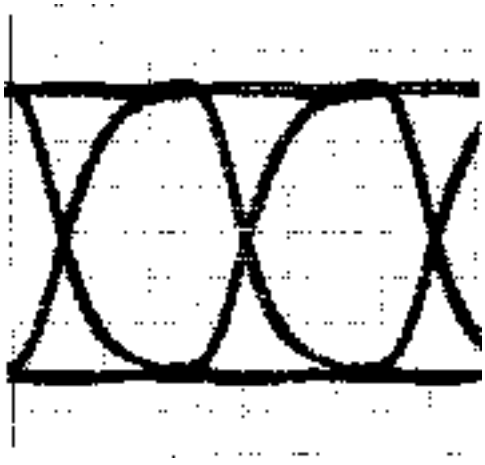
100 mV/div



100 psec/div

(c) V_{IN+} = 500 mVp-p

100 mV/div



100 psec/div

♦ *General Description*

A post-amplifier is positioned between a preamplifier (an amplifier for a faint photocurrent from PIN photo diode) and a decision circuit (a circuit to discriminate the logic level of the received signal), enlarging the output signal from the preamplifier to a higher level to discriminate the logic level. The input signal amplitude of the post-amplifier, meaning the output signal of the preamplifier, varies widely, because the optical signal power received by the PIN photo diode depends on the length of the transmission line. Therefore, the post-amplifier should function to output an almost constant signal level under widely varying input voltage. This is called a limiting function, and the F0321818B provides excellent limiting characteristics. As shown in the data sheet, the increase of only 200 mV (400 mV→600 mV) in the output voltage can be observed even if the 2.5 Gps input signal varies widely from 50 mV to 500 mV

Wide use analog IC's having satisfactory limiting functions as described above can not be found except for the F0321818B. Customized IC's for each application or a circuit designed by discrete transistors are believed to have been developed.

♦ *Post Matching*

Input/output VSWR's of the F0321818B are well-designed for 50 Ω, typically showing excellent VSWR's of 1.1:1. Therefore, the F0321818B can be applied for 50 Ω systems with no external parts. Furthermore, the fine VSWR characteristics provide stable operation even for cascade connections of two IC's for a higher gain. The excellent VSWR characteristics of the F0321818B gives full play in a clock recovery system using SAW filters, because the impedance mismatch has a significant effect on the quality of the recovered clock signal.

♦ *Gain Consideration*

The F0321818B has a small signal gain of 20 dB. A too high gain can be harmful because of parasitic oscillation. If a slightly higher gain is needed, a 6 dB higher gain of 26 dB can be obtained by a high impedance termination instead of a 50 Ω load. A double gain can be achieved by simple cascade connection if a still higher gain is required.

♦ *Noise Performance*

The F0321818B based on the GaAs FET fabrication process intrinsically has more excellent low-noise characteristics compared with IC's based on the silicon bipolar process. Many transmission systems often demand superior signal-to-noise ratio; the F0321818B is the best choice for such applications.

The differential circuit configuration in the input and output enable a complete differential operation to reduce common mode noise: simple single ended input and output operation is also available.

♦ *LPF+ & LPF-*

The F0321818B has two terminals, LPF+ and LPF-, for AC ground. These terminals are connected to ground by a capacitor. The time constant of the feedback loop in the F0321818B depends on the capacitor, giving the lower frequency cutoff of the circuit by the large capacitor. A 0.1 micro farad is employed for conventional applications.

♦ *Die-Chip Description*

The F0321818B is shipped like the die-chip described above. The die thickness is typically 450 μm ± 20 μm with the available pad size uncovered by a passivation film of 95 μm square. The material of the pads is TiW/Pt/Au and the backside is metalized by Ti/Au.

♦ *Assembling Condition*

SEI recommends the assembling process as shown below and affirms sufficient wire-pull and die-shear strength. The heating time of one minutes at the temperature of 310 °C gave satisfactory results for die-bonding with AuSn performs. The heating and ultrasonic wire-bonding at the temperature of 150 °C by a ball-bonding machine is effective.

♦ *Quality Assurance*

For the Die-chip products, there is only one technically inevitable drawback in terms of quality assurance which is to be impossible of the burn-in test for screening owing to die-shipment. SEI will not ship them if customers do not agree on this point. On the other hand, the lot assurance test is performed completely without any problems according to SEI's authorized rules. A microscope inspection is conducted in conformance with the MIL-STD-883C Method 2010.7.

♦ *Precautions*

Owing to their small dimensions, the GaAs FET's from which the F0321818B is designed are easily damaged or destroyed if subjected to large transient voltages. Such transients can be generated by power supplies when switched on if not properly decoupled. It is also possible to induce spikes from static-electricity-charged operations or ungrounded equipment.