ELPIDA

PRELIMINARY DATA SHEET

512M bits Mobile RAM MCP
2 pcs of 256Mb components

EDL5132CBMA (16M words × 32 bits)

Description

The EDL5132CBMA is a 512M bits Mobile RAM MCP (Multi Chip Package) organized as 4,194,304 words × 32 bits × 4 banks, 2 pieces of 256M bits Mobile RAM in one package. It is packaged in 90-ball FBGA.

Features

- Low voltage power supply
  - VDD: 1.7V to 1.95V
  - VDDQ: 1.7V to 1.95V
- Wide temperature range (–25°C to 85°C)
- Programmable Partial Array Self Refresh
- Programmable Driver Strength
- Auto Temperature Compensated Self Refresh by built-in temperature sensor.
- Deep power down mode
- Fully Synchronous Dynamic RAM, with all signals referenced to a positive clock edge
- Pulsed interface
- Possible to assert random column address in every cycle
- Quad internal banks controlled by BA0 and BA1
- Byte control by DQM
- Wrap sequence = Sequential/ Interleave
- /CAS latency (CL) = 2, 3
- Automatic precharge and controlled precharge
- Auto refresh and self refresh
- ×32 organization
- 8,192 refresh cycles/64ms
- Burst termination by Burst stop command and Precharge command
- FBGA package with lead free solder (Sn-Ag-Cu)

Pin Configurations

/xxx indicates active low signal.

90-ball FBGA

	1	2	3	4	5	6	7	8	9
A	DQ26	DQ24	VSS				VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ				VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25				DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30				DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC				NC	DQ16	VSSQ
F	VSS	DQM3	A3				A2	DQM2	VDD
G	A4	A5	A6				A10	A0	A1
H	A7	A8	A12				NC	BA1	A11
J	CLK	CKE	A9				BA0	/CS	/RAS
K	DQM1	NC	NC				/CAS	/WE	DQM0
L	VDDQ	DQ8	VSS				VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9				DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14				DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ				VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS				VDD	DQ0	DQ2

(Top view)

A0 to A12	Address inputs
BA0, BA1	Bank select address
DQ0 to DQ31	Data-input/output
/CS	Chip select
/RAS	Row address strobe
/CAS	Column address strobe
/WE	Write enable
DQM0 to DQM3	DQ mask enable
CKE	Clock enable
CLK	Clock input
VDD	Power supply
VSS	Ground
VDDQ	Power supply for DQ
VSSQ	Ground for DQ
NC	No connection

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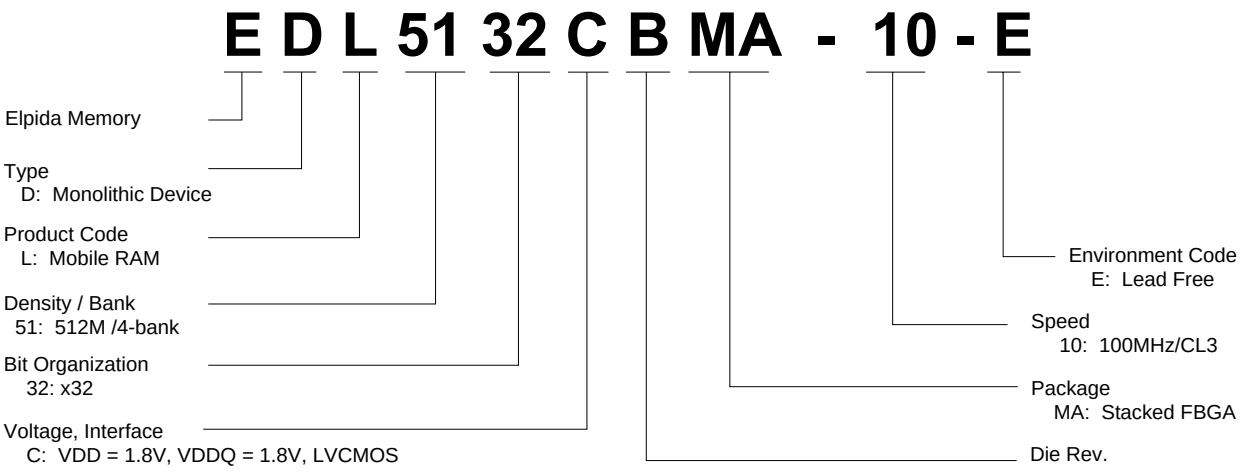
Ordering Information

Part number	Organization (words × bits)	Internal banks	Clock frequency MHz (max.)	/CAS latency	Package
EDL5132CBMA-10-E	16M × 32	4	100	3	90-ball FBGA

Part Number



CONTENTS

Electrical Specifications

- All voltages are referenced to VSS (GND).
- After power up, wait more than 200 μs and then, execute Power on sequence and two Auto Refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to +2.6	V	
Supply voltage relative to VSS	VDD, VDDQ	–0.5 to +2.6	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	1.0	W	
Operating ambient temperature	TA	–25 to +85	°C	
Storage temperature	Tstg	–55 to +125	°C	

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (TA = –25 to +85°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD	1.7	1.8	1.95	V	
	VSS, VSSQ	0	0	0	V	
DQ Supply voltage	VDDQ	1.7	1.8	1.95	V	
Input high voltage	VIH	0.8 × VDDQ	—	VDDQ + 0.3	V	1
Input low voltage	VIL	–0.3	—	0.3	V	2

Notes: 1. VIH (max.) = 2.6V (pulse width ≤ 5ns)

2. VIL (min.) = –1.0V (pulse width ≤ 5ns)

DC Characteristics 1 (TA = –25 to +85°C, VDD = VDDQ = 1.7V to 1.95V, VSS, VSSQ = 0V)

Parameter /CAS latency	Symbol	Grade	max.	Unit	Test condition	Notes
Operating current (CL = 2)	IDD1		80	mA	Burst length = 1 tRC ≥ tRC min., IO = 0mA, One bank active	1
(CL = 3)	IDD1		80	mA		
Standby current in power down	IDD2P		1.2	mA	CKE ≤ VIL max., tCK = 15ns	
Standby current in power down (input signal stable)	IDD2PS		1	mA	CKE ≤ VIL max., tCK = ∞	
Standby current in non power down	IDD2N		6	mA	CKE ≥ VIH min., tCK = 15ns, /CS ≥ VIH min., Input signals are changed one time during 30ns.	
Standby current in non power down (input signal stable)	IDD2NS		4	mA	CKE ≥ VIH min., tCK = ∞, Input signals are stable.	
Active standby current in power down	IDD3P		2	mA	CKE ≤ VIL max., tCK = 15ns	
Active standby current in power down (input signal stable)	IDD3PS		1.6	mA	CKE ≤ VIL max., tCK = ∞	
Active standby current in non power down	IDD3N		30	mA	CKE ≥ VIH min., tCK = 15 ns, /CS ≥ VIH min., Input signals are changed one time during 30ns.	
Active standby current in non power down (input signal stable)	IDD3NS		10	mA	CKE ≥ VIH min., tCK = ∞, Input signals are stable.	
Burst operating current (CL = 2)	IDD4		90	mA	tCK ≥ tCK min., IOUT = 0mA, All banks active	2
(CL = 3)	IDD4		120	mA		
Refresh current (CL = 2)	IDD5		110	mA	tRC ≥ tRC min.	3
(CL = 3)	IDD5		110	mA		
Standby current in deep power down mode	IDD7		20	µA	CKE ≤ 0.2V	

Self refresh current	Symbol	Grade	typ.	max.	Unit	Condition	Notes
PASR="000" (Full)	IDD6		—	800	µA	TA ≤ 85°C +0°C/–15°C, CKE ≤ 0.2V	4
PASR="001" (2BK)			—	600	µA		
PASR="010" (1BK)			—	500	µA		
PASR="000" (Full)	IDD6		400	—	µA	TA ≤ 45°C, CKE ≤ 0.2V	4
PASR="001" (2BK)			360	—	µA		
PASR="010" (1BK)			300	—	µA		

Notes: 1. IDD1 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD1 is measured on condition that addresses are changed only one time during tCK (min.).

2. IDD4 depends on output loading and cycle rates. Specified values are obtained with the output open. In addition to this, IDD4 is measured on condition that addresses are changed only one time during tCK (min.).

3. IDD5 is measured on condition that addresses are changed only one time during tCK (min.).

4. IDD6 is specified when self refresh state is maintained long enough under the specified TA condition, after a busy sequence of read and write operations.

DC Characteristics 2 (TA = –25 to +85°C, VDD = VDDQ = 1.7V to 1.95V, VSS, VSSQ = 0V)

Parameter	Symbol	min.	max.	Unit	Test condition	Note
Input leakage current	ILI	–2.0	2.0	µA	0 ≤ VIN ≤ VDDQ	
Output leakage current	ILO	–1.5	1.5	µA	0 ≤ VOUT ≤ VDDQ, DQ = disable	
Output high voltage	VOH	VDDQ – 0.2	—	V	IOH = –0.1 mA	
Output low voltage	VOL	—	0.2	V	IOL = 0.1 mA	

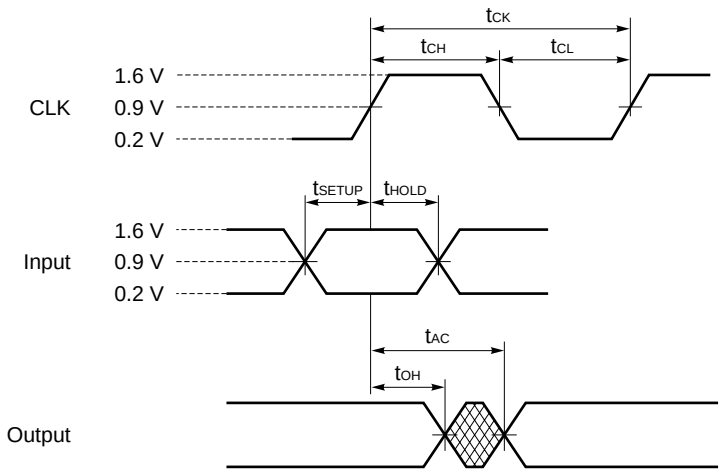
Pin Capacitance (TA = 25°C, f = 1MHz)

Parameter	Symbol	Pins	min.	typ.	max.	Unit	Note
Input capacitance	CI1	CLK	4.0	—	7.0	pF	
	CI2	Address, CKE, /CS, /RAS, /CAS, /WE	4.0	—	7.6	pF	
	CI3	DQM	2.0	—	3.8	pF	
Data input/output capacitance	CI/O	DQ	6.0	—	7.5	pF	

AC Characteristics (TA = –25 to +85°C, VDD = VDDQ = 1.7V to 1.95V, VSS, VSSQ = 0V)

Test Conditions

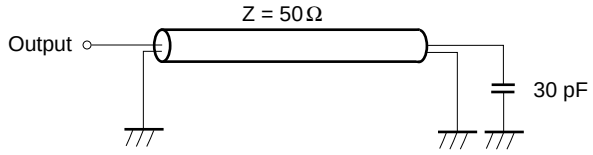
- AC high level input voltage / low level input voltage: 1.6 / 0.2V
- Input timing measurement reference level: 0.9V
- Transition time (Input rise and fall time): 1ns
- Output timing measurement reference level: 0.9V



Synchronous Characteristics

Parameter	Symbol	min.	max.	Unit	Note
Clock cycle time (CL= 2)	tCK2	15	—	ns	
(CL= 3)	tCK3	10	—	ns	
Access time from CLK (CL= 2)	tAC2	—	9	ns	1
(CL= 3)	tAC3	—	7	ns	1
CLK high level width	tCH	3	—	ns	
CLK low level width	tCL	3	—	ns	
Data-out hold time	tOH	3	—	ns	1
Data-out low-impedance time	tLZ	0	—	ns	
Data-out high-impedance time (CL= 2)	tHZ2	3	9	ns	
(CL= 3)	tHZ3	3	7	ns	
Data-in setup time	tDS	2	—	ns	
Data-in hold time	tDH	1	—	ns	
Address setup time	tAS	2	—	ns	
Address hold time	tAH	1	—	ns	
CKE setup time	tCKS	2	—	ns	
CKE hold time	tCKH	1	—	ns	
CKE setup time (Power down exit)	tCKSP	2	—	ns	
Command (/CS, /RAS, /CAS, /WE, DQM) setup time	tCMS	2	—	ns	
Command (/CS, /RAS, /CAS, /WE, DQM) hold time	tCMH	1	—	ns	

Note: 1. Output load.

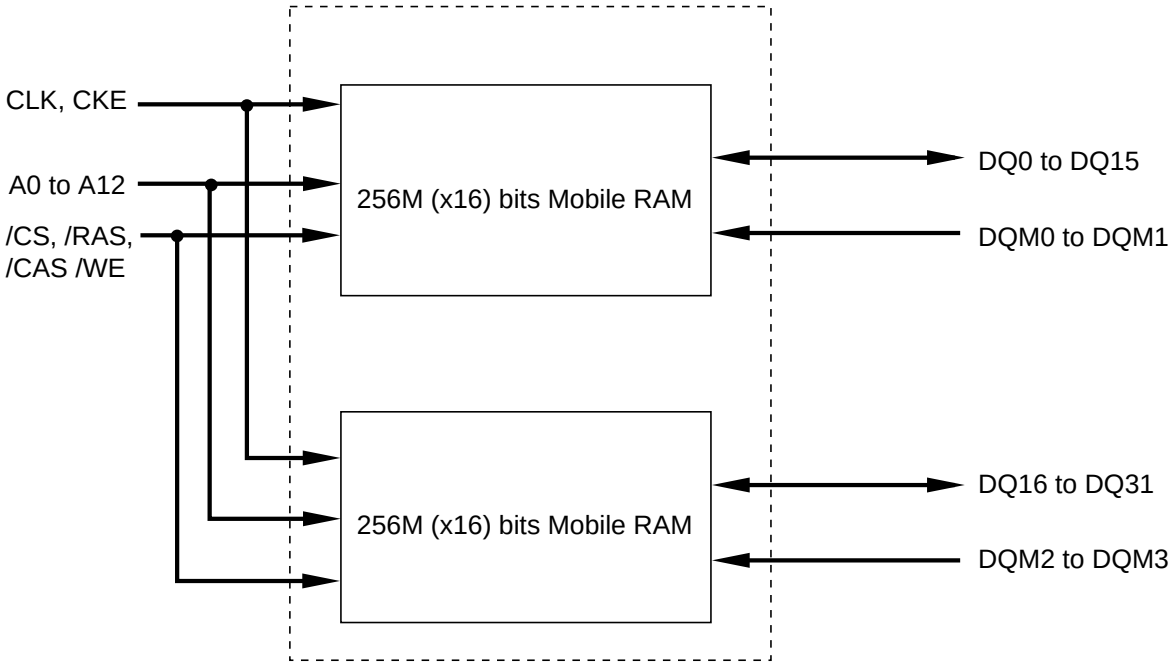


Output load

Asynchronous Characteristics

Parameter	Symbol	min.	max.	Unit	Note
ACT to REF/ACT command period (operation)	tRC	90	—	ns	
ACT to REF/ACT command period (refresh)	tRC1	110	—	ns	
Self refresh exit to REF/ACT command period	tRC2	120	—	ns	
ACT to PRE command period	tRAS	60	120000	ns	
PRE to ACT command period	tRP	30	—	ns	
Delay time ACT to READ/WRITE command	tRCD	30	—	ns	
ACT (one) to ACT (another) command period	tRRD	2	—	CLK	
Data-in to PRE command period	tDPL	2	—	CLK	
Data-in to ACT (REF) command period (Auto precharge) (CL = 2)	tDAL2	2CLK + 30	—	ns	
(CL = 3)	tDAL3	2CLK + 30	—	ns	
Mode register set cycle time	tRSC	2	—	CLK	
Transition time	tT	1	30	ns	
Refresh time (8,192 refresh cycles)	tREF	—	64	ms	

Block Diagram



Pin Function

CLK (input pin)

CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.

CKE (input pins)

CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and the Mobile RAM suspends operation.

When the Mobile RAM is not in burst mode and CKE is negated, the device enters power down mode. During power down mode, CKE must remain low.

/CS (input pins)

/CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.

/RAS, /CAS, and /WE (input pins)

/RAS, /CAS and /WE have the same symbols on conventional DRAM but different functions. For details, refer to the command table.

A0 to A12 (input pins)

Row Address is determined by A0 to A12 at the CLK (clock) rising edge in the active command cycle. It does not depend on the bit organization.

Column Address (See "Address Pins Table") is determined by A0 to A8 at the CLK rising edge in the read or write command cycle.

[Address Pins Table]

	Address (A0 to A12)	
Part Number	Row addresss	Column address
EDL5132CB	AX0 to AX12	AY0 to AY8

A10 defines the precharge mode. When A10 is high in the precharge command cycle, all banks are precharged; when A10 is low, only the bank selected by BA0 and BA1 is precharged.

When A10 is high in read or write command cycle, the precharge starts automatically after the burst access.

BA0 and BA1 (input pin)

BA0 and BA1 are bank select signal. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1
Bank A	L	L
Bank B	H	L
Bank C	L	H
Bank D	H	H

Remark: H: VIH. L: VIL.

DQM0 to DQM3 (input pins)

DQM controls I/O buffers. In read mode, DQM controls the output buffers like a conventional /OE pin. DQM high and DQM low turn the output buffers off and on, respectively. The DQM latency for the read is two clocks. In write mode, DQM controls the word mask. Input data is written to the memory cell if DQM is low but not if DQM is high. The DQM latency for the write is zero.

Each DQM pin corresponds to eight DQ pins, respectively (See DQM Correspondence Table).

[DQM Correspondence Table]

DQ mask enabe	DQs
DQM0	DQ0 to DQ7
DQM1	DQ8 to DQ15
DQM2	DQ16 to DQ23
DQM3	DQ24 to DQ31

DQ0 to DQ31 (input/output pins)

DQ pins have the same function as I/O pins on a conventional DRAM.

VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers.

Command Operation

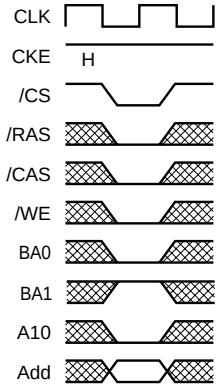
Extended Mode register set command (/CS, /RAS, /CAS, /WE, BA0 = Low, BA1 = High)

The Mobile RAM has an extended mode register that defines low power functions. In this command, A0 through A12 are the data input pins.

After power on, the extended mode register set command must be executed to fix low power functions.

The extended mode register can be set only when all banks are in idle state.

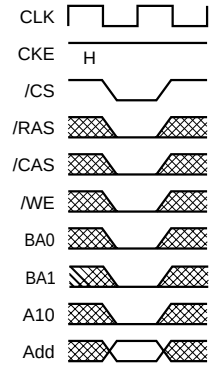
During tRSC following this command, the Mobile RAM can not accept any other commands.



Extended Mode register set command

Mode register set command (/CS, /RAS, /CAS, /WE, BA0, BA1 = Low)

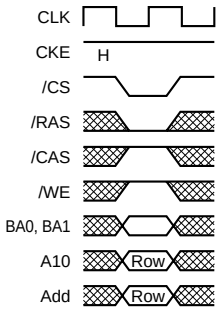
The Mobile RAM has a mode register that defines how the device operates. In this command, A0 through A12 are the data input pins. After power on, the mode register set command must be executed to initialize the device. The mode register can be set only when all banks are in idle state. During tRSC following this command, the Mobile RAM cannot accept any other commands.



Mode register set command

Activate command (/CS, /RAS = Low, /CAS, /WE = High)

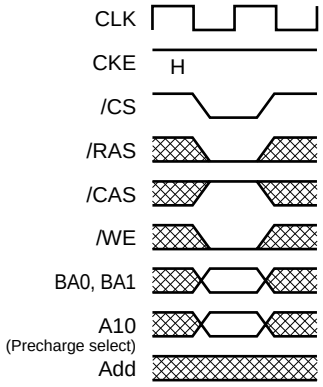
The Mobile RAM has four banks, each with 8,192 rows. This command activates the bank selected by BA0 and BA1 and a row address selected by A0 through A12. This command corresponds to a conventional DRAM's /RAS falling.



Activate command

Precharge command (/CS, /RAS, /WE = Low, /CAS = High)

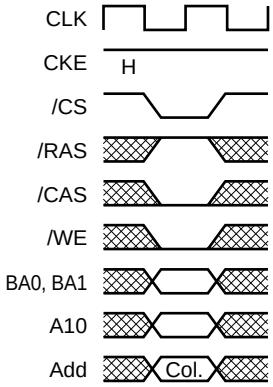
This command begins precharge operation of the bank selected by BA0 and BA1. When A10 is High, all banks are precharged, regardless of BA0 and BA1. When A10 is Low, only the bank selected by BA0 and BA1 is precharged. After this command, the Mobile RAM can't accept the activate command to the precharging bank during tRP (precharge to activate command period). This command corresponds to a conventional DRAM's /RAS rising.



Precharge command

Write command (/CS, /CAS, /WE = Low, /RAS = High)

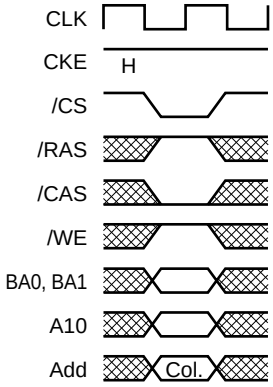
This command sets the burst start address given by the column address to begin the burst write operation. The first write data in burst mode can input with this command with subsequent data on following clocks.



Write command

Read command (/CS, /CAS = Low, /RAS, /WE = High)

Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column address.

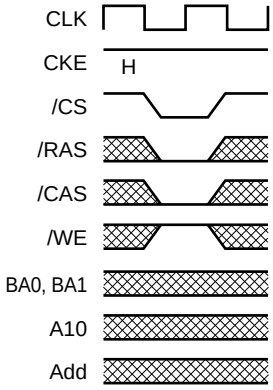


Read command

Auto refresh command (/CS, /RAS, /CAS = Low, /WE, CKE = High)

This command is a request to begin the Auto refresh operation. The refresh address is generated internally.

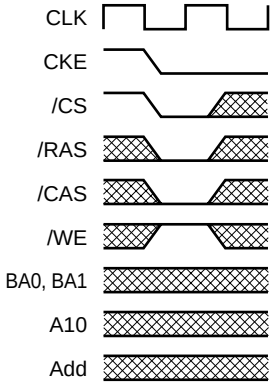
Before executing Auto refresh, all banks must be precharged. After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command. During tRC1 period (from refresh command to refresh or activate command), the Mobile RAM cannot accept any other command



Auto refresh command

Self refresh entry command (/CS, /RAS, /CAS, CKE = Low, /WE = High)

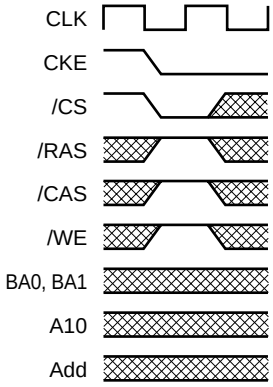
After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the Mobile RAM exits the self refresh mode. During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control. Before executing self refresh, all banks must be precharged.



Self refresh entry command

Power down entry command (/CS, CKE = Low, /RAS, /CAS, /WE = High)

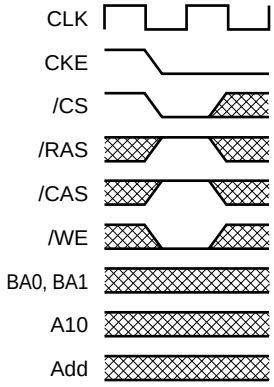
After the command execution, power down mode continues while CKE remains low. When CKE goes high, the Mobile RAM exits the power down mode. Before executing power down, all banks must be precharged.



Power down entry command

Deep power down entry command(/CS, CKE, /WE = Low, /RAS, /CAS = High)

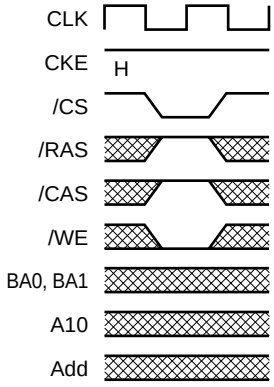
After the command execution, deep power down mode continues while CKE remains low. When CKE goes high, the Mobile RAM exits the deep power down mode. Before executing deep power down, all banks must be precharged.



Deep power down entry command

Burst stop command (/CS = /WE = Low, /RAS, /CAS = High)

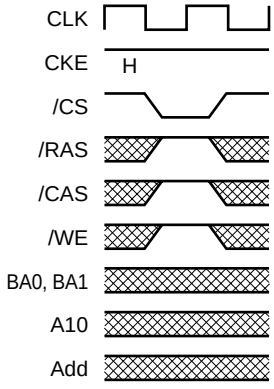
This command can stop the current burst operation.



Burst stop command

No operation (/CS = Low, /RAS, /CAS, /WE = High)

This command is not an execution command. No operations begin or terminate by this command.



No operation

Truth Table

Command Truth Table

Function	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	BA1	BA0	A10	A11, A12, A9 - A0
Device deselect	DESL	H	×	H	×	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×	×
Burst stop	BST	H	H	L	H	H	L	×	×	×	×
Read	READ	H	×	L	H	L	H	V	V	L	V
Read with auto precharge	READA	H	×	L	H	L	H	V	V	H	V
Write	WRIT	H	×	L	H	L	L	V	V	L	V
Write with auto precharge	WRITA	H	×	L	H	L	L	V	V	H	V
Bank activate	ACT	H	×	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	V	L	×
Precharge all banks	PALL	H	×	L	L	H	L	×	×	H	×
Mode register set	MRS	H	×	L	L	L	L	L	L	L	V
Extended mode register set	EMRS	H	×	L	L	L	L	H	L	L	V

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data

DQM Truth Table

Function	Symbol	CKE n – 1	CKE n	DQM 0	DQM 1	DQM 2	DQM 3
Data write / output enable	ENB	H	×	L	L	L	L
Data mask / output disable	MASK	H	×	H	H	H	H
DQ0 to DQ7 write enable/output enable	ENB0	H	×	L	×	×	×
DQ8 to DQ15 write enable/output enable	ENB1	H	×	×	L	×	×
DQ16 to DQ23 write enable/output enable	ENB2	H	×	×	×	L	×
DQ24 to DQ31 write enable/output enable	ENB3	H	×	×	×	×	L
DQ0 to DQ7 write inhibit/output disable	MASK0	H	×	H	×	×	×
DQ8 to DQ15 write inhibit/output disable	MASK 1	H	×	×	H	×	×
DQ16 to DQ23 write inhibit/output disable	MASK 2	H	×	×	×	H	×
DQ24 to DQ31 write inhibit/output disable	MASK 3	H	×	×	×	×	H

Remark: H: VIH. L: VIL. ×: VIH or VIL

CKE Truth Table

Current state	Function	Symbol	CKE n – 1	CKE n	/CS	/RAS	/CAS	/WE	Address
Activating	Clock suspend mode entry		H	L	×	×	×	×	×
Any	Clock suspend mode		L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit		L	H	×	×	×	×	×
Idle	Auto refresh command	REF	H	H	L	L	L	H	×
Idle	Self refresh entry	SELF	H	L	L	L	L	H	×
Idle	Power down entry	PD	H	L	L	H	H	H	×
			H	L	H	×	×	×	×
Idle	Deep power down entry	DPD	H	L	L	H	H	L	×
Self refresh	Self refresh exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Power down	Power down exit		L	H	L	H	H	H	×
			L	H	H	×	×	×	×
Deep power down	Deep power down exit		L	H	×	×	×	×	×

Remark: H: VIH. L: VIL. ×: VIH or VIL

Function Truth Table

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Idle	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	H	L	×	BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	→ Row activating	
	L	L	H	L	BA, A10	PRE/PALL	Nop	
	L	L	L	H	×	REF	Auto refresh	
	L	L	L	L	OC, BA1= L	MRS	Mode register set	
	L	L	L	L	OC, BA1= H	EMRS	Extended mode register set	
Row active	H	×	×	×	×	DESL	Nop	
	L	H	H	H	×	NOP	Nop	
	L	H	H	L	×	BST	Nop	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	3
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin write	3
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Precharge/Precharge all banks	4
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Read	H	×	×	×	×	DESL	Continue burst to end → Row active	
	L	H	H	H	×	NOP	Continue burst to end → Row active	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read	5
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write	5, 6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst → Precharging	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write	H	×	×	×	×	DESL	Continue burst to end → Write recovering	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering	
	L	H	H	L	×	BST	Burst stop → Row active	
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP	5, 6
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP	5
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst → Precharging	7
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Read with auto	H	×	×	×	×	DESL	Continue burst to end → Precharging	
precharge	L	H	H	H	×	NOP	Continue burst to end → Precharging	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write with auto precharge	H	×	×	×	×	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	×	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Precharging	H	×	×	×	×	DESL	Nop → Enter idle after tRP	
	L	H	H	H	×	NOP	Nop → Enter idle after tRP	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	Nop → Enter idle after tRP	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Row activating	H	×	×	×	×	DESL	Nop → Enter bank active after tRCD	
	L	H	H	H	×	NOP	Nop → Enter bank active after tRCD	
	L	H	H	L	×	BST	ILLEGAL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	2
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2
	L	L	H	H	BA, RA	ACT	ILLEGAL	2, 8
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

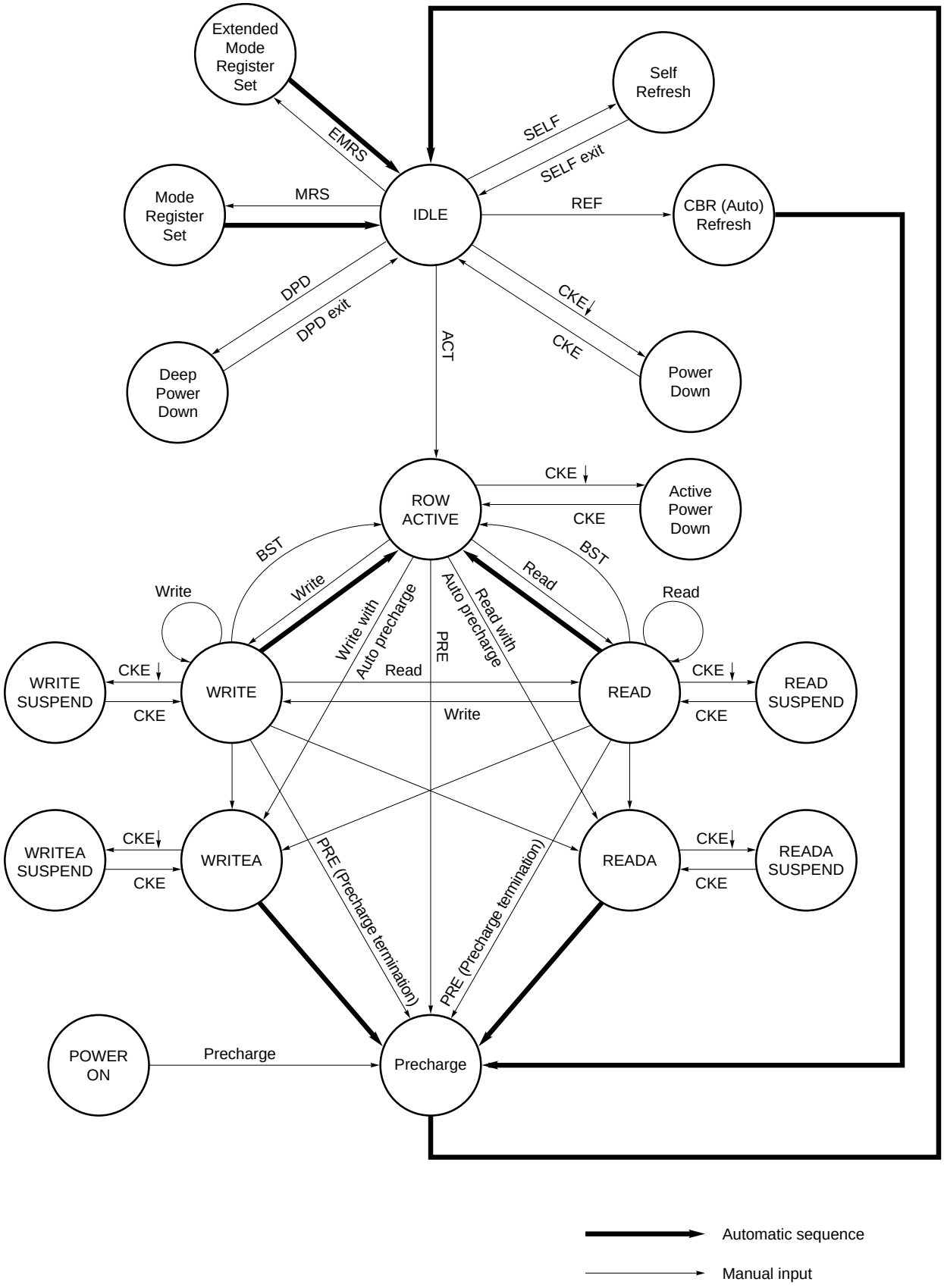
Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Write recovering	H	×	×	×	×	DESL	Nop → Enter row active after tDPL	
	L	H	H	H	×	NOP	Nop → Enter row active after tDPL	
	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	Begin read	6
	L	H	L	L	BA, CA, A10	WRIT/ WRITA	Begin new write	
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Write recovering	H	×	×	×	×	DESL	Nop → Enter precharge after tDPL	
with auto	L	H	H	H	×	NOP	Nop → Enter precharge after tDPL	
precharge	L	H	H	L	×	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	2, 6
	L	L	H	H	BA, RA	ACT	ILLEGAL	2
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	2
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Refresh	H	×	×	×	×	DESL	Nop → Enter idle after tRC1	
	L	H	H	H	×	NOP	Nop → Enter idle after tRC1	
	L	H	H	L	×	BST	Nop → Enter idle after tRC1	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	
Mode register	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
accessing	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	×	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Action	Notes
Extended mode	H	×	×	×	×	DESL	Nop → Enter idle after tRSC	
register	L	H	H	H	×	NOP	Nop → Enter idle after tRSC	
accessing	L	H	H	L	×	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL	
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA, RA	ACT	ILLEGAL	
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL	
	L	L	L	H	×	REF	ILLEGAL	
	L	L	L	L	OC, BA0,BA1	MRS/EMRS	ILLEGAL	

Remark: H: VIH. L: VIL. ×: VIH or VIL, V = Valid data
BA: Bank Address, CA: Column Address, RA: Row Address, OC: Op-Code

Notes: 1. All entries assume that CKE is active (CKE_{n-1}=CKE_n=H).
2. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
3. Illegal if tRCD is not satisfied.
4. Illegal if tRAS is not satisfied.
5. Must satisfy burst interrupt condition.
6. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
7. Must mask preceding data which don't satisfy tDPL.
8. Illegal if tRRD is not satisfied.

Simplified State Diagram



Initialization

The synchronous DRAM is initialized in the power-on sequence according to the following.

(1) To stabilize internal circuits, when power is applied, a 200 μs or longer pause must precede any signal toggling.

(2) After the pause, all banks must be precharged using the Precharge command (The Precharge all banks command is convenient).

(3) Once the precharge is completed and the minimum tRP is satisfied, two or more Auto refresh must be performed.

(4) Both the mode register and the extended mode register must be programmed. After the mode register set cycle or the extended mode register set cycle, tRSC (2 CLK minimum) pause must be satisfied.

Remarks:

1 The sequence of Auto refresh, mode register programming and extended mode register programming above may be transposed.

2 CKE and DQM must be held high until the Precharge command is issued to ensure data-bus High-Z.

Programming Mode Registers

The mode register and extended mode register are programmed by the Mode register set command and Extended mode register command, respectively using address bits A12 through A0, BA0 and BA1 as data inputs. The registers retain data until they are re-programmed, or the device enters into the deep power down or the device loses power.

Mode register

The mode register has three fields;

Options	:	A12 through A7
/CAS latency	:	A6 through A4
Wrap type	:	A3
Burst length	:	A2 through A0

Following mode register programming, no command can be issued before at least 2 CLK have elapsed.

/CAS Latency

/CAS latency is the most critical of the parameters being set. It tells the device how many clocks must elapse before the data will be available. The value is determined by the frequency of the clock and the speed grade of the device.

Burst Length

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become High-Z. The burst length is programmable as 1, 2, 4, 8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either “Sequential” or “Interleave”. The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. “Burst Length Sequence” shows the addressing sequence for each burst length using them. Both sequences support bursts of 1, 2, 4 and 8. Additionally, sequence supports the full page length.

Extended Mode Register

The extended mode register has four fields;

Options	: A12 through A7, A4, A3
Auto Temperature Compensated Self Refresh	: A9
Driver Strength	: A6 through A5
Partial Array Self Refresh	: A2 through A0

Following extended mode register programming, no command can be issued before at least 2 CLK have elapsed.

Driver Strength

By setting specific parameter on A6 and A5, driving capability of data output drivers is selected.

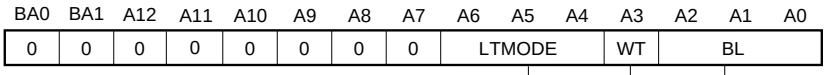
Auto Temperature Compensated Self Refresh (ATCSR)

With the built-in temperature sensor, the internal self refresh frequency is controlled autonomously.

Partial Array Self Refresh

Memory array size to be refreshed during self refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self refresh.

Mode Register Definition

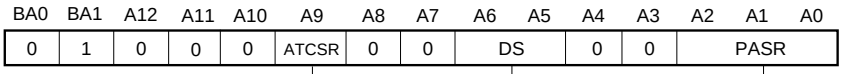


Mode Register Set

Latency mode	Bits6-4	/CAS latency
	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Burst length	Bits2-0	WT = 0	WT = 1
	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type		
	0	Sequential
	1	Interleave



Extended Mode Register Set

ATCSR	Bit9	ATCSR
	0	Enable
	1	R

Partial Array Self Refresh	Bits2-0	Refresh Array
	000	All banks
	001	Bank A & Bank B (BA1=0)
	010	Bank A (BA0=BA1=0)
	011	R
	100	R
	101	R
	110	R
	111	R

Driver Strength	Bits6-5	Strength
	00	Normal
	01	1/2 strength
	10	1/4 strength
	11	1/8 strength

Remark R : Reserved

Burst Length and Sequence

[Burst of Two]

Starting address (column address A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
0	0, 1	0, 1
1	1, 0	1, 0

[Burst of Four]

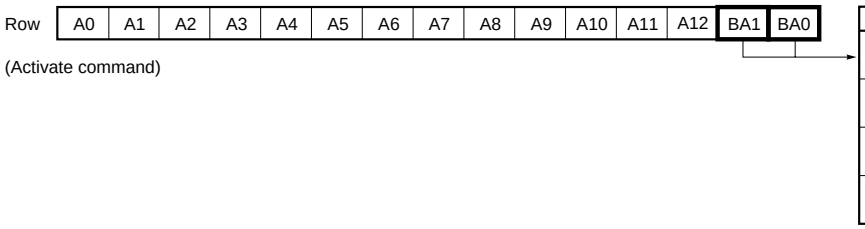
Starting address (column address A1–A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
00	0, 1, 2, 3	0, 1, 2, 3
01	1, 2, 3, 0	1, 0, 3, 2
10	2, 3, 0, 1	2, 3, 0, 1
11	3, 0, 1, 2	3, 2, 1, 0

[Burst of Eight]

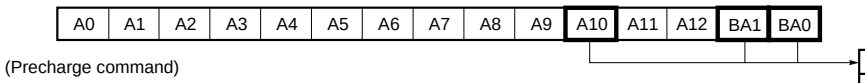
Starting address (column address A2–A0, binary)	Sequential addressing sequence (decimal)	Interleave addressing sequence (decimal)
000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
001	1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
010	2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
011	3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
101	5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
110	6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
111	7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

Full page burst is an extension of the above tables of sequential addressing, with the length being 512.

Address Bits of Bank-Select and Precharge

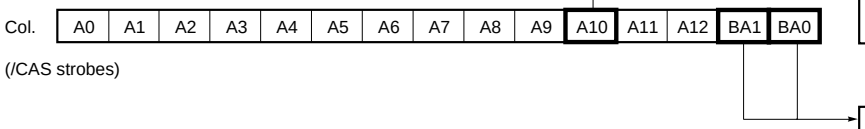


BA1	BA0	Result
0	0	**Select Bank A "Activate" command**
0	1	**Select Bank B "Activate" command**
1	0	**Select Bank C "Activate" command**
1	1	**Select Bank D "Activate" command**



A10	BA1	BA0	Result
0	0	0	**Precharge Bank A**
0	0	1	**Precharge Bank B**
0	1	0	**Precharge Bank C**
0	1	1	**Precharge Bank D**
1	x	x	**Precharge All Banks**

x : Don't care



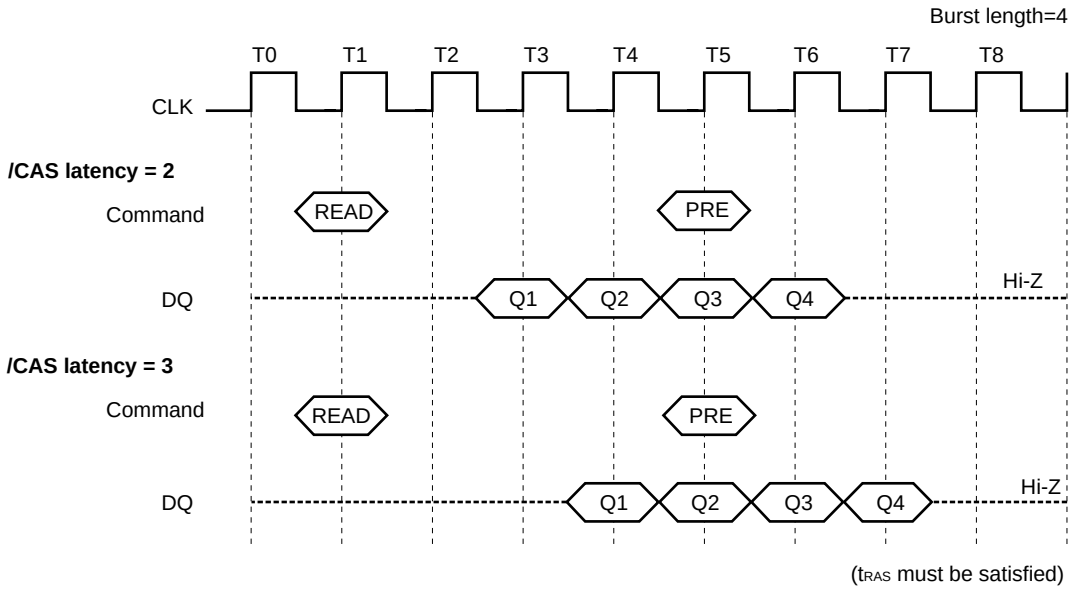
0	**disables Auto-Precharge (End of Burst)**
1	**enables Auto-Precharge (End of Burst)**

BA1	BA0	Result
0	0	**enables Read/Write commands for Bank A**
0	1	**enables Read/Write commands for Bank B**
1	0	**enables Read/Write commands for Bank C**
1	1	**enables Read/Write commands for Bank D**

Operation of the Mobile RAM

Precharge

The precharge command can be issued anytime after tRAS min. is satisfied. Soon after the precharge command is issued, precharge operation performed and the synchronous DRAM enters the idle state after tRP is satisfied. The parameter tRP is the time required to perform the precharge. The earliest timing in a read cycle that a precharge command can be issued without losing any data in the burst is as follows.



(t_{RAS} must be satisfied)

Precharge

In order to write all data to the memory cell correctly, the asynchronous parameter tDPL must be satisfied. The tDPL (min.) specification defines the earliest time that a precharge command can be issued. Minimum number of clocks is calculated by dividing tDPL (min.) with clock cycle time. In summary, the precharge command can be issued relative to reference clock that indicates the last data word is valid. In the following table, minus means clocks before the reference; plus means time after the reference.

/CAS latency	Read	Write
2	-1	+tDPL(min.)
3	-2	+tDPL(min.)

Auto Precharge

During a read or write command cycle, A10 controls whether auto precharge is selected. A10 high in the Read or Write command (Read with Auto precharge command or Write with Auto precharge command), auto precharge is selected and begins automatically. The tRAS must be satisfied with a read with auto precharge or a write with auto precharge operation. In addition, the next activate command to the bank being precharged cannot be executed until the precharge cycle ends.

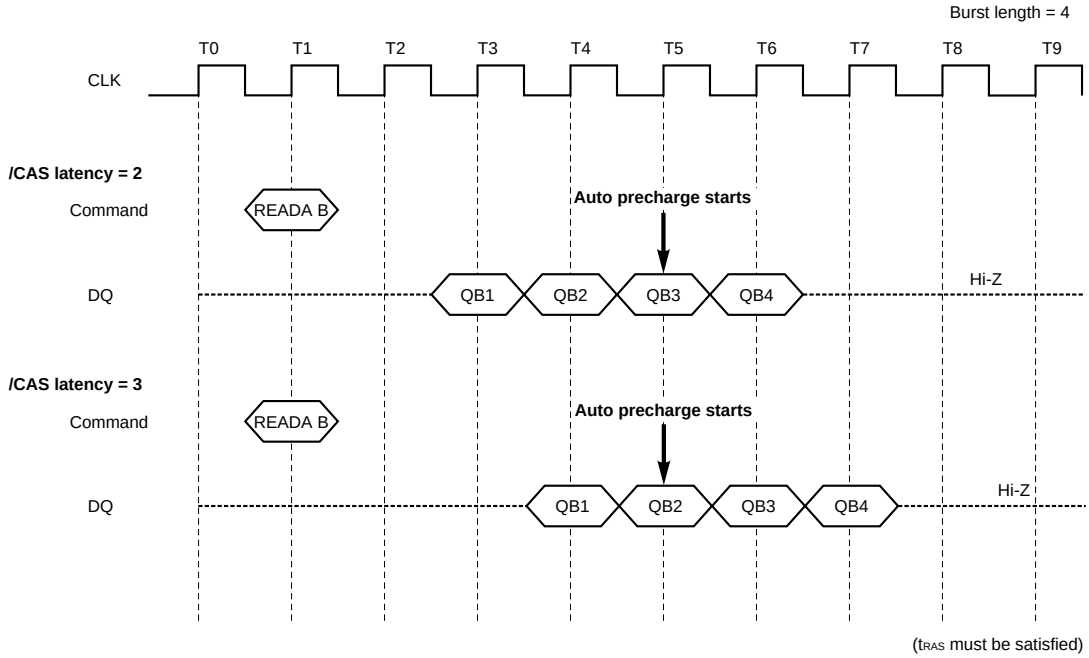
In read cycle, once auto precharge has started, an activate command to the bank can be issued after tRP has been satisfied.

In write cycle, the tDAL must be satisfied to issue the next activate command to the bank being precharged.

The timing that begins the auto precharge cycle depends on whether read or write cycle.

Read with Auto Precharge

During a read cycle, the auto precharge begins one clock earlier (/CAS latency of 2) or two clocks earlier (/CAS latency of 3) the last data word output.

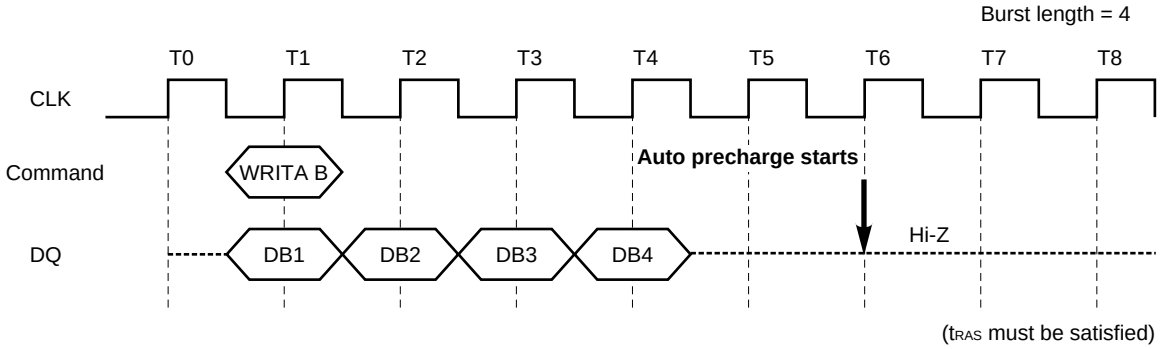


Read with Auto Precharge

Remark: READA means Read with Auto precharge

Write with Auto Precharge

During a write cycle, the auto precharge starts at the timing of 2 clocks after the last data word input to the device.



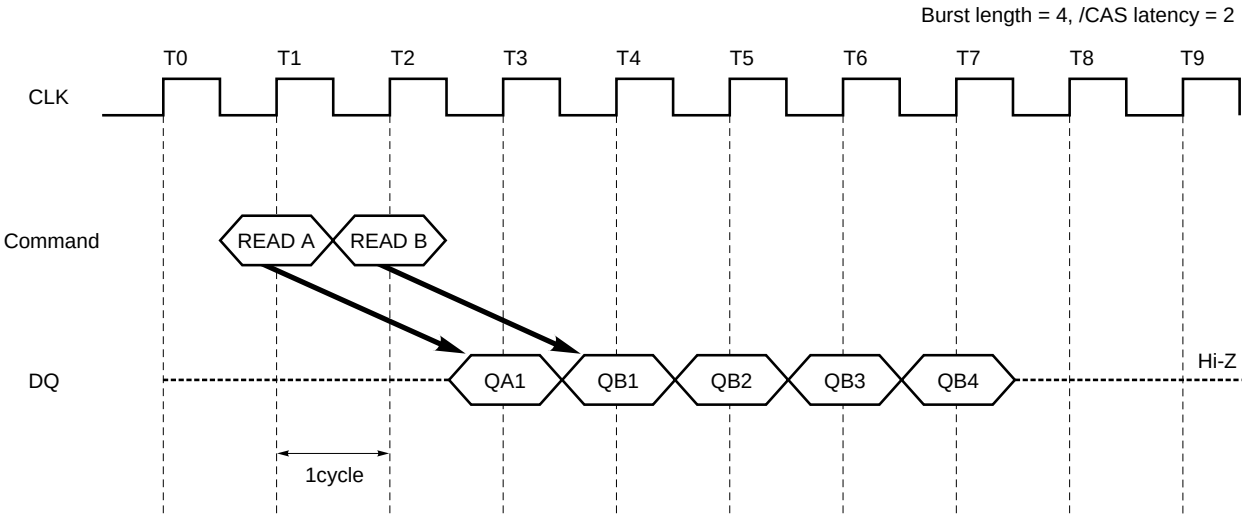
Write with Auto Precharge

Remark: WRITA means Write with Auto Precharge

Read / Write Command Interval

Read to Read Command Interval

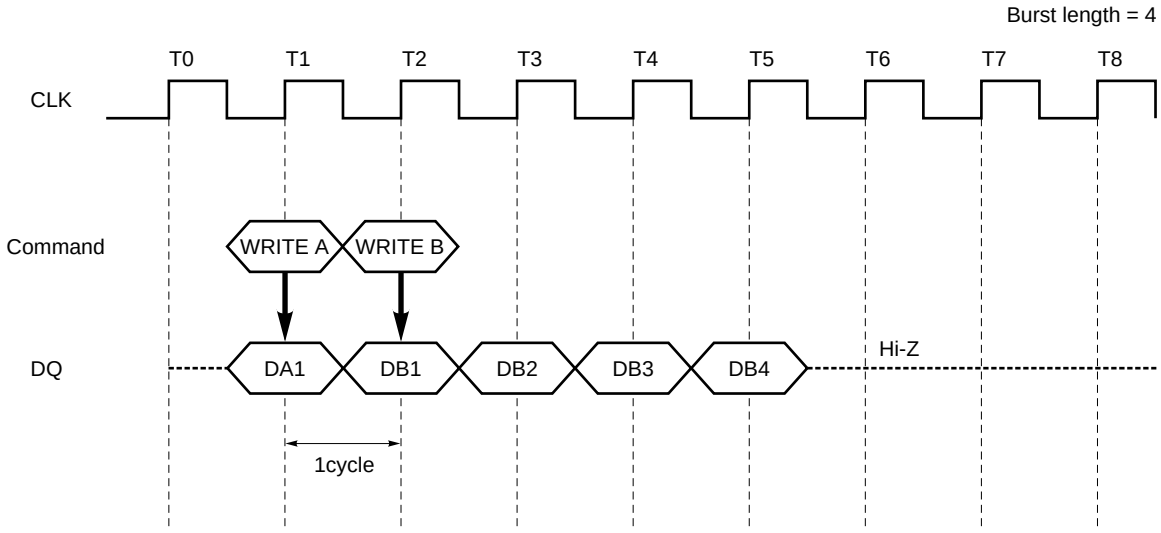
During a read cycle, when new Read command is issued, it will be effective after /CAS latency, even if the previous read operation does not completed. READ will be interrupted by another READ. The interval between the commands is 1 cycle minimum. Each Read command can be issued in every clock without any restriction.



Read to Read Command Interval

Write to Write Command Interval

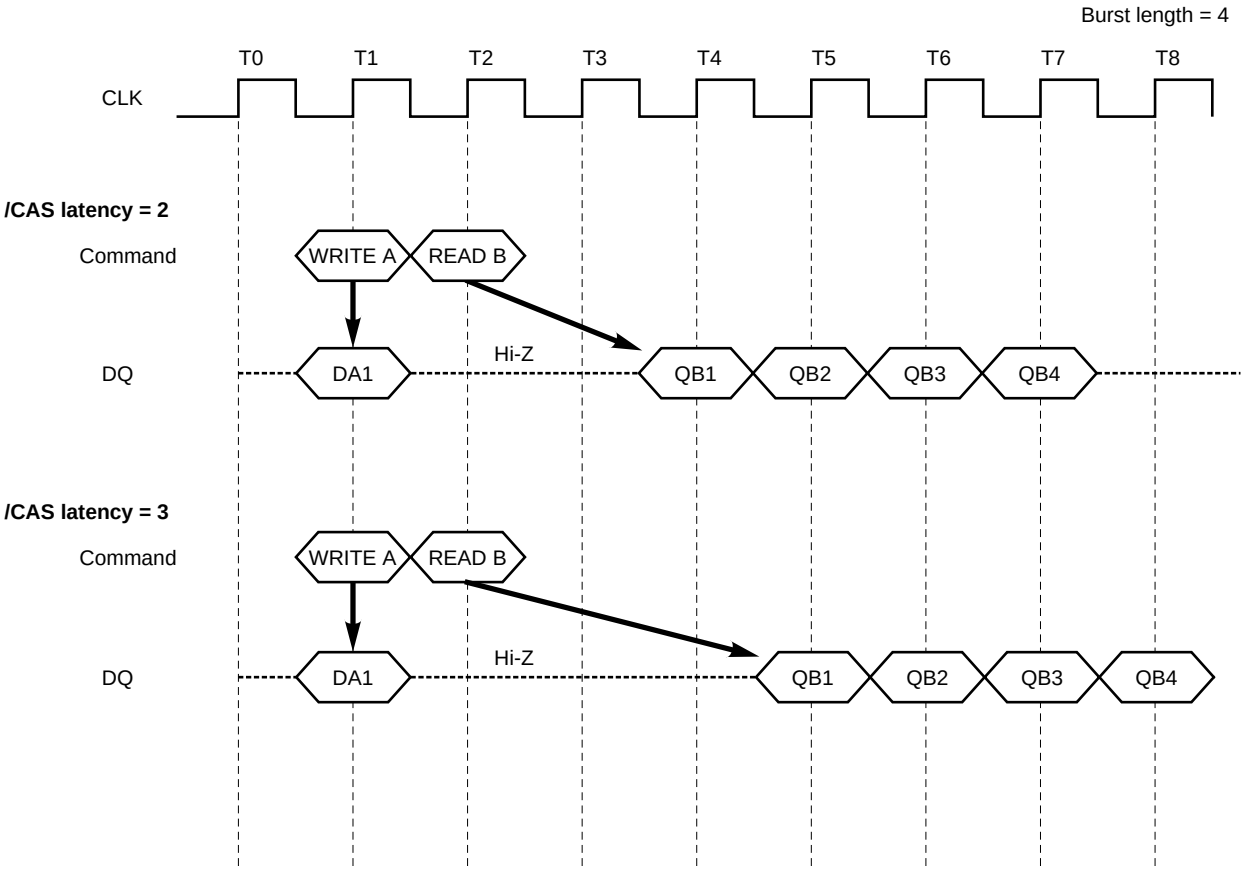
During a write cycle, when a new Write command is issued, the previous burst will terminate and the new burst will begin with a new Write command. WRITE will be interrupted by another WRITE. The interval between the commands is minimum 1 cycle. Each Write command can be issued in every clock without any restriction.



Write to Write Command Interval

Write to Read Command Interval

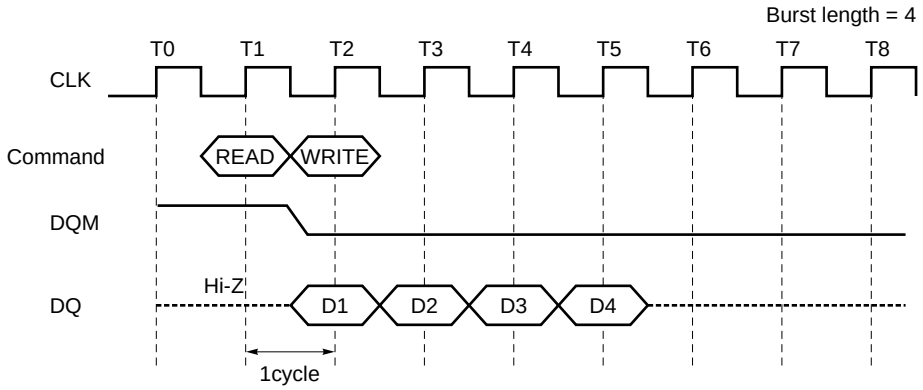
Write command and Read command interval is also 1 cycle. Only the write data before Read command will be written. The data bus must be High-Z at least one cycle prior to the first DOUT.



Write to Read Command Interval

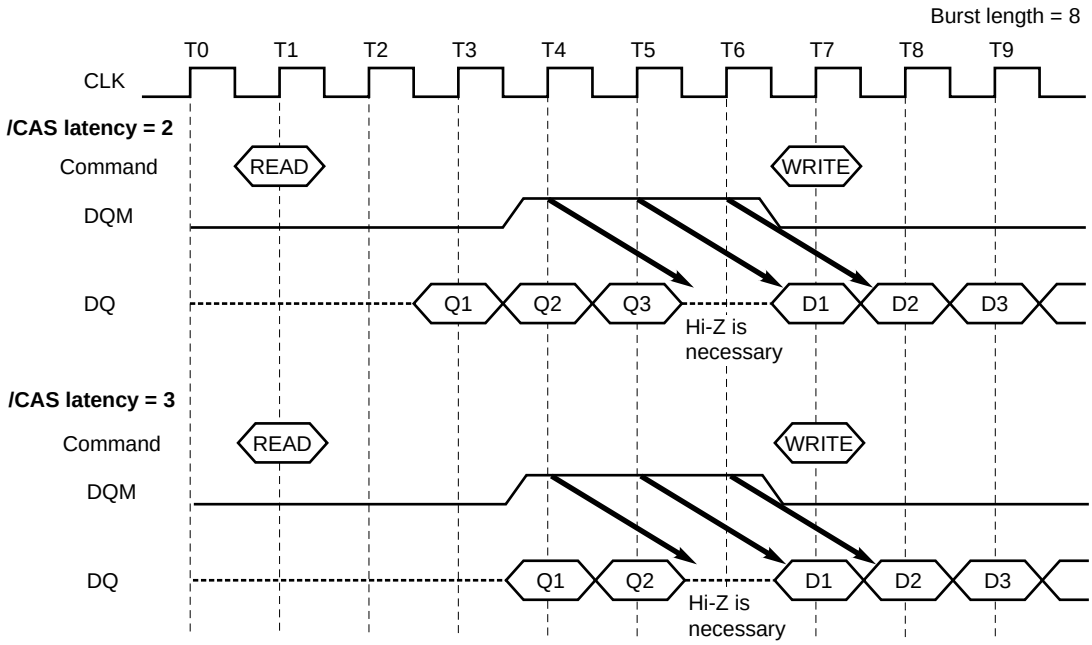
Read to Write Command Interval

During a read cycle, READ can be interrupted by WRITE. The Read and Write command interval is 1 cycle minimum. There is a restriction to avoid data conflict. The Data bus must be High-Z using DQM before WRITE.



Read to Write Command Interval 1

READ can be interrupted by WRITE. DQM must be High at least 3 clocks prior to the Write command.



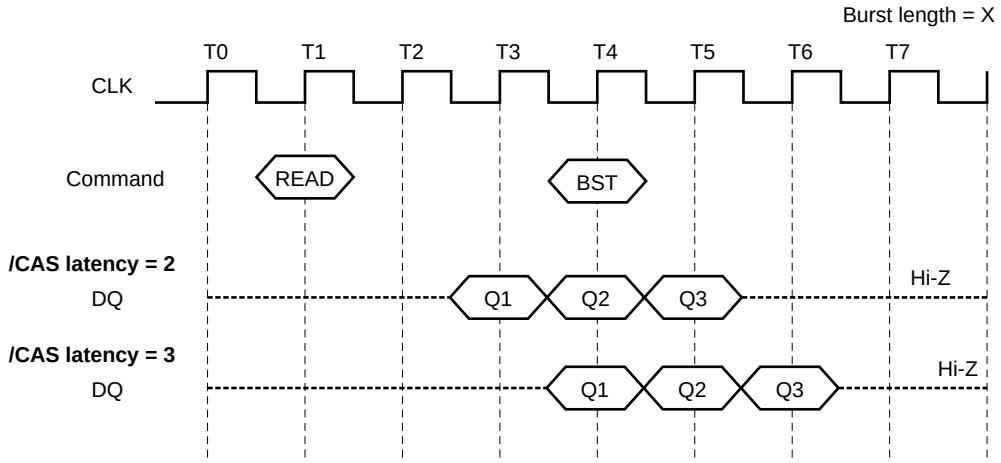
Read to Write Command Interval 2

Burst Termination

There are two methods to terminate a burst operation other than using a Read or a Write command. One is the burst stop command and the other is the precharge command.

Burst Termination in READ Cycle

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the /CAS latency from the burst stop command.

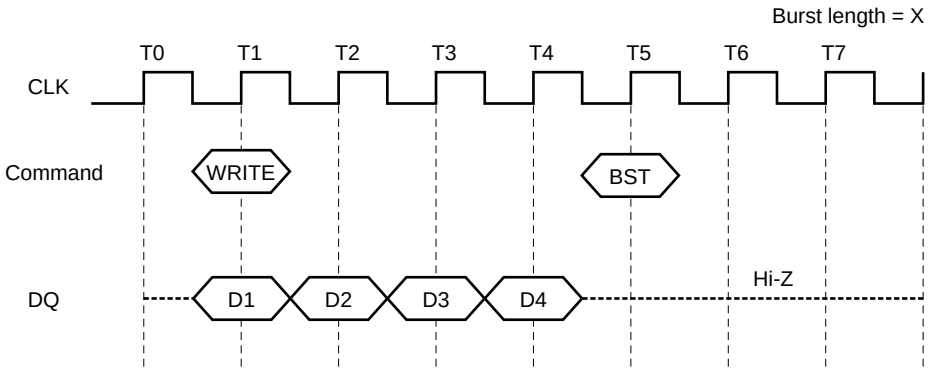


Burst Termination in READ Cycle

Remark: BST: Burst stop command

Burst Termination in WRITE Cycle

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.



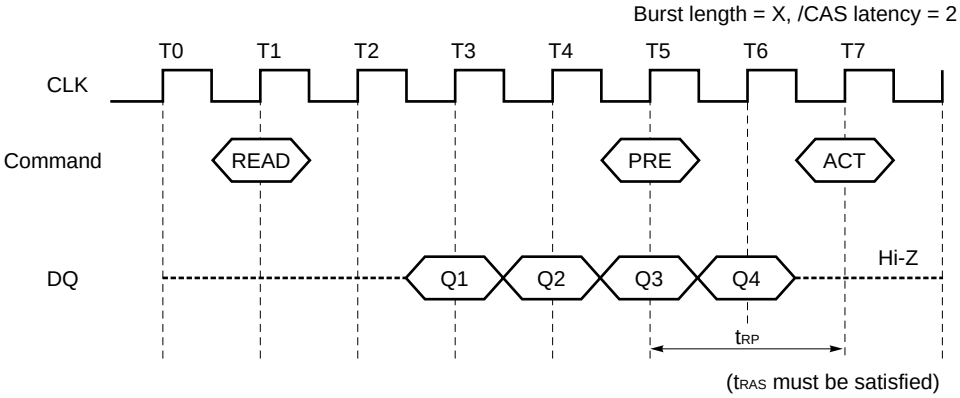
Burst Termination in WRITE Cycle

Remark: BST: Burst stop command

Precharge Termination in READ Cycle

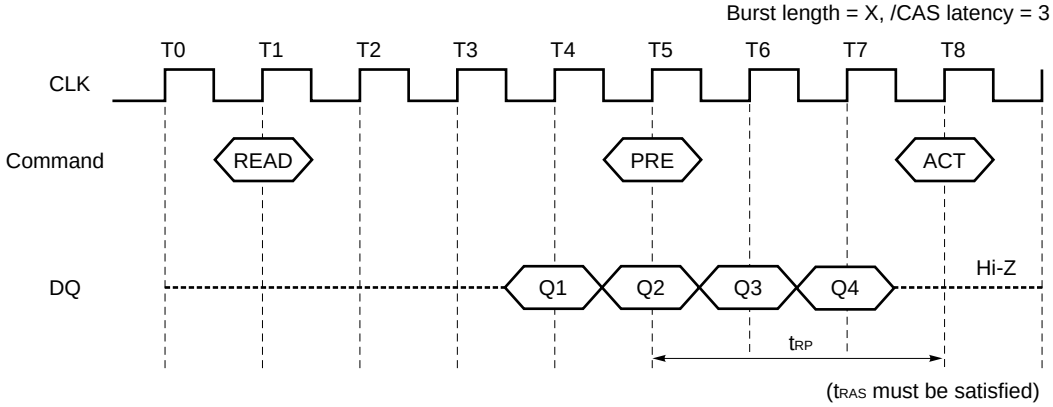
During a read cycle, the burst read operation is terminated by a precharge command. When the precharge command is issued, the burst read operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. To issue a precharge command, tRAS must be satisfied.

When /CAS latency is 2, the read data will remain valid until one clock after the precharge command.



Precharge Termination in READ Cycle (CL = 2)

When /CAS latency is 3, the read data will remain valid until two clocks after the precharge command.

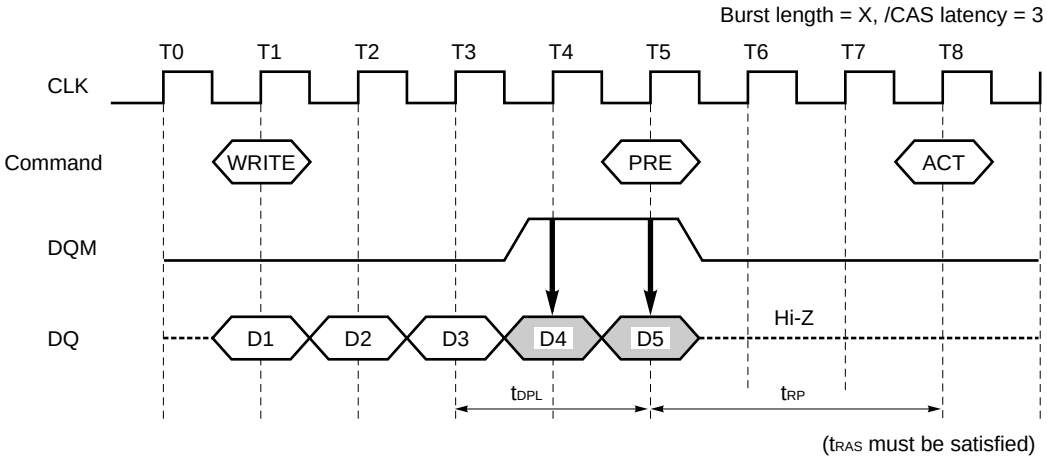


Precharge Termination in READ Cycle (CL = 3)

Precharge Termination in WRITE Cycle

During a write cycle, the burst write operation is terminated by a precharge command. When the precharge command is issued, the burst write operation is terminated and precharge starts. The same bank can be activated again after tRP from the precharge command. To issue a precharge command, tRAS must be satisfied.

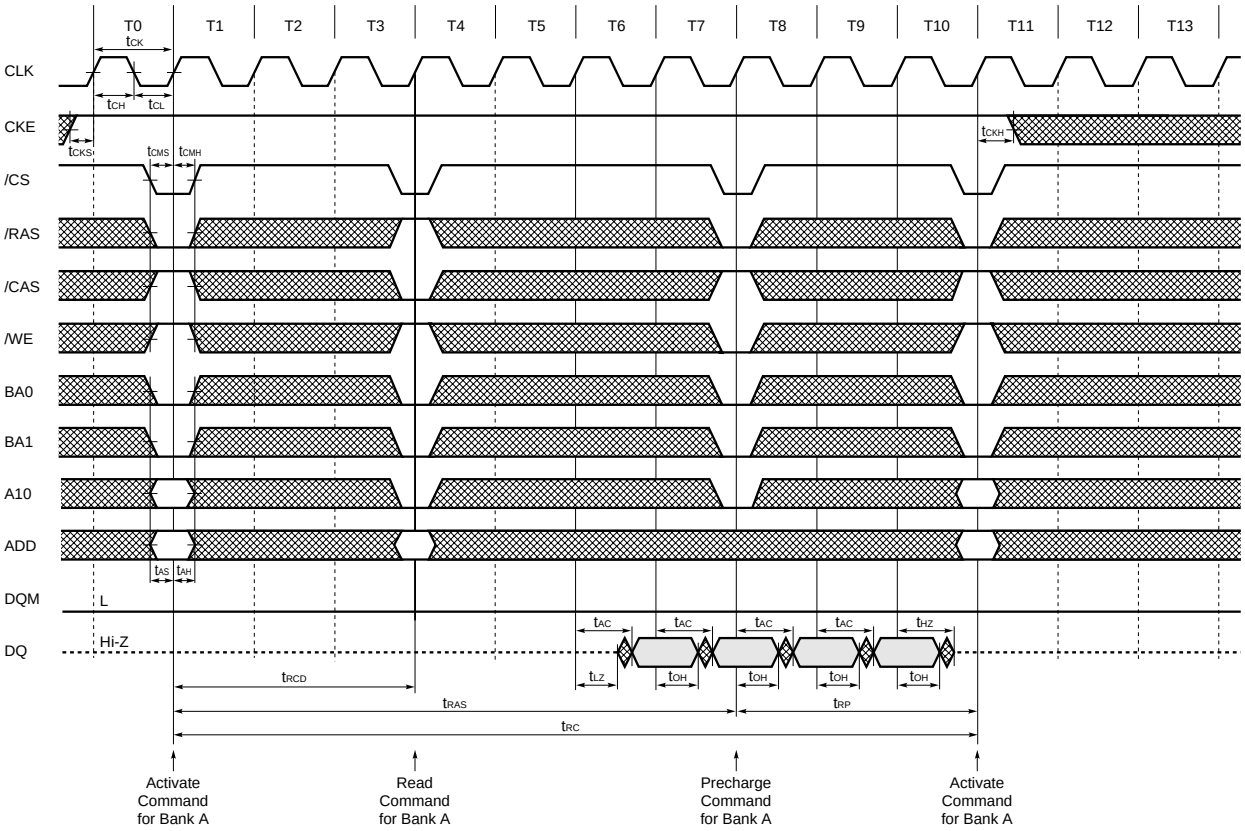
The write data written up to two clocks prior to the precharge command will be correctly stored. However, invalid data may be written at the same clock as the precharge command and one clock before the precharge command. To prevent this from happening, DQM must be high and mask the invalid data.



Precharge Termination in WRITE Cycle

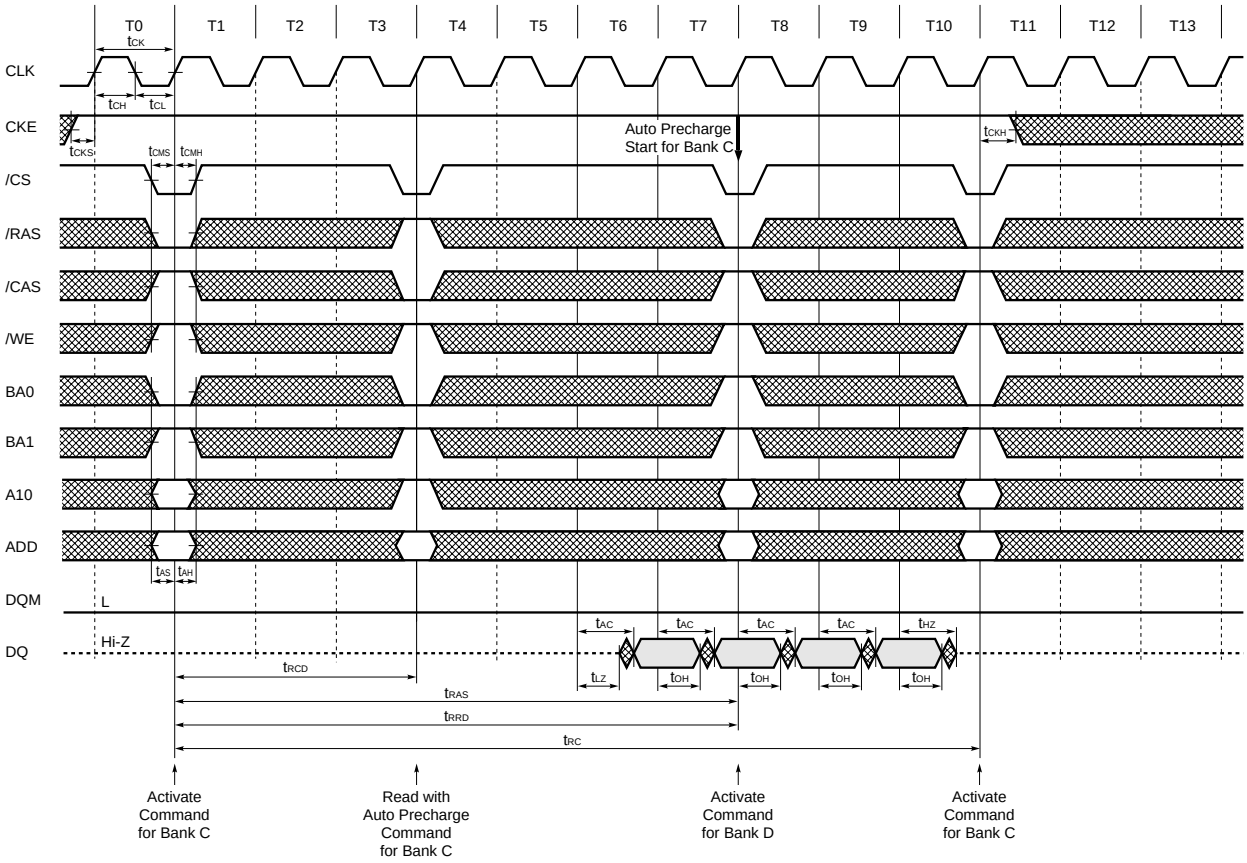
Timing Waveforms

AC Parameters for Read Timing with Manual Precharge



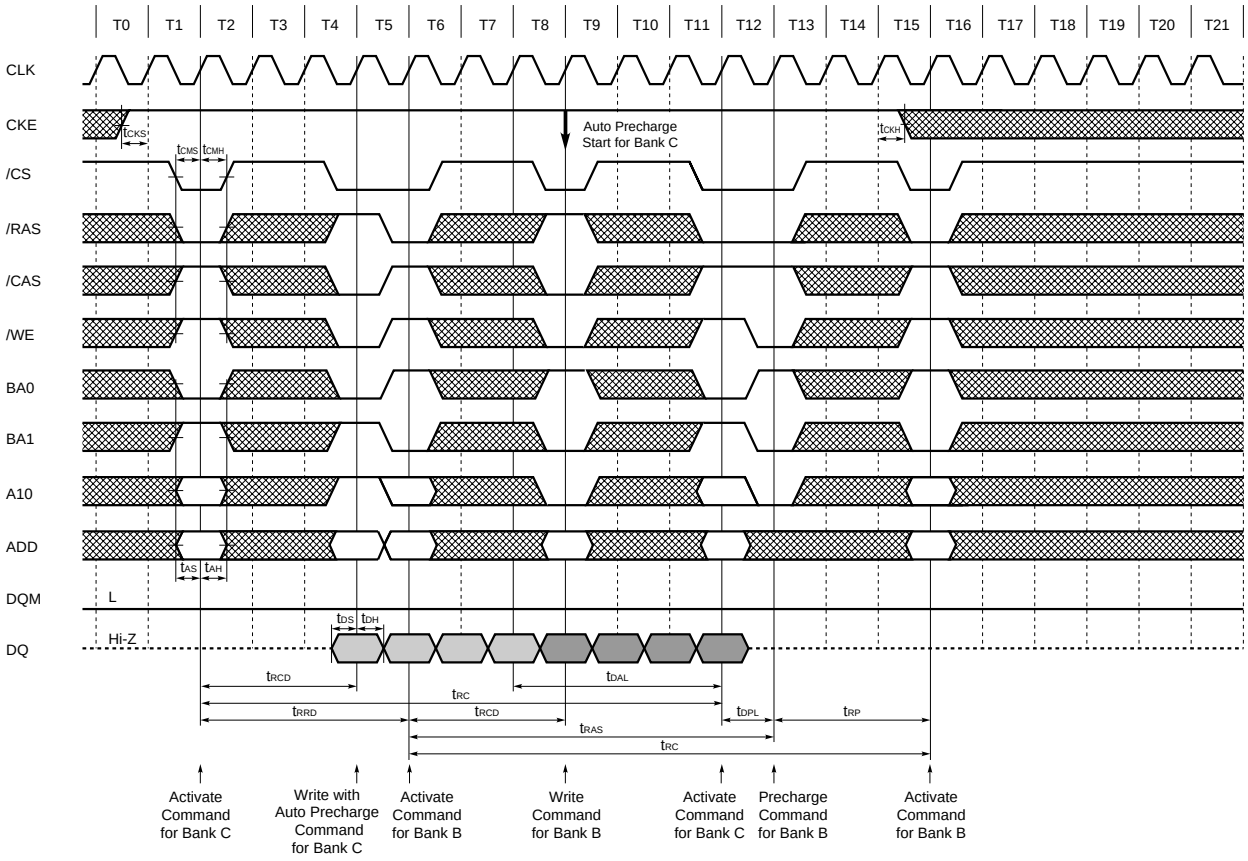
[Burst Length = 4, /CAS Latency = 3]

AC Parameters for Read Timing with Auto Precharge



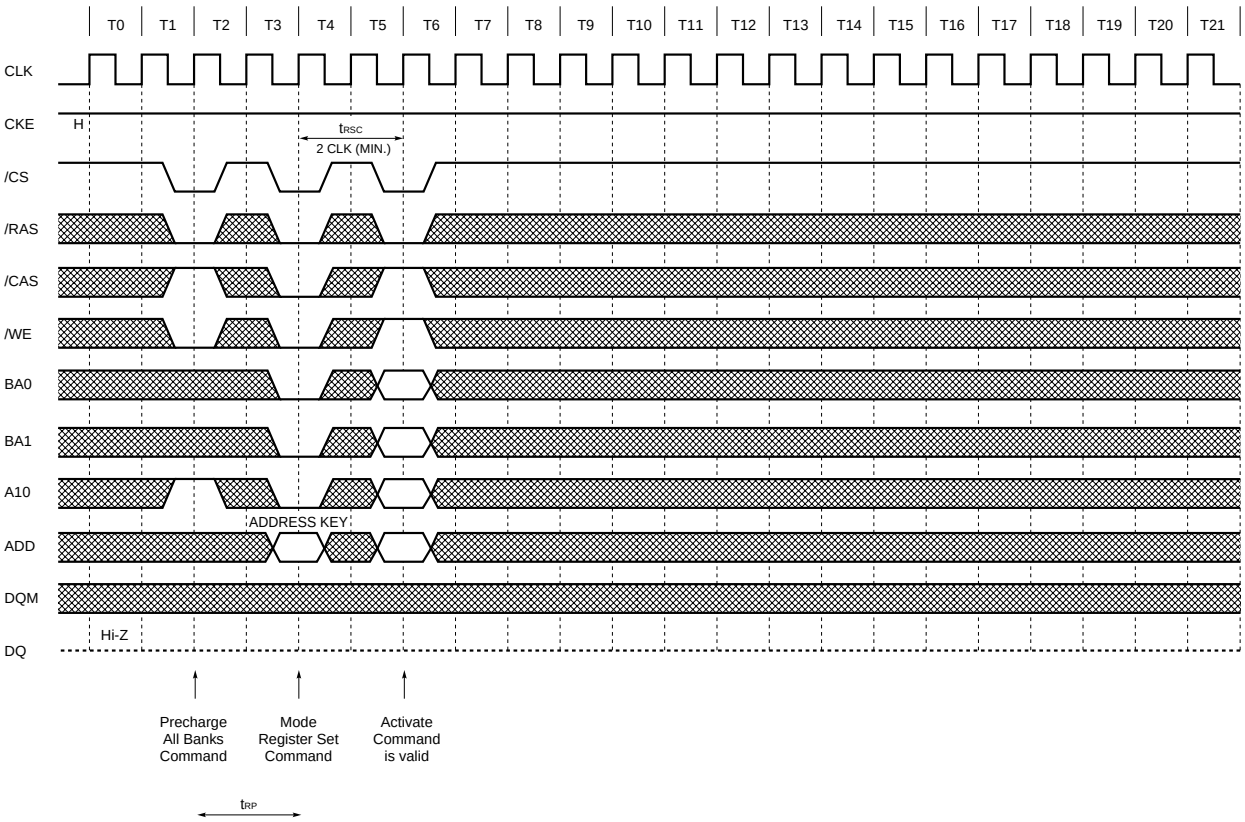
[Burst Length = 4, /CAS Latency = 3]

AC Parameters for Write Timing

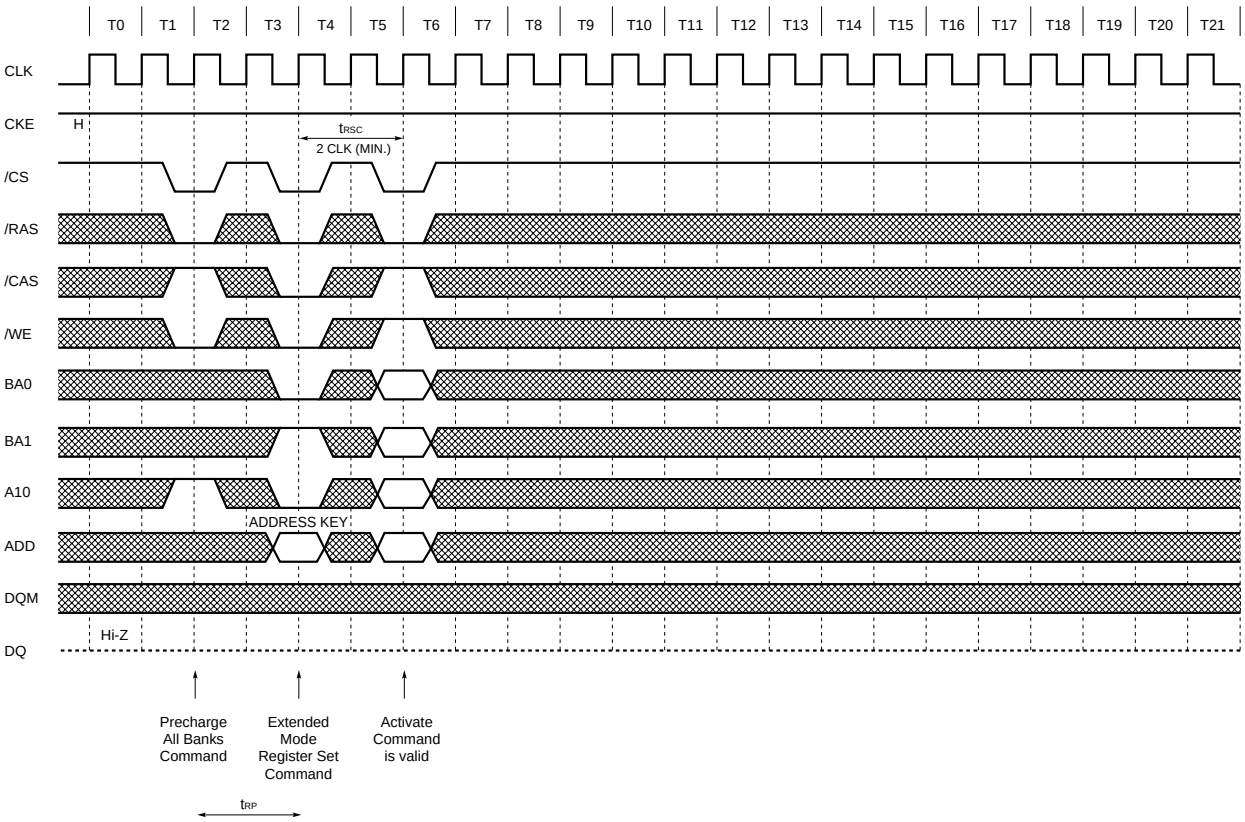


[Burst Length = 4]

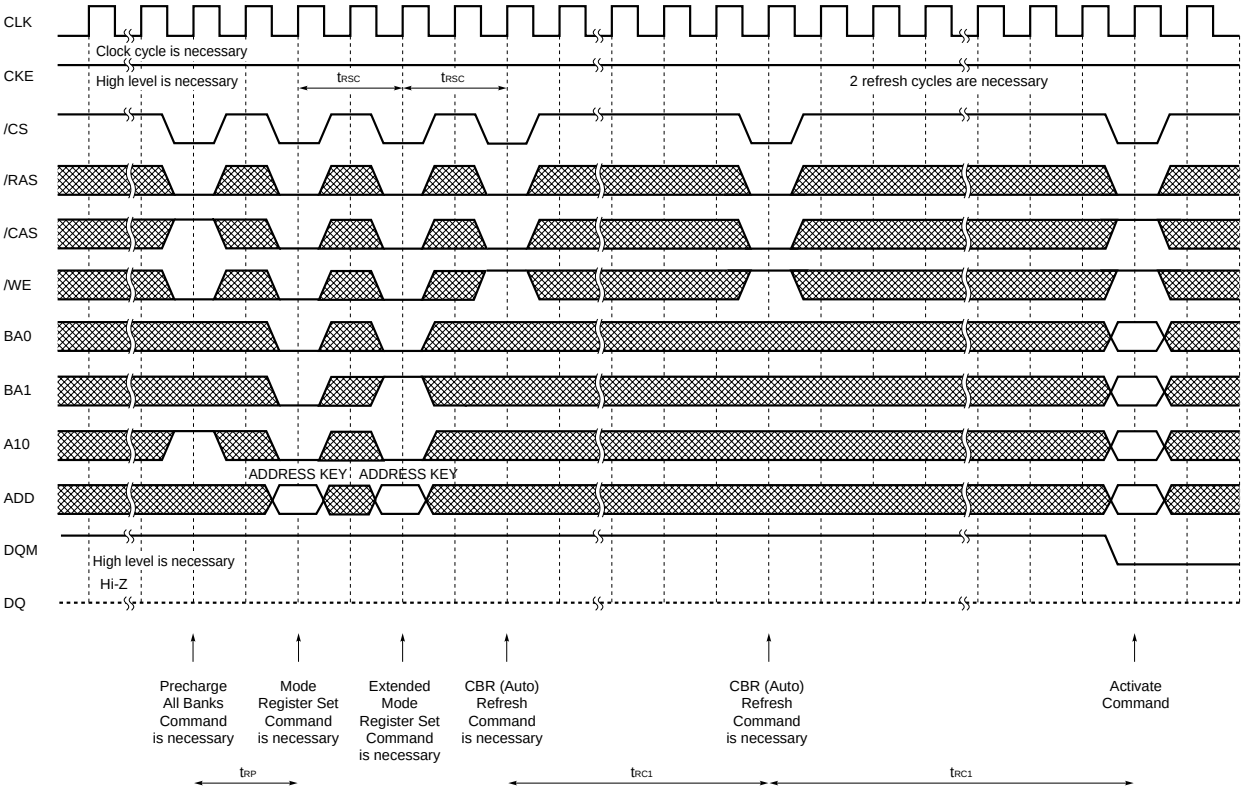
Mode Register Set



Extended Mode Register Set

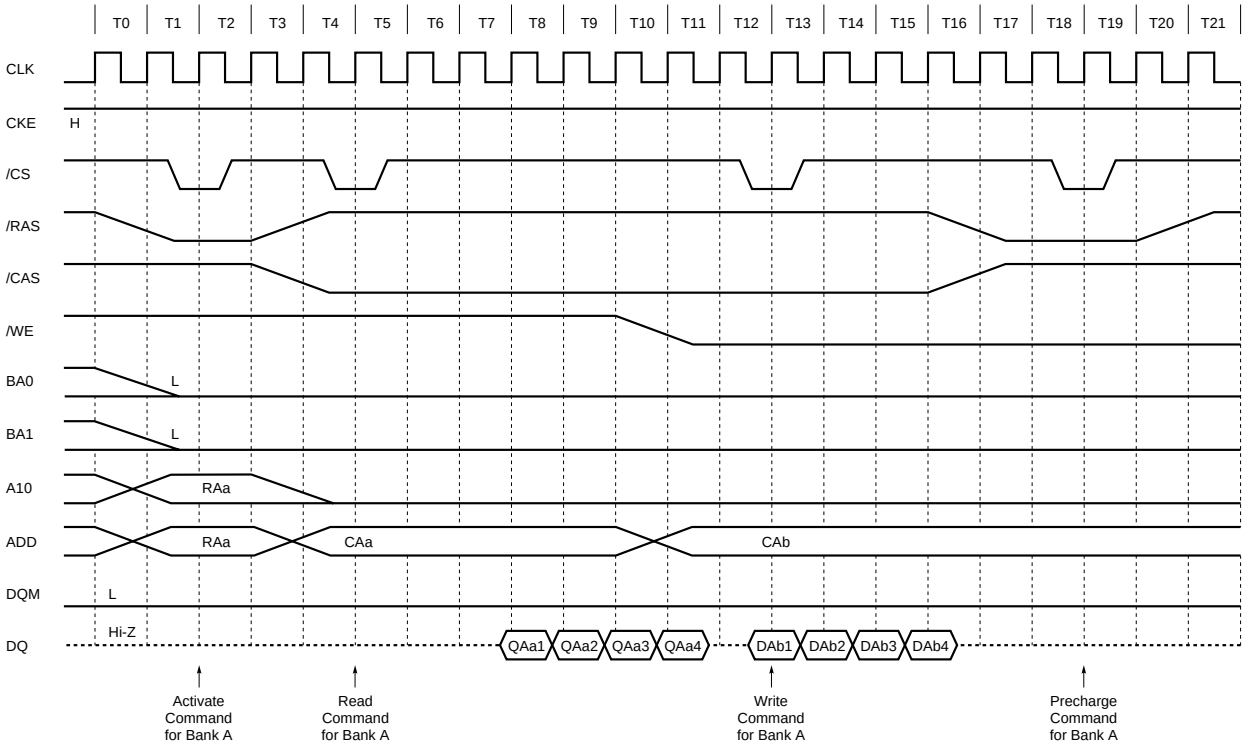


Power On Sequence



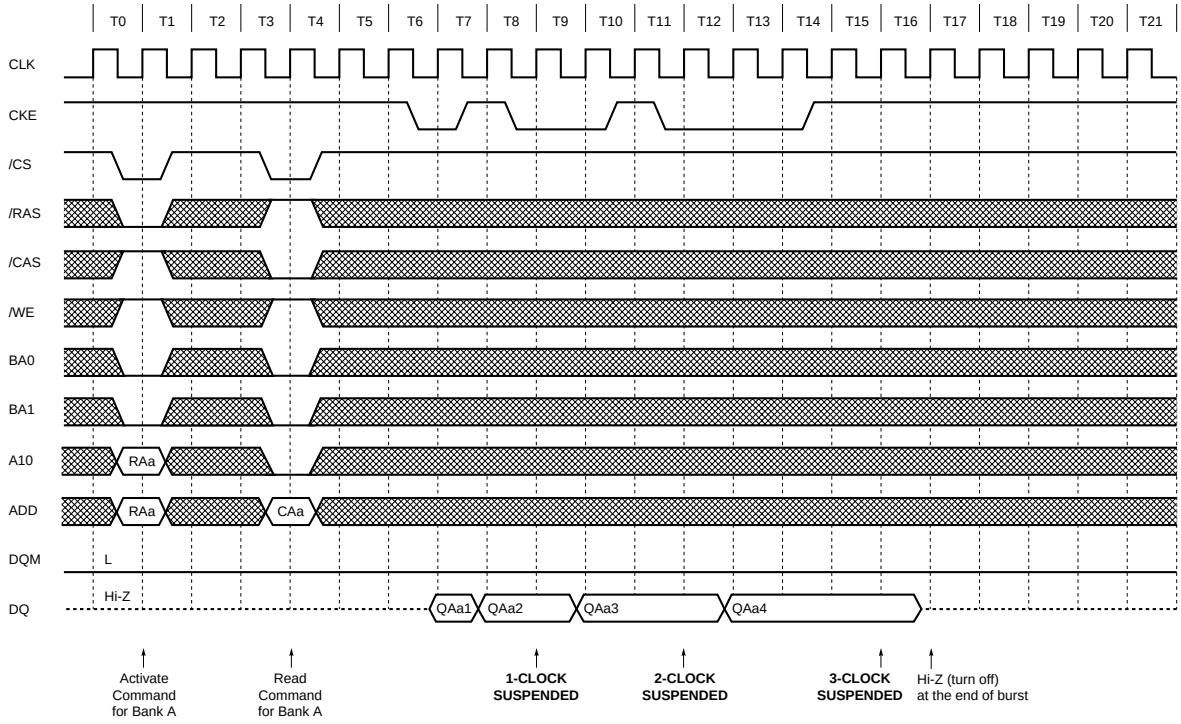
/CS Function

Only /CS signal needs to be issued at minimum rate

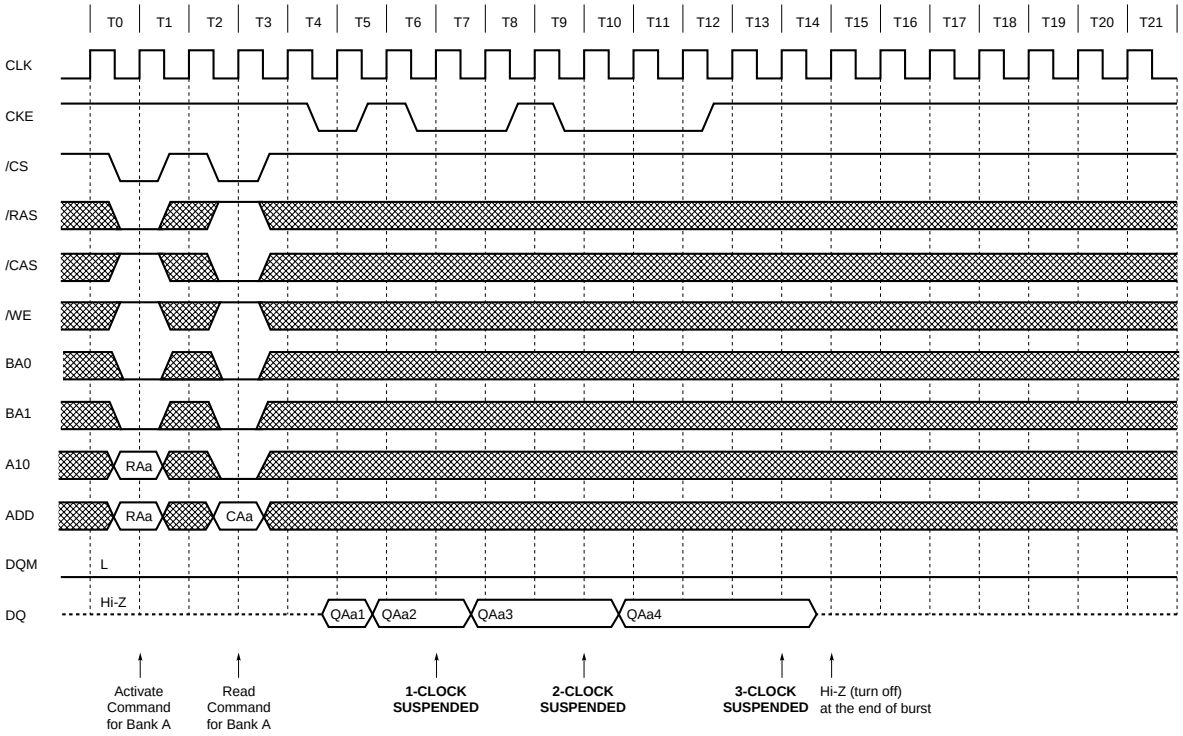


[Burst Length = 4, /CAS Latency = 3]

Clock Suspension during Burst Read

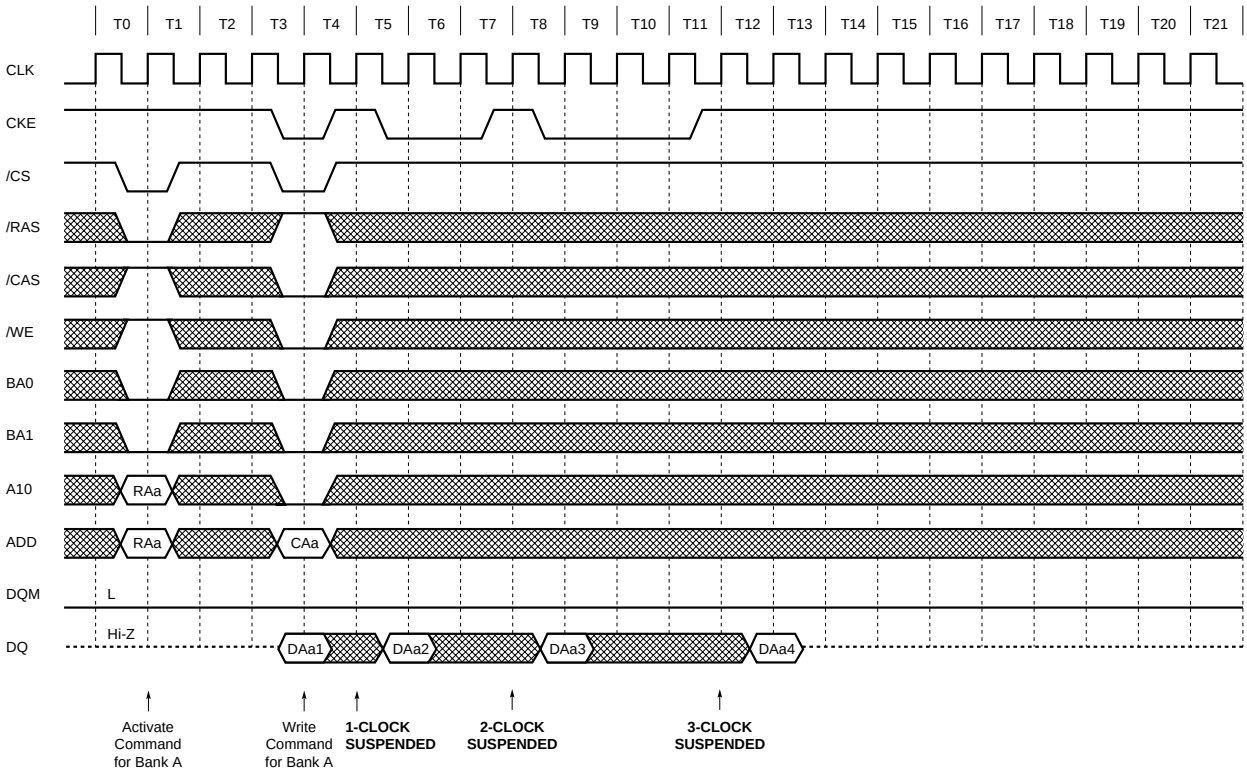


[Burst Length = 4, /CAS Latency = 3]

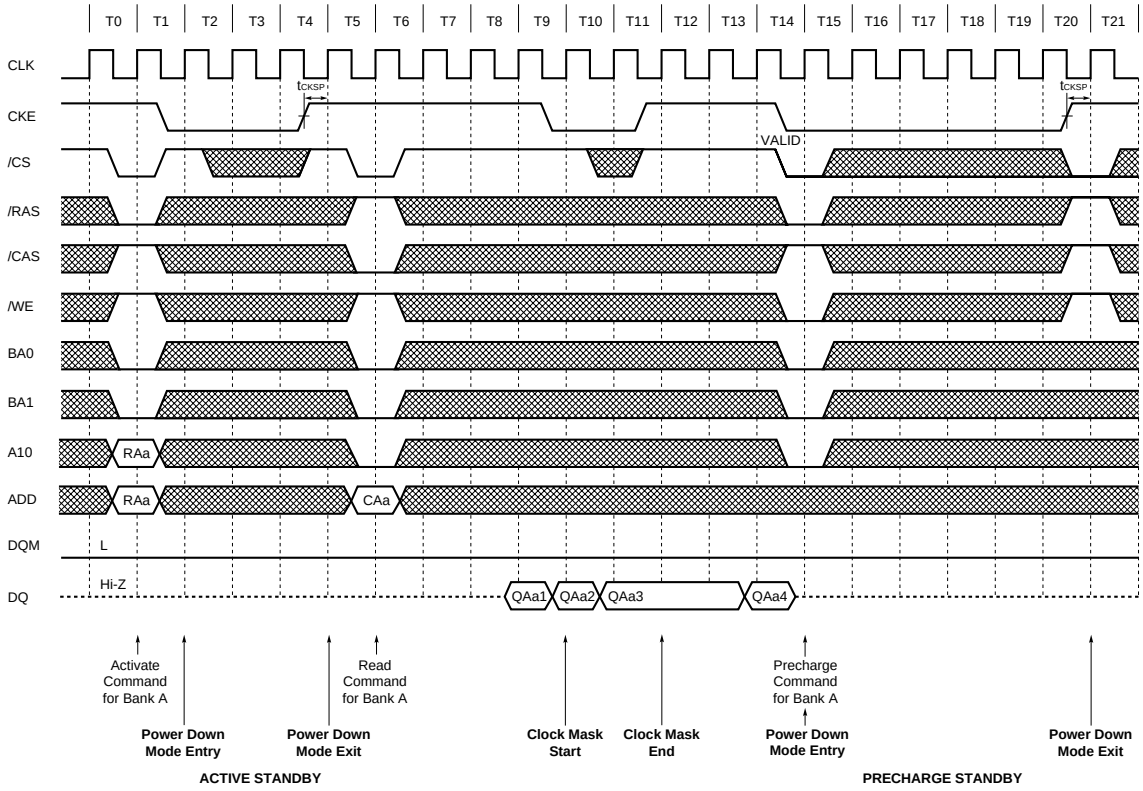


[Burst Length = 4, /CAS Latency = 2]

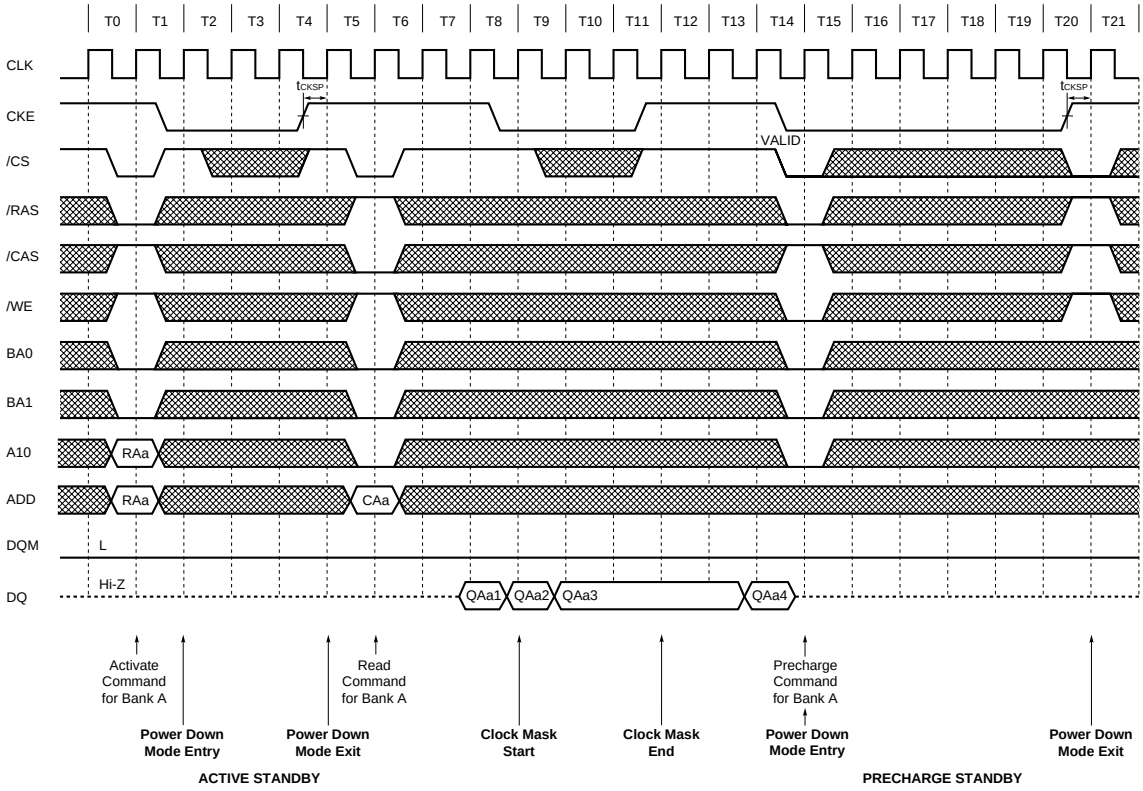
Clock Suspension during Burst Write



Power Down Mode and Clock Mask

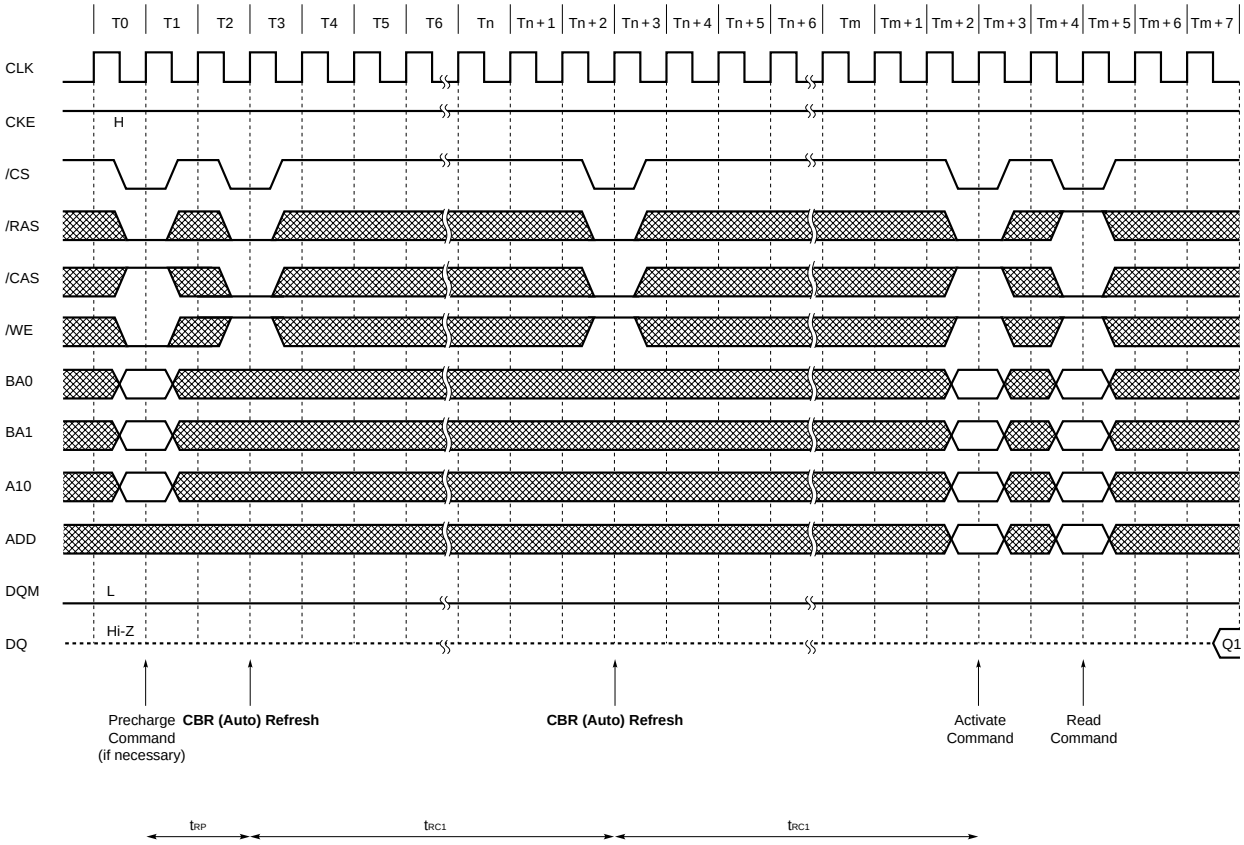


[Burst Length = 4, /CAS Latency = 3]

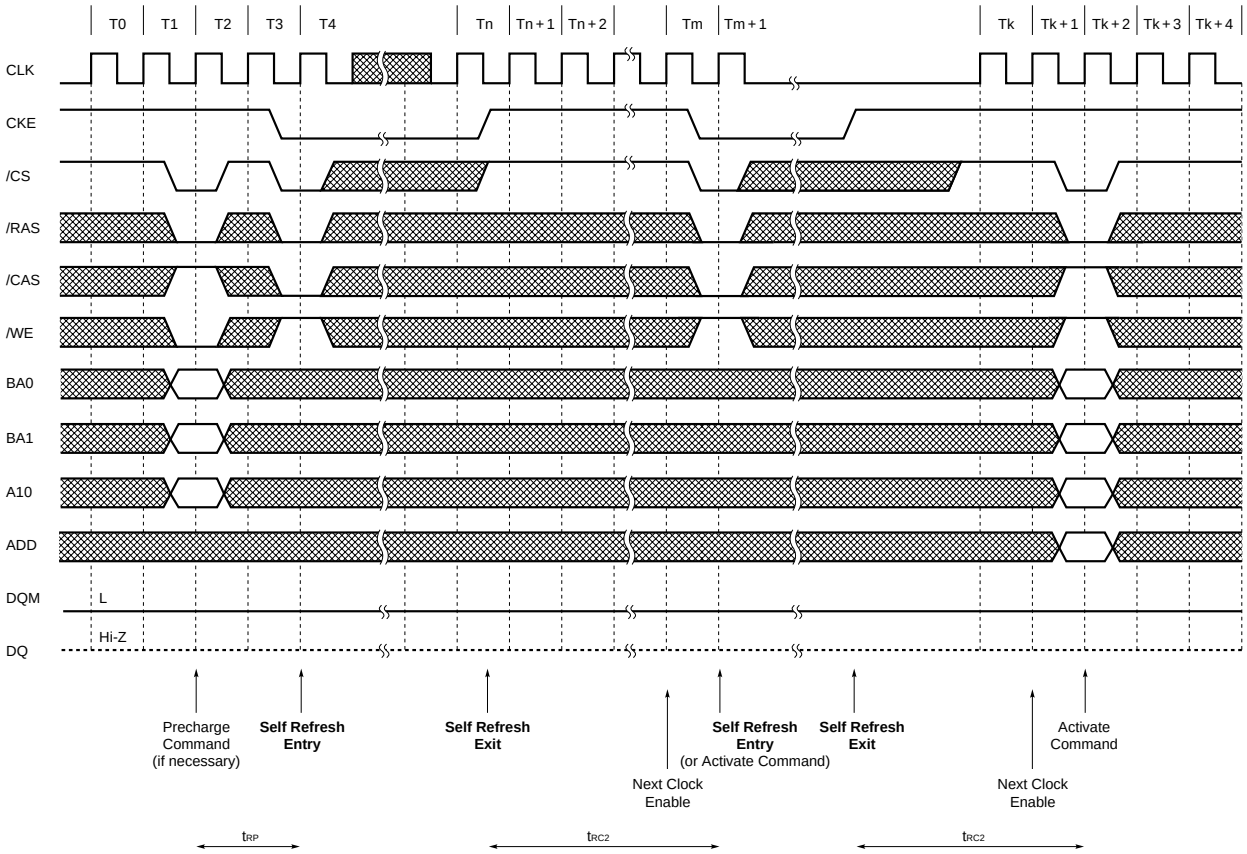


[Burst Length = 4, /CAS Latency = 2]

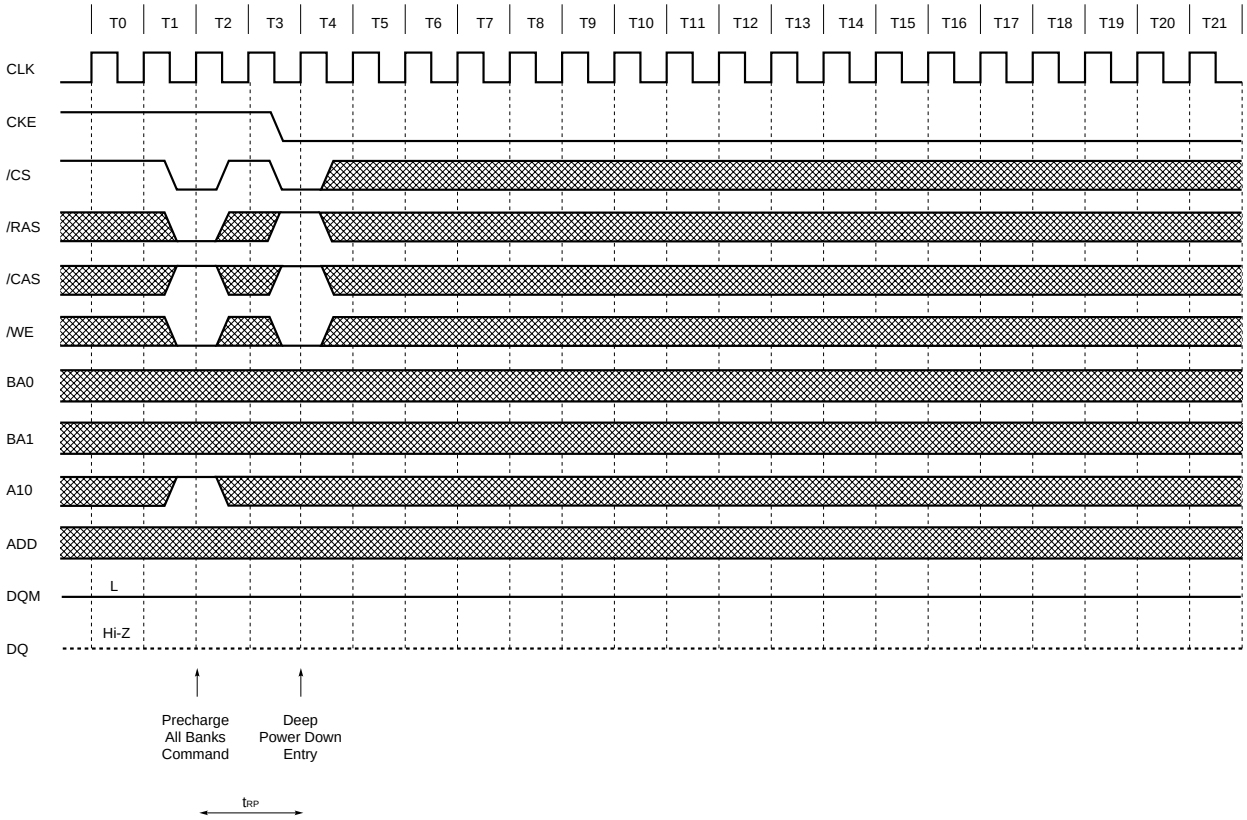
Auto Refresh



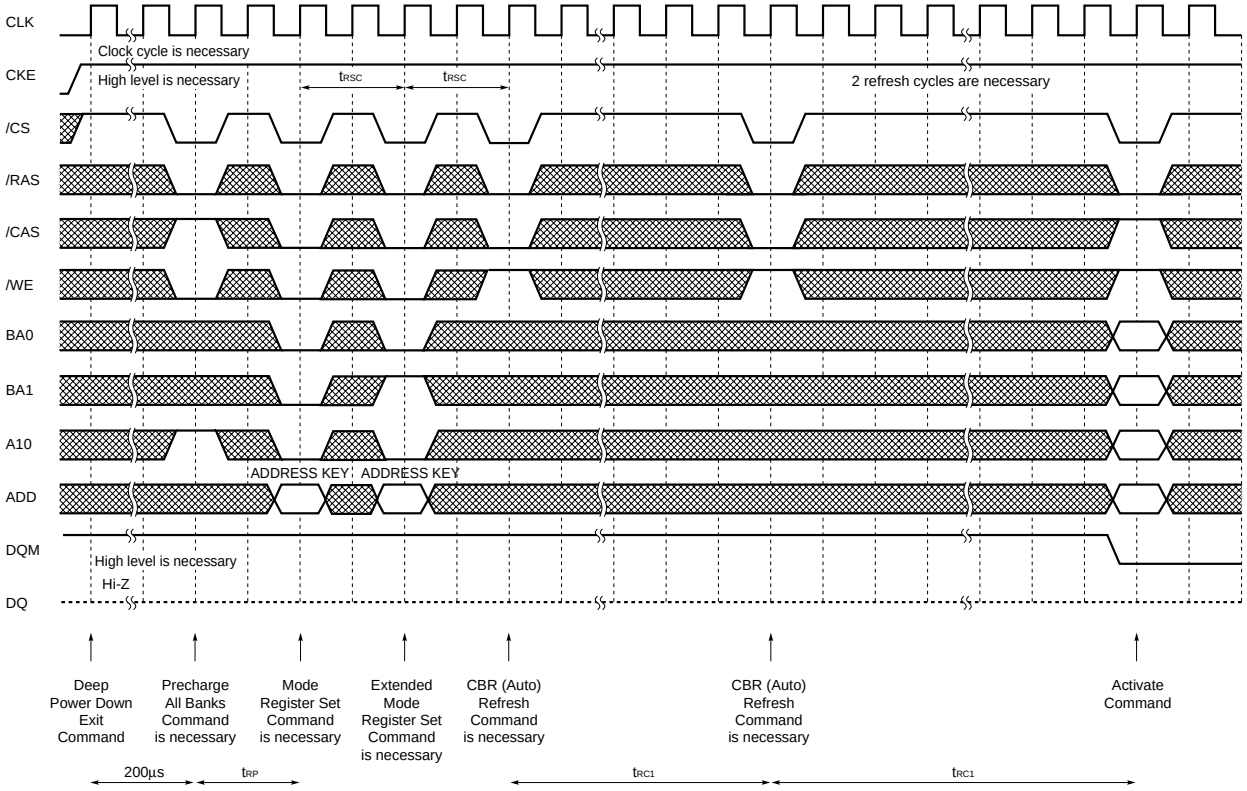
Self Refresh (Entry and Exit)



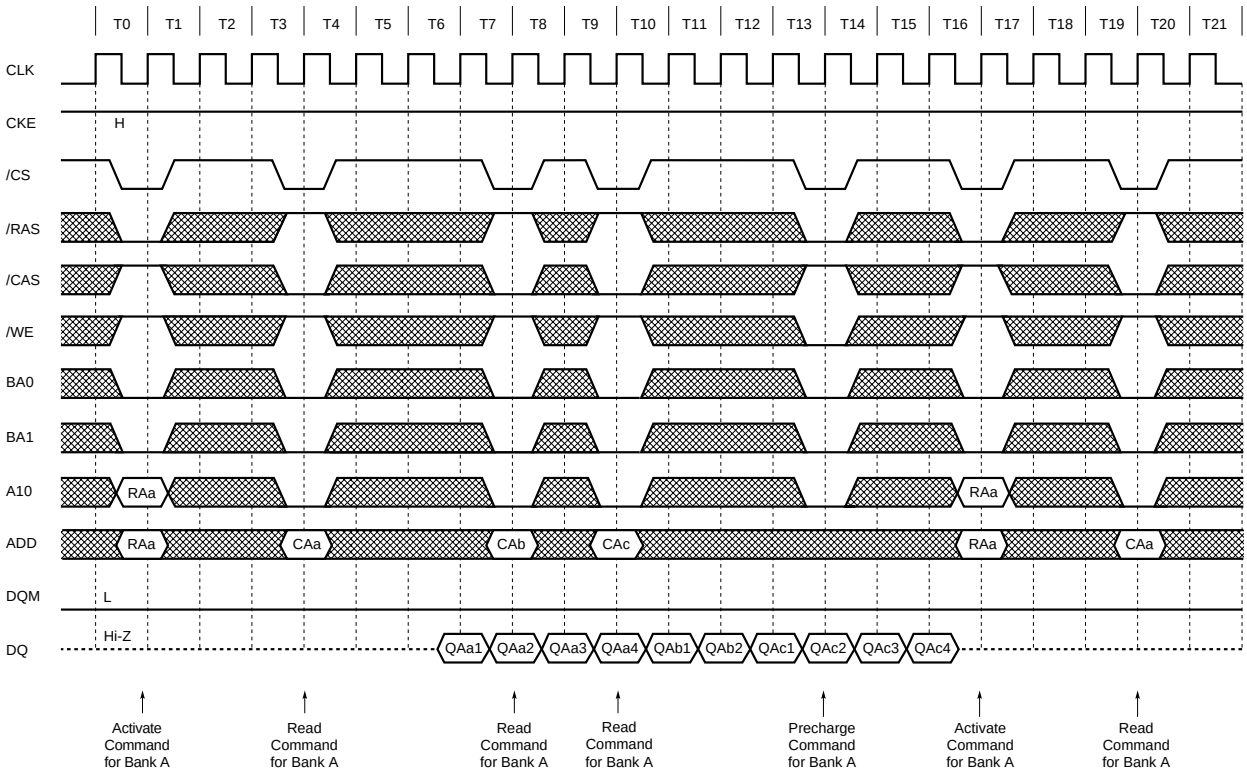
Deep Power Down Entry



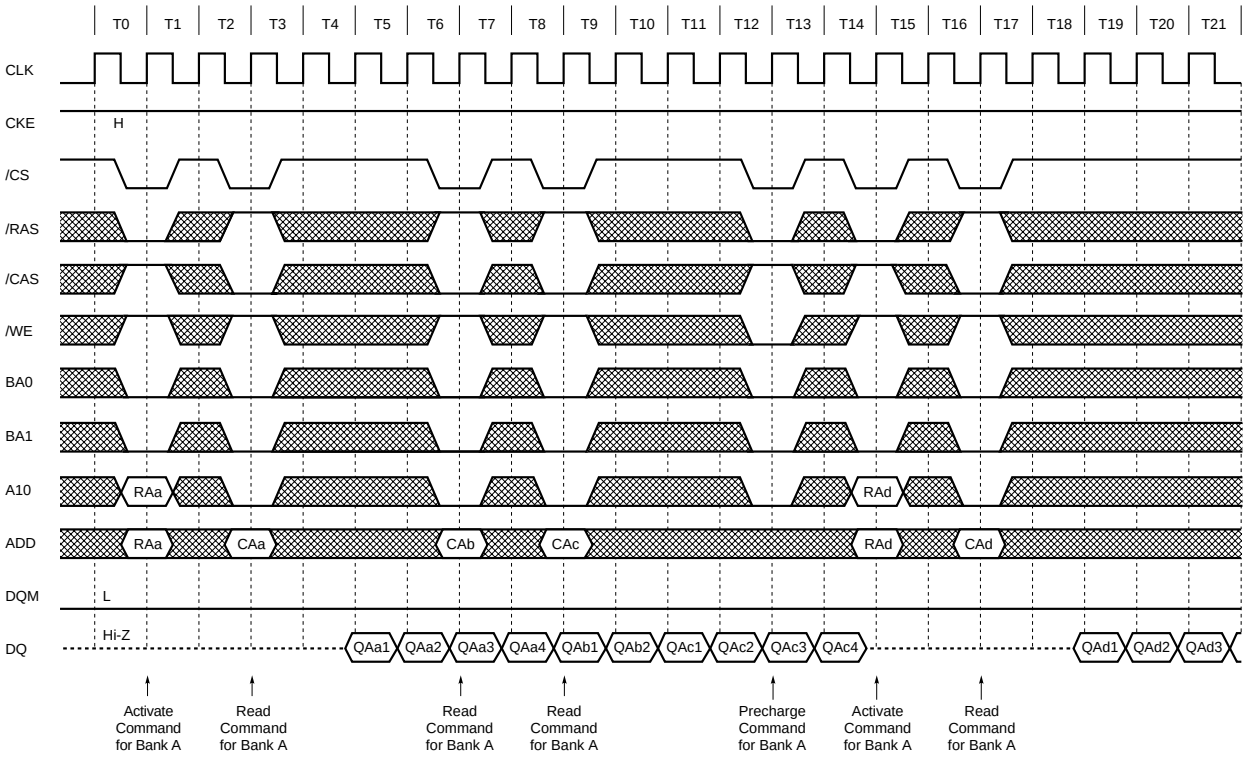
Deep Power Down Exit



Random Column Read

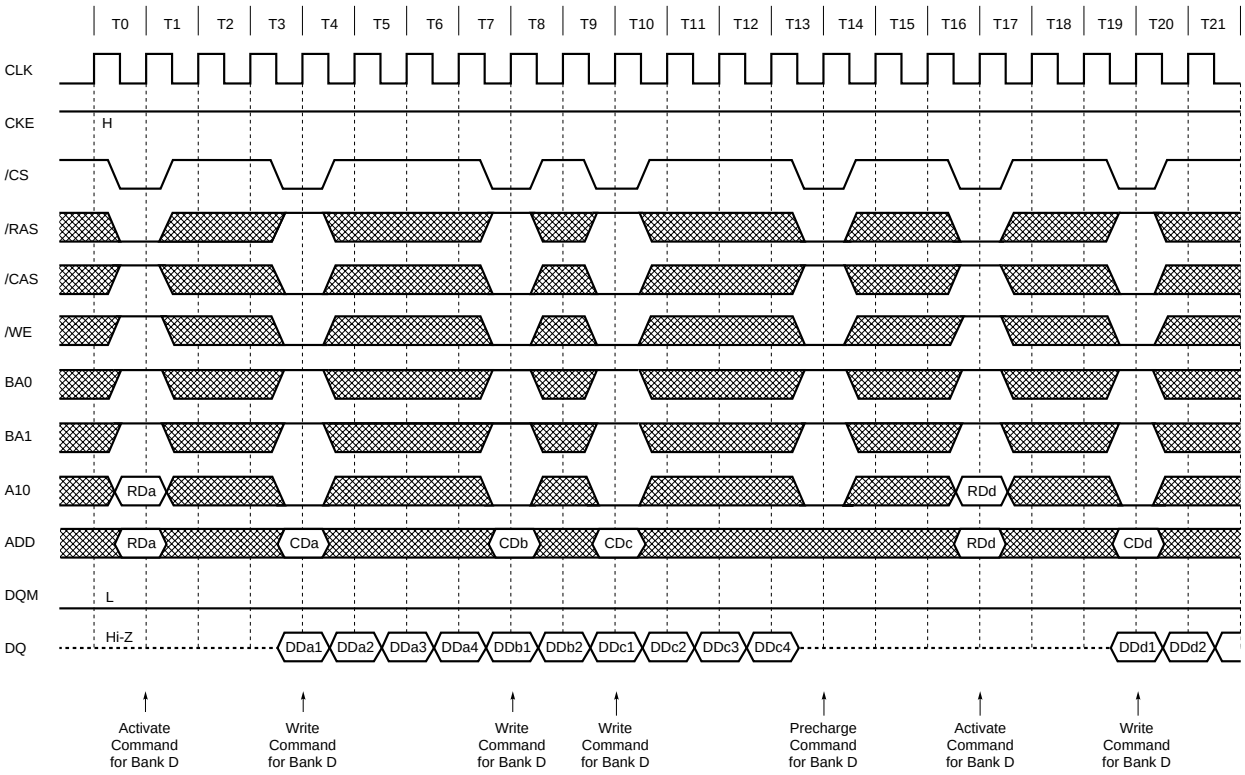


[Burst Length = 4, /CAS Latency = 3]



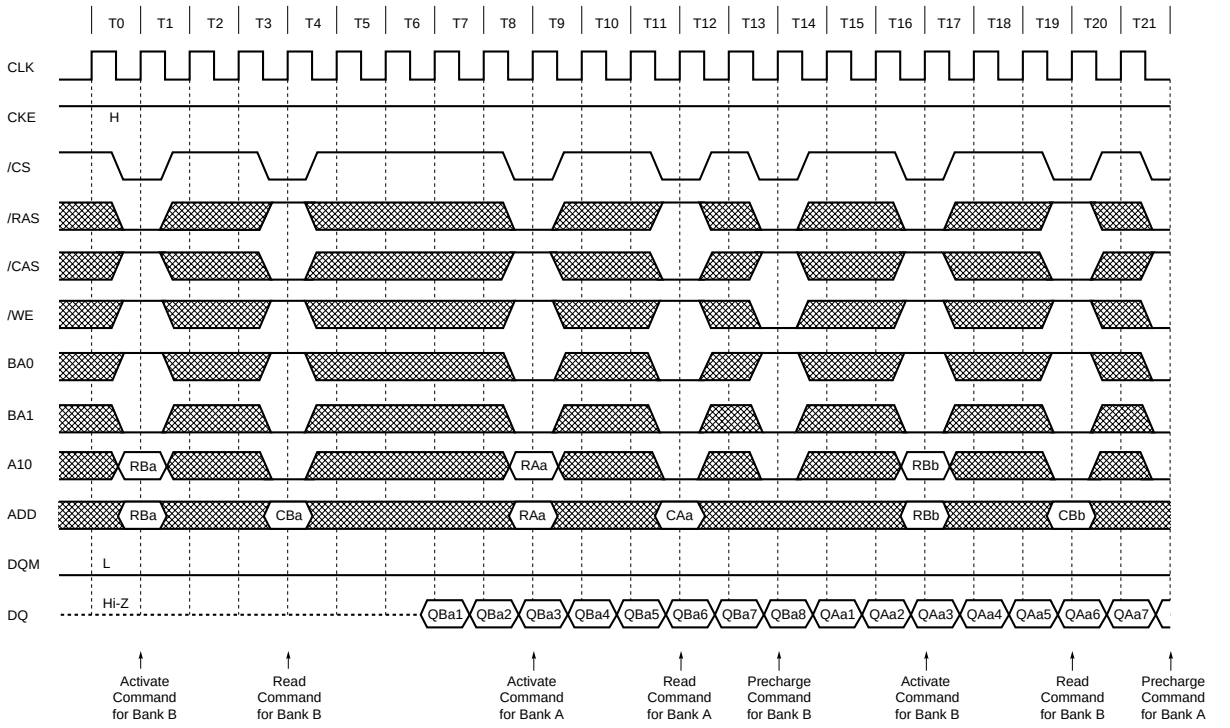
[Burst Length = 4, /CAS Latency = 2]

Random Column Write

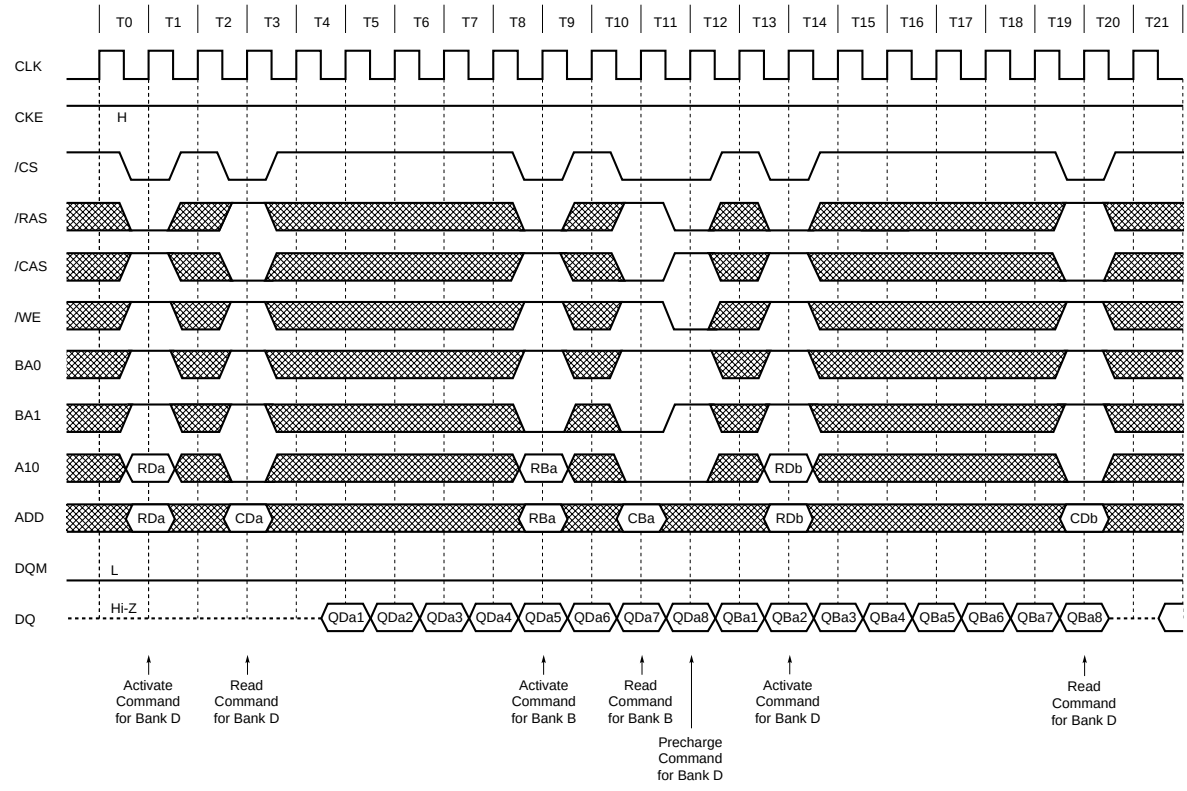


[Burst Length = 4]

Random Row Read

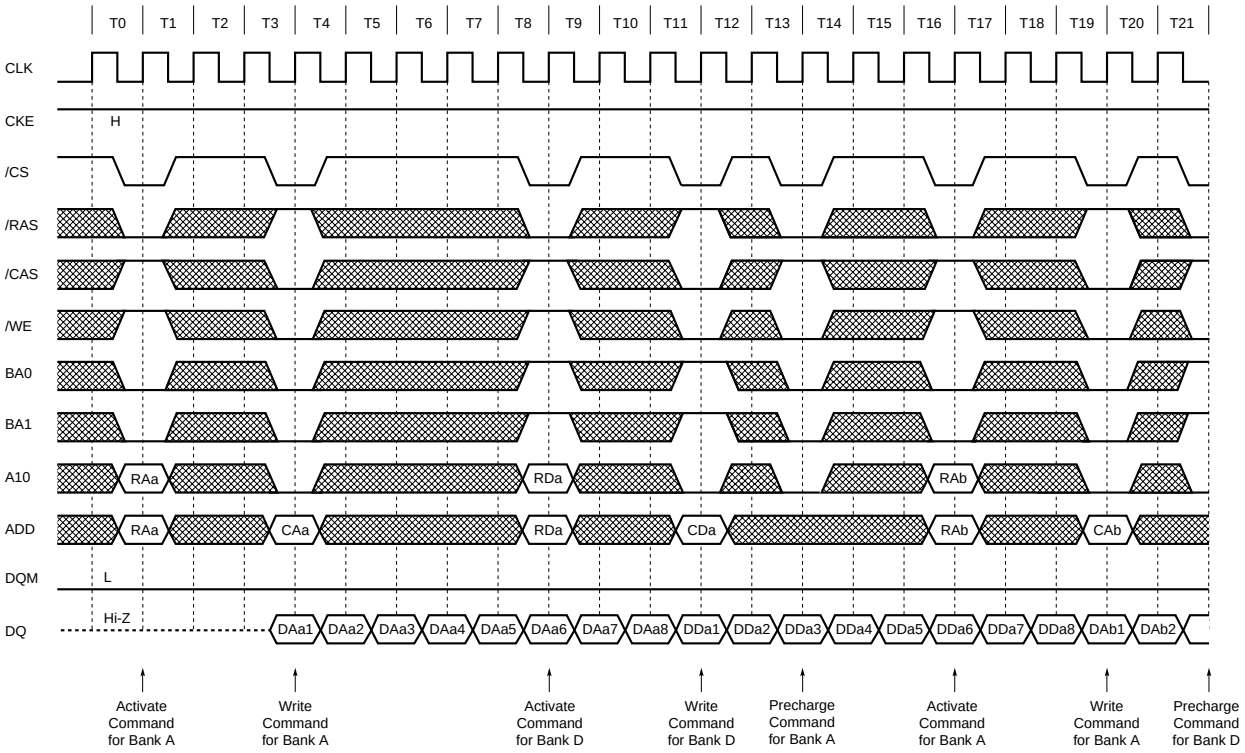


[Burst Length = 8, /CAS Latency = 3]



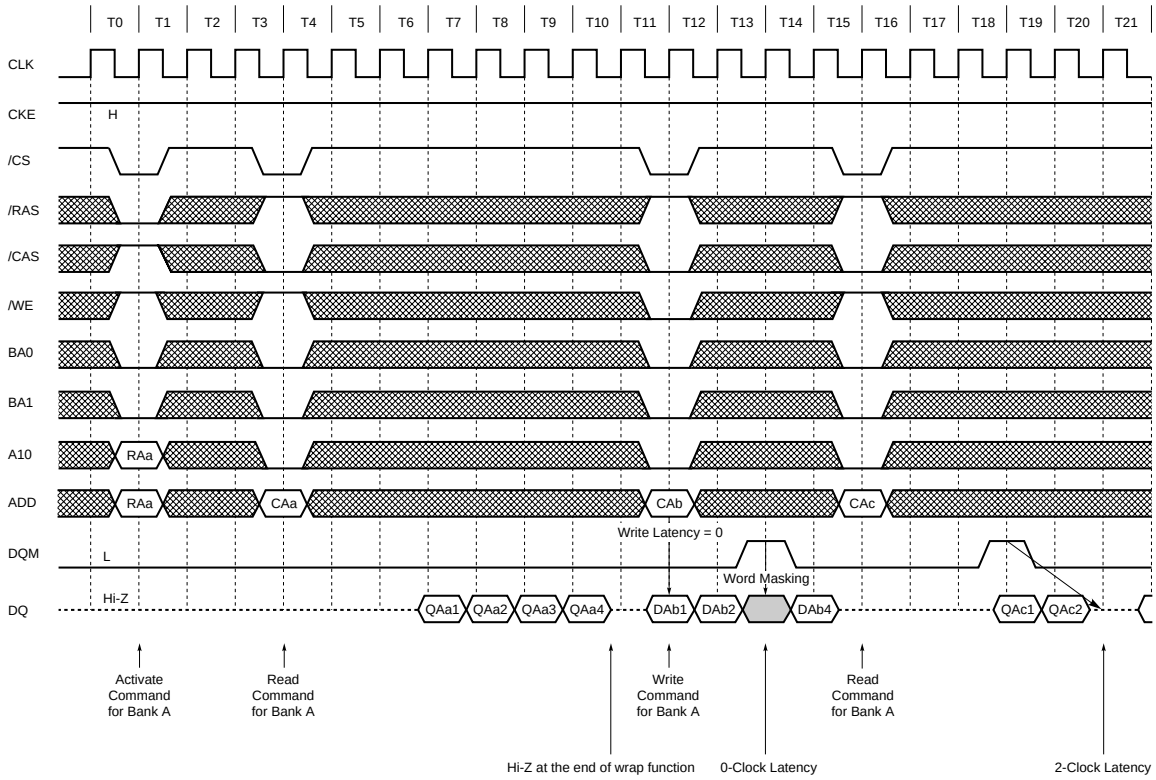
[Burst Length = 8, /CAS Latency = 2]

Random Row Write

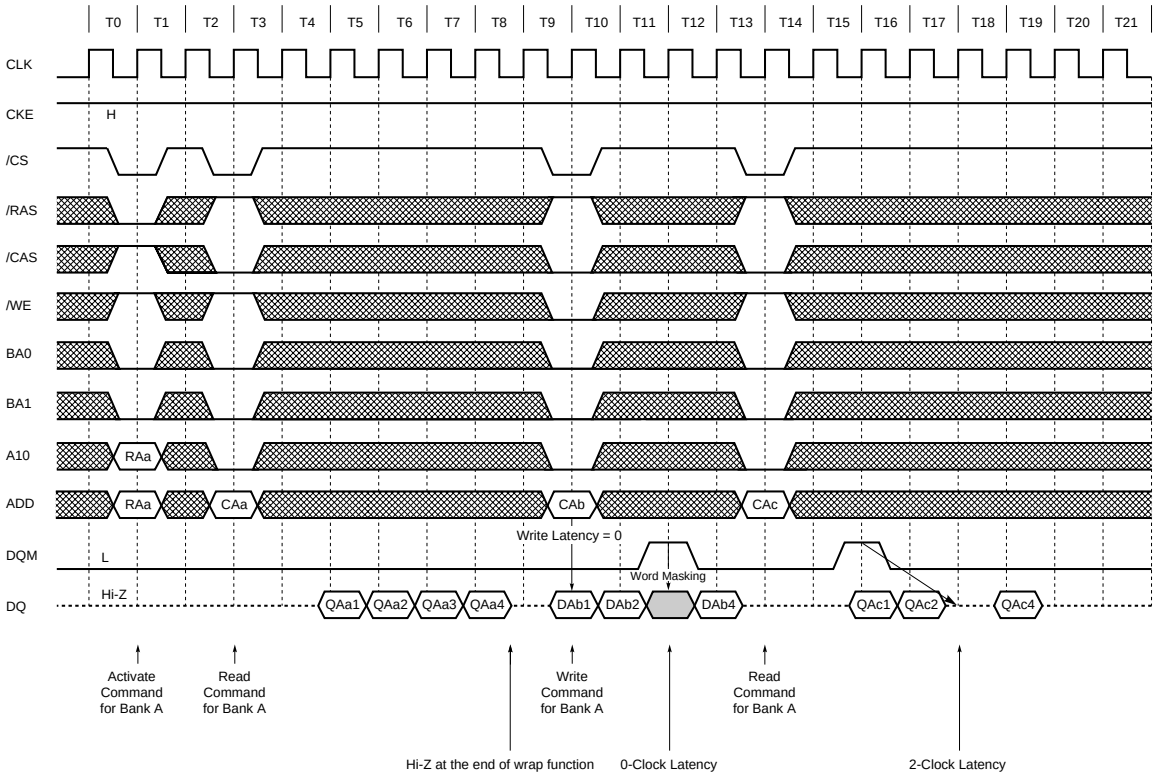


[Burst Length = 8]

Read and Write

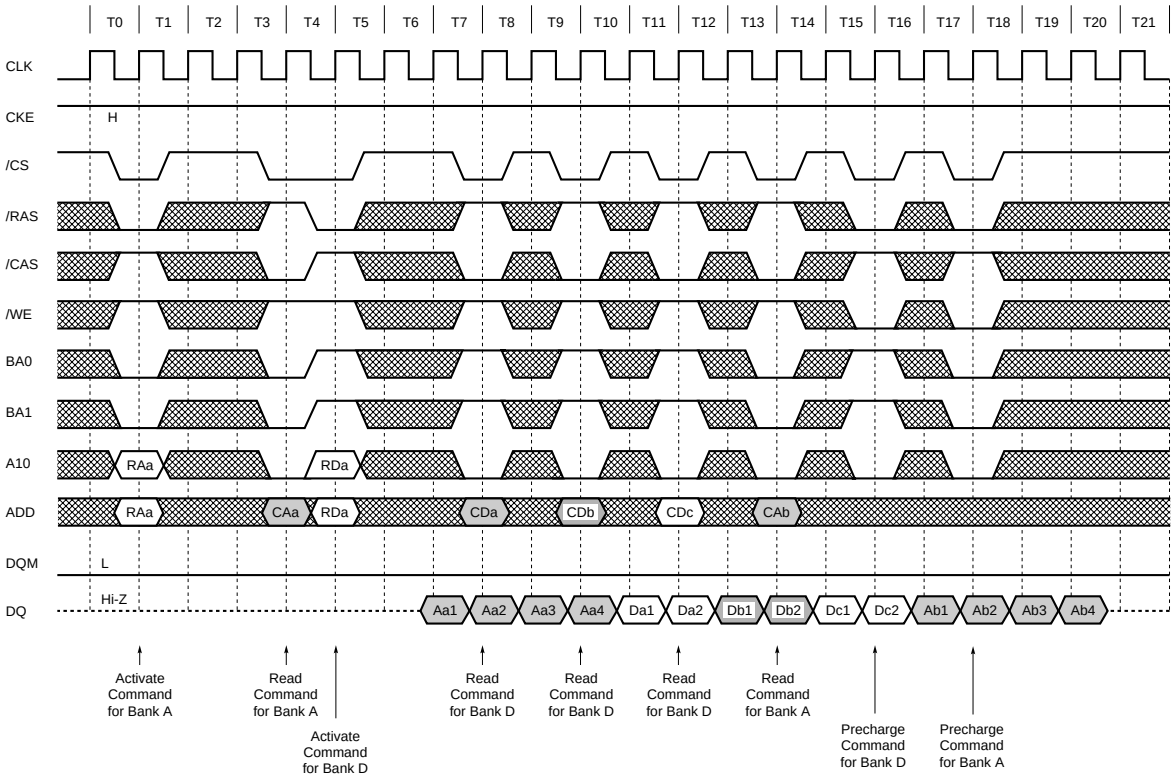


[Burst Length = 4, /CAS Latency = 3]

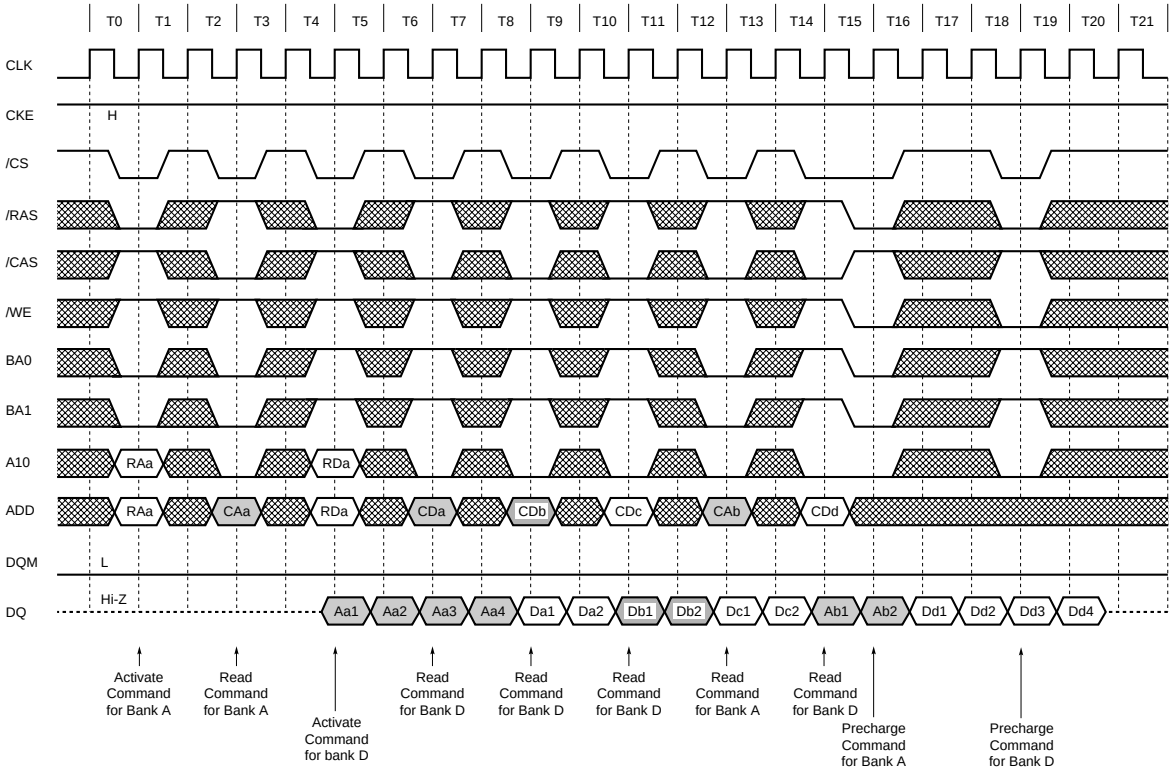


[Burst Length = 4, /CAS Latency = 2]

Interleaved Column Read Cycle

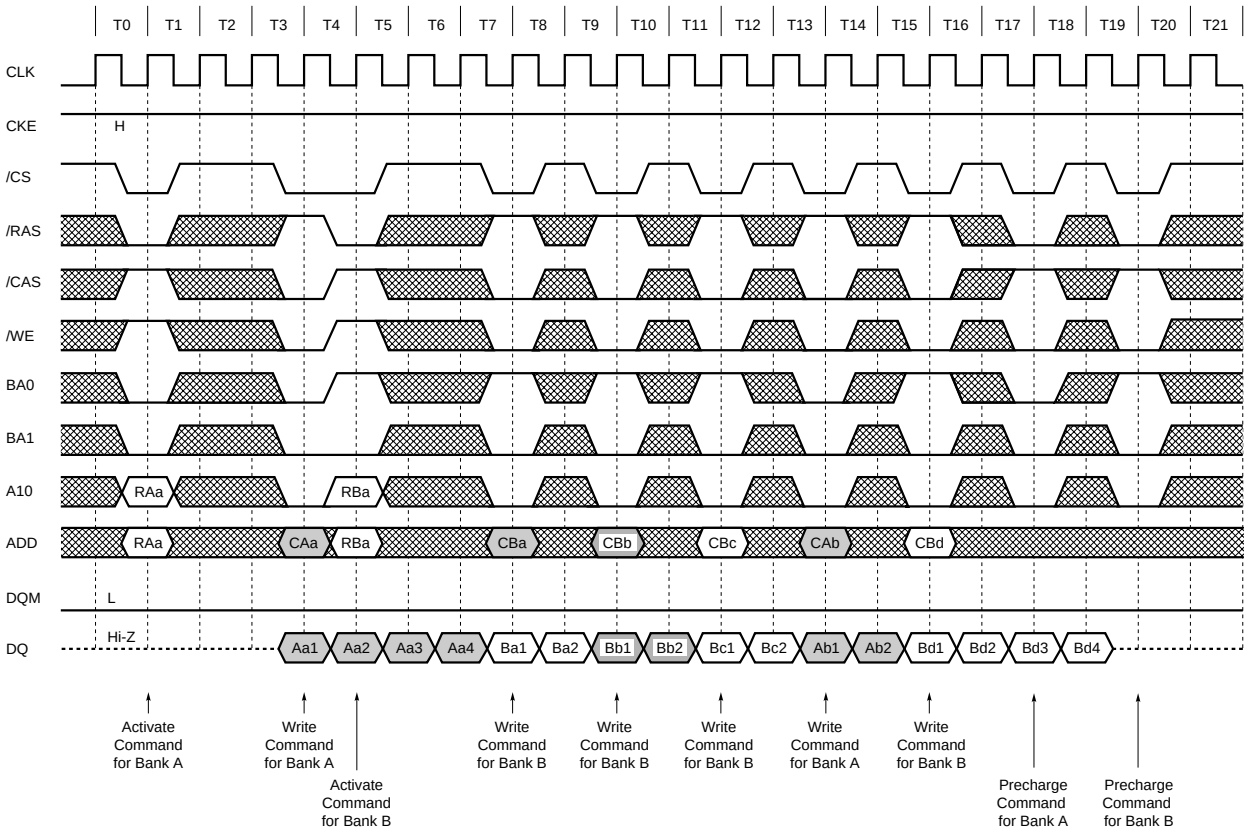


[Burst Length = 4, /CAS Latency = 3]



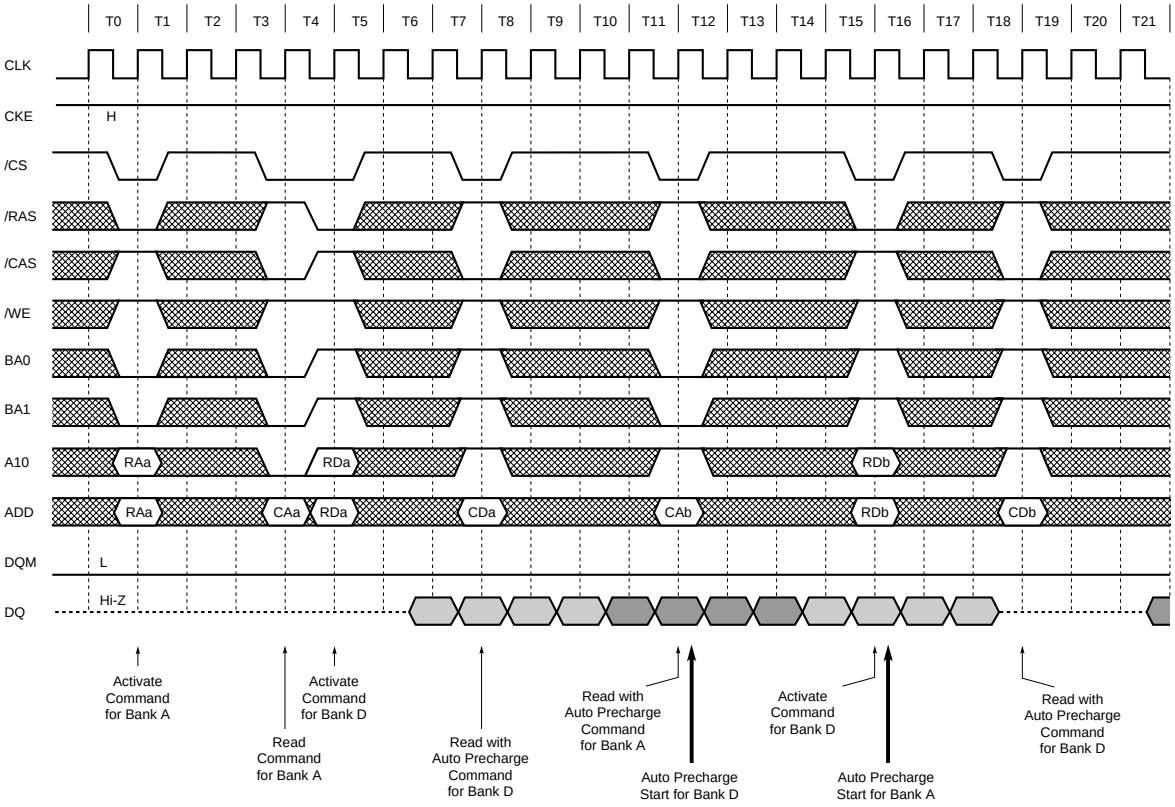
[Burst Length = 4, /CAS Latency = 2]

Interleaved Column Write Cycle

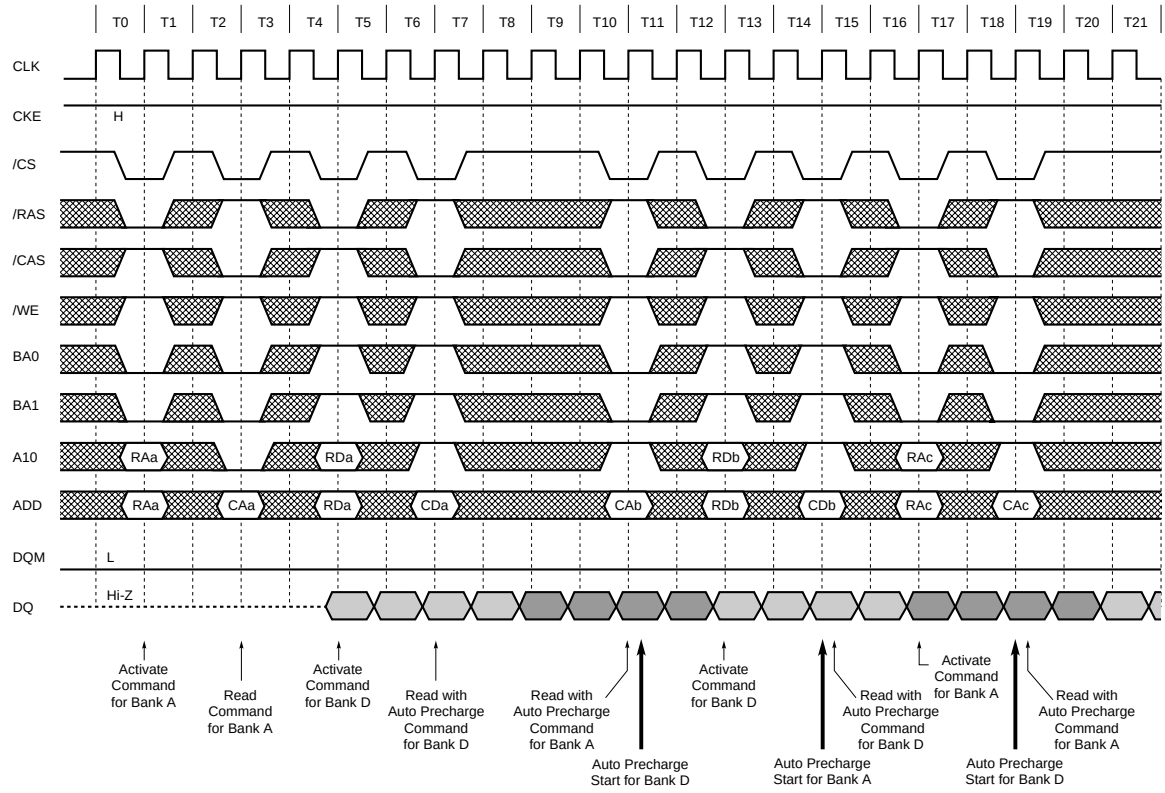


[Burst Length = 4]

Auto Precharge after Read Burst

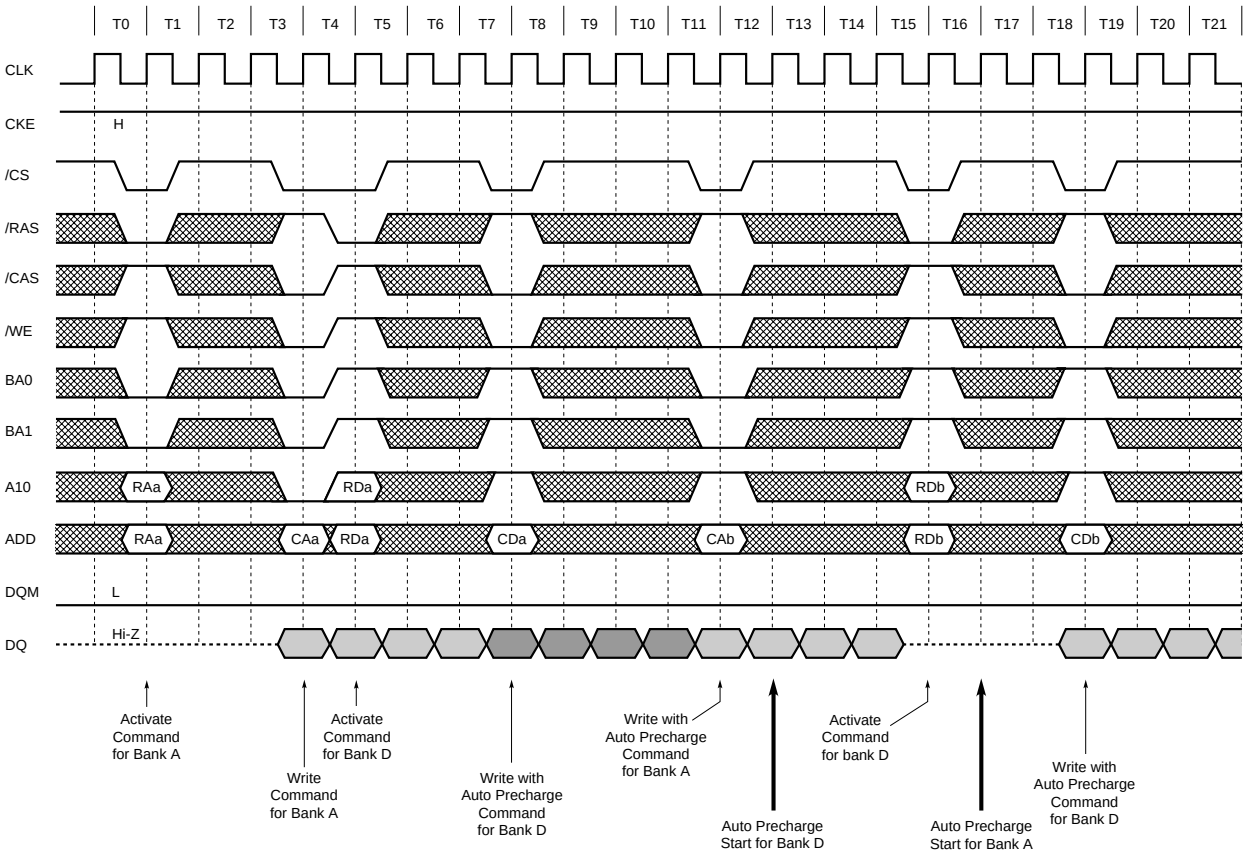


[Burst Length = 4, /CAS Latency = 3]



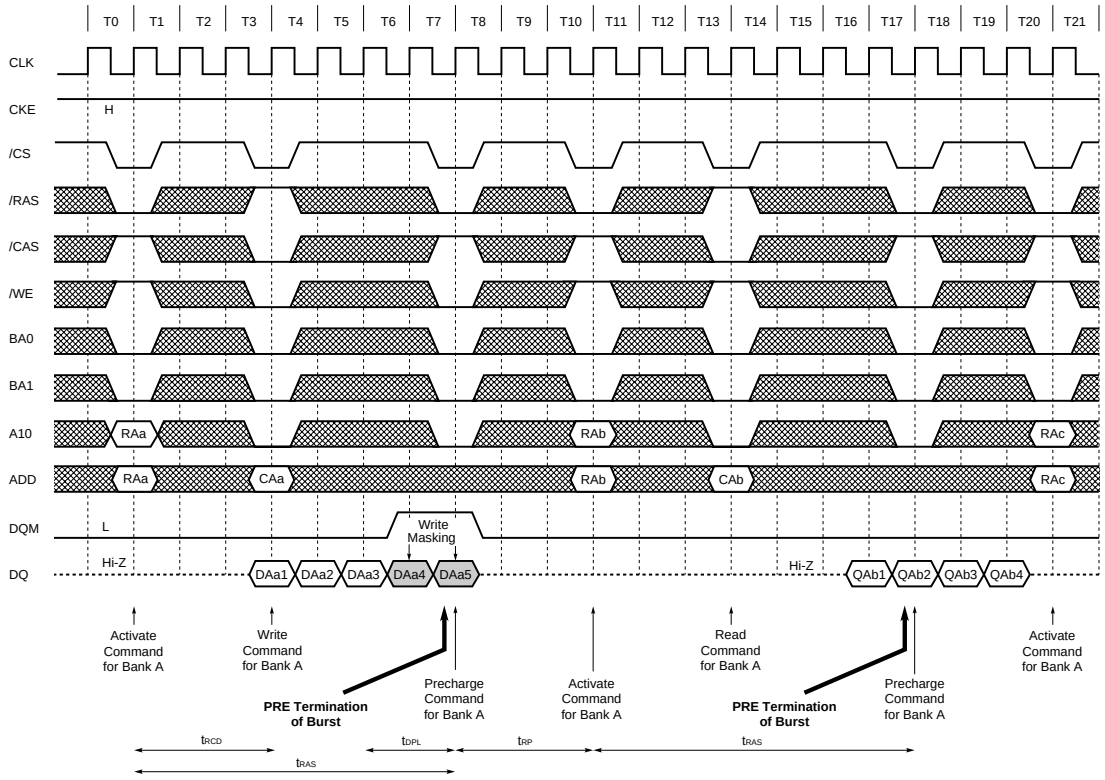
[Burst Length = 4, /CAS Latency = 2]

Auto Precharge after Write Burst

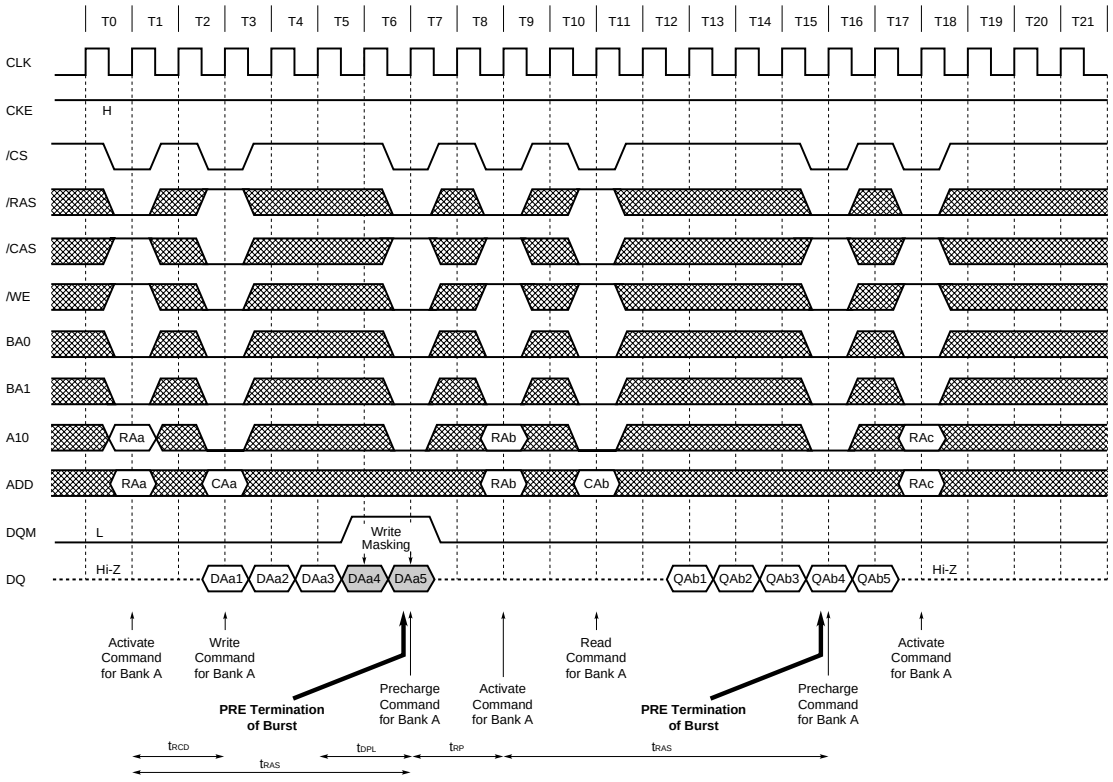


[Burst Length = 4]

Precharge Termination



[Burst Length = 8, /CAS Latency = 3]



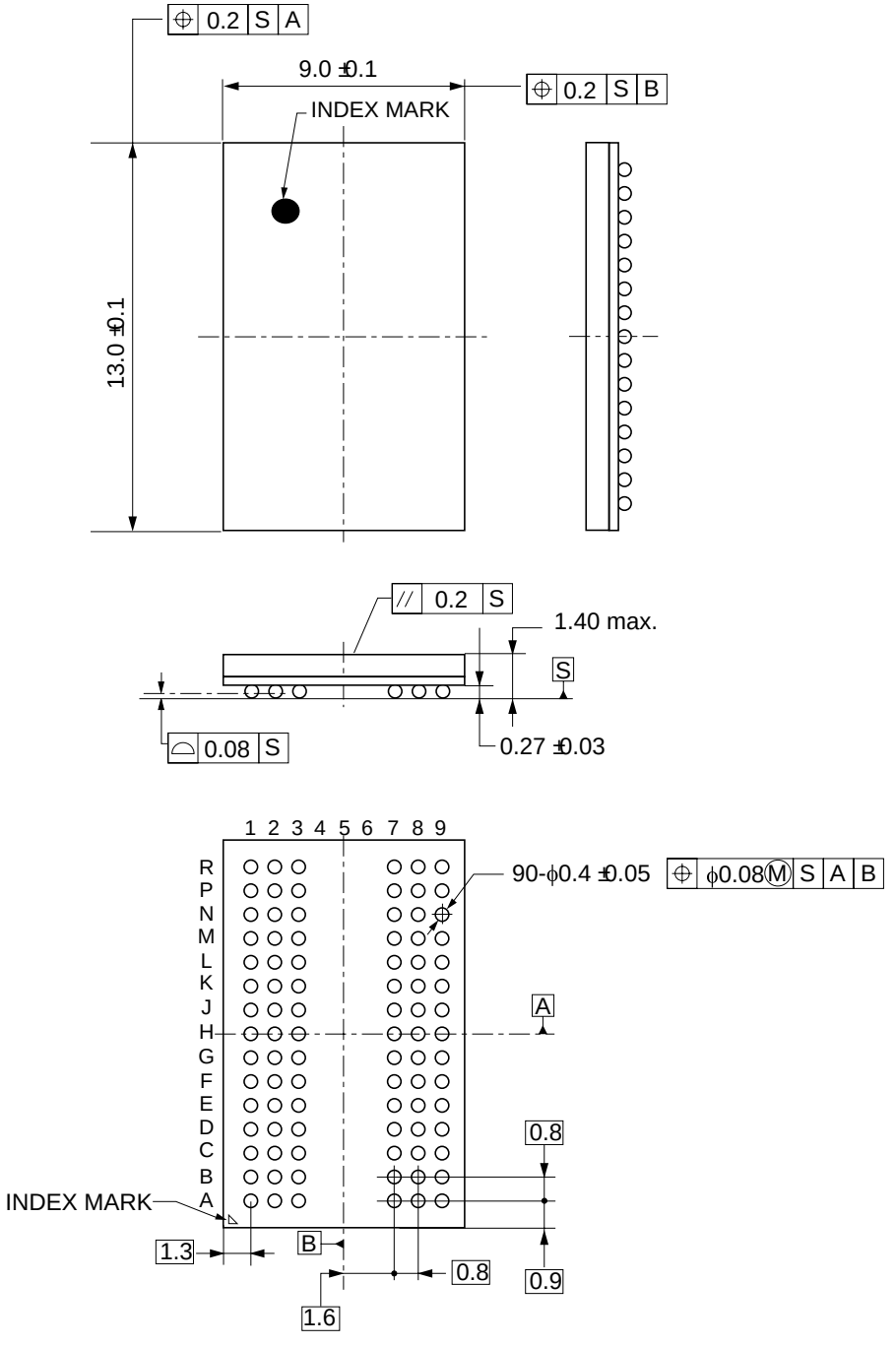
[Burst Length = 8, /CAS Latency = 2]

Package Drawing

90-ball FBGA

Solder ball: Lead free (Sn-Ag-Cu)

Unit: mm



ECA-TS2-0120-01

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the EDL5132CBMA.

Type of Surface Mount Device

EDL5132CBMA: 90-ball FBGA < Lead free (Sn-Ag-Cu) >

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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[Product usage]
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[Usage environment]
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