



1024Kx32 Static RAM CMOS, High Speed Module

FEATURES

- 1024Kx32 bit CMOS Static RAM
 - Access Times: 15, 20, and 25ns
 - Individual Byte Selects
 - Fully Static, No Clocks
 - TTL Compatible I/O
- High Density Package
 - 72 Pin ZIP, No. 175
 - 72 lead SIMM, No. 176 (Angle)
 - 72 lead SIMM, No. 356 (Straight)
 - Common Data Inputs and Outputs
- Single +5V (±10%) Supply Operation

*This product is subject to change without notice.

DESCRIPTION

The EDI8F321024C is a high speed 32 megabit Static RAM module organized as 1024K words by 32 bits. This module is constructed from eight 1024Kx4 Static RAMs in SOJ packages on an epoxy laminate (FR4) board.

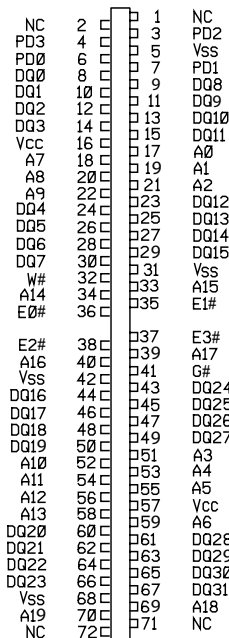
Four chip enables (E0#-E3#) are used to independently enable the four bytes. Reading or writing can be executed on individual bytes or any combination of multiple bytes through proper use of selects.

The EDI8F321024C is offered in 72 pin ZIP and 72 lead SIMM packages, which enable 32 megabits of memory to be placed in less than 1.3 square inches of board space.

All inputs and outputs are TTL compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refreshing for operation and provides equal access and cycle times for ease of use.

Pins PD1- PD4, are used to identify module memory density in applications where alternate modules can be interchanged.

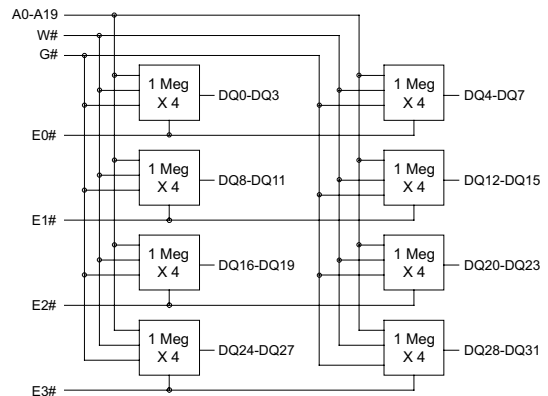
FIG. 1 PIN CONFIGURATIONS AND BLOCK DIAGRAM



PD0 AND PD2 = GROUND
 PD1 AND PD3 = OPEN
 8F321024C Pin Config.

PIN NAMES

A0-A19	Address Inputs
E0#-E3#	Chip Enables
W#	Write Enable
G#	Output Enable
DQ0-DQ31	Common Data Input/Output
Vcc	Power (+5V±10%)
Vss	Ground
NC	No Connection



8F321024C Blk Dia.



ABSOLUTE MAXIMUM RATINGS*

Voltage on any pin relative to V _{SS}	-0.5V to 7.0V
Operating Temperature T _A (Ambient) Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Storage Temperature, Plastic	-55°C to +125°C
Power Dissipation	7.0 Watts
Output Current	20 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Supply Voltage	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	6.0	V
Input Low Voltage	V _{IL}	-0.3	-	0.8	V

AC TEST CONDITIONS

Input Pulse Levels	V _{SS} to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	1TTL, CL = 30pF

(Note: For t_{EHQZ}, t_{GHQZ} and t_{WLQZ}, CL = 5pF)

DC ELECTRICAL CHARACTERISTICS

Parameter	Sym	Conditions	Min	Typ	Max	Units
Operating Power Supply Current	I _{CC1}	W#, E# = V _{IL} , I/I/O = 0mA, Min Cycle			1280	mA
Standby (TTL) Power Supply Current	I _{CC2}	E# ≥ V _{IH} , V _{IN} ≤ V _{IL} or V _{IN} ≥ V _{IH}			480	mA
Full Standby Power Supply Current CMOS	I _{CC3}	E# ≥ V _{CC} -0.2V V _{IN} ≥ V _{CC} -0.2V or V _{IN} ≤ 0.2V			80	mA
Input Leakage Current	I _{LI}	V _{IN} = 0V to V _{CC}	-	-	±80	µA
Output Leakage Current	I _{LO}	V I/O = 0V to V _{CC}	-	-	±20	µA
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8.0mA	-	-	0.4	V

*Typical: T_A = 25°C, V_{CC} = 5.0V

TRUTH TABLE

E#	W#	G#	Mode	Output	Power
H	X	X	Standby	HIGH Z	I _{CC2} /I _{CC3}
L	H	L	Read	D _{OUT}	I _{CC1}
L	L	X	Write	D _{IN}	I _{CC1}
L	H	H	Output Deselect	HIGH Z	I _{CC1}

CAPACITANCE

(f=1.0MHz, V_{IN}=V_{CC} or V_{SS})

Parameter	Sym	Max	Unit
Address Lines	CI	60	pF
Data Lines	CD/Q	20	pF
Chip Enable Line	CC	20	pF
Write Line	CN	60	pF

These parameters are sampled, not 100% tested.



AC CHARACTERISTICS READ CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	15		20		25		ns
Address Access Time	t _{AVQV}	t _{AA}		15		20		25	ns
Chip Enable Access	t _{ELQV}	t _{ACS}		15		20		25	ns
Chip Enable to Output in Low Z (1)	t _{ELQX}	t _{CLZ}	3		3		3		ns
Chip Disable to Output in High Z (1)	t _{EHQZ}	t _{CHZ}		7		10		12	ns
Output Hold from Address Change	t _{AVQX}	t _{OH}	3		3		3		ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		7		8		10	ns
Output Enable to Output in Low Z (1)	t _{GLQX}	t _{OLZ}	0		0		0		ns
Output Disable to Output in High Z(1)	t _{GHQZ}	t _{OHZ}		7		8		10	ns

Note 1: Parameter guaranteed, but not tested.

FIG. READ CYCLE 1 - W# HIGH, G#, E# LOW

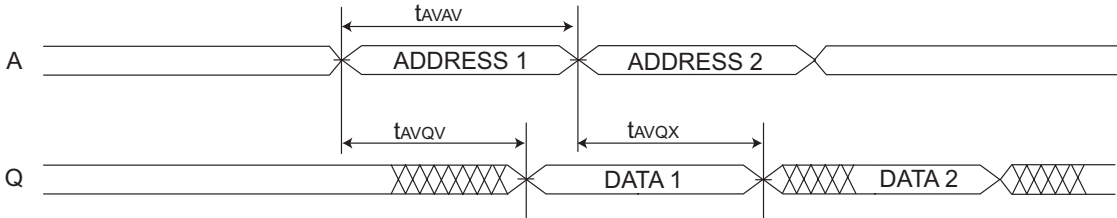
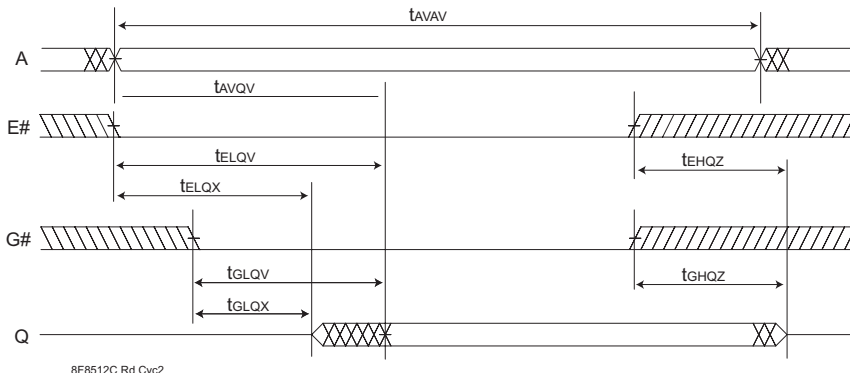


FIG. 3 READ CYCLE 2 - W# HIGH



8F8512C Rd Cyc2

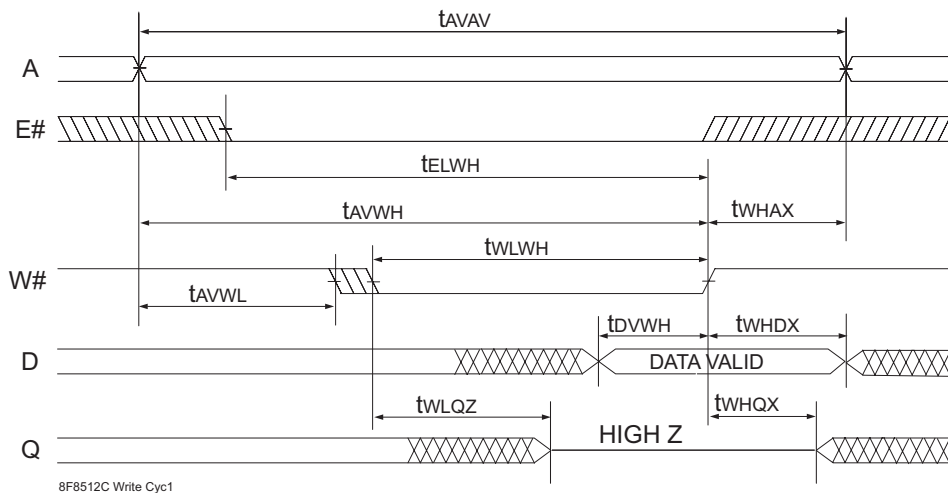


AC CHARACTERISTICS WRITE CYCLE

Parameter	Symbol		15ns		20ns		25ns		Units
	JEDEC	Alt.	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	15		20		25		ns
Chip Enable to End of Write	t _{ELWH}	t _{EW}	10		15		20		ns
	t _{WLEH}	t _{EW}	10		15		20		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
	t _{AVEL}	t _{AS}	0		0		0		ns
Address Valid to End of Write	t _{AVWH}	t _{AW}	10		15		20		ns
	t _{AVEH}	t _{AW}	10		15		20		ns
Write Pulse Width	t _{WLWH}	t _{WP}	12		15		20		ns
	t _{WLEH}	t _{WP}	12		15		20		ns
Write Recovery Time	t _{WHAX}	t _{WR}	0		0		0		ns
	t _{EHAX}	t _{WR}	0		0		0		ns
Data Hold Time	t _{WHDX}	t _{DH}	3		3		0		ns
	t _{EHDX}	t _{DH}	3		3		0		ns
Write to Output in High Z (1)	t _{WLQZ}	t _{WHZ}	0	7	0	8	0	12	ns
Data to Write Time	t _{DVWH}	t _{DW}	7		12		15		ns
	t _{DVEH}	t _{DW}	7		12		15		ns
Output Active from End of Write (1)	t _{WHQX}	t _{WLZ}	3		3		3		ns

Note 1: Parameter guaranteed, but not tested.

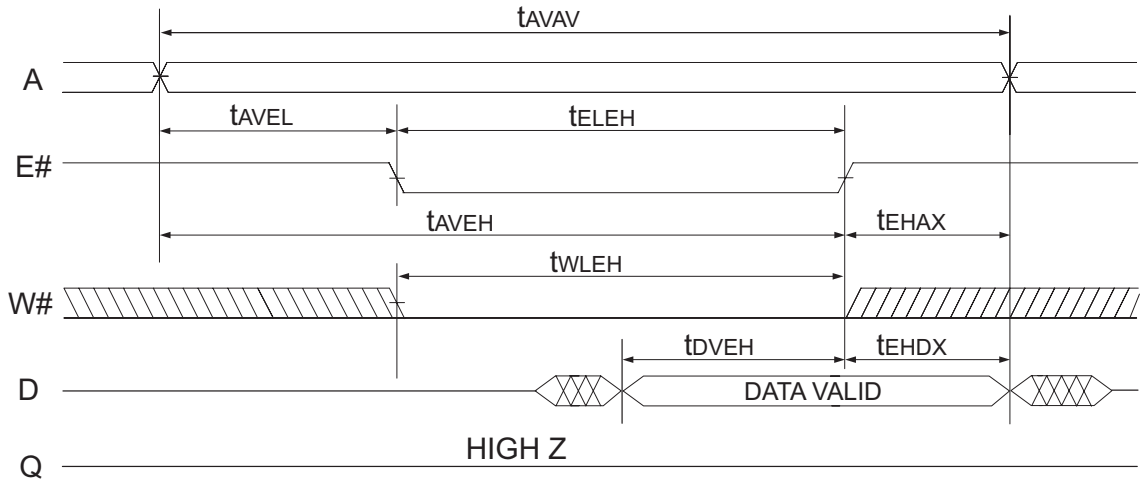
FIG. 4
WRITE CYCLE 1 - W# CONTROLLED



8F8512C Write Cyc1



FIG. 5
WRITE CYCLE 2 - E# CONTROLLED



8F8512C Write Cyc2



ORDERING INFORMATION

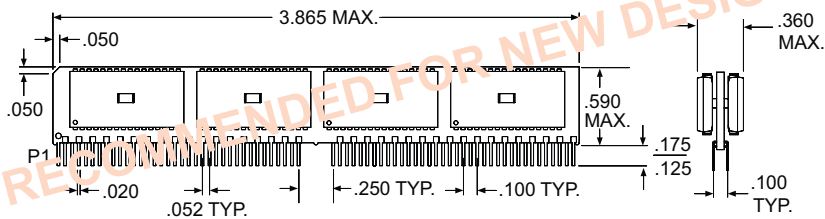
Part Number	Speed (ns)	Package No.
EDI8F321024C15MNC	15	176
EDI8F321024C20MNC	20	176
EDI8F321024C25MNC	25	176

Note: To order gold SIMM option, change "EDIF" to "EDIG".

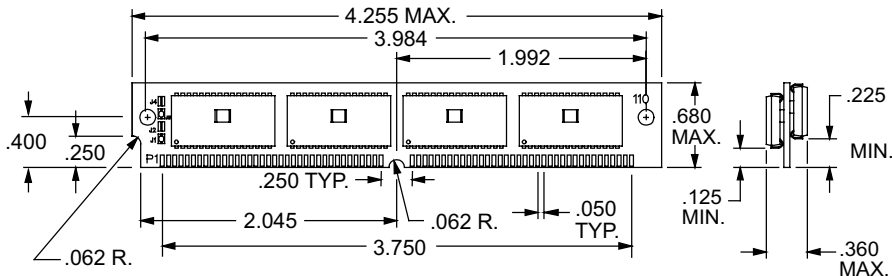
Part Number	Speed (ns)	Package No.
EDI8F321024C15MZC	15	175
EDI8F321024C20MZC	20	175
EDI8F321024C25MZC	25	175
EDI8F321024C15MMC	15	356
EDI8F321024C20MMC	20	356
EDI8F321024C25MMC	25	356

PACKAGE DESCRIPTIONS

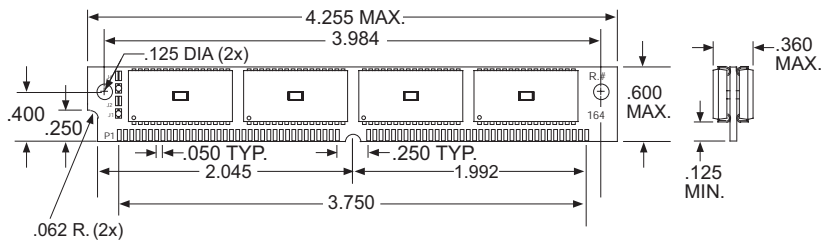
PACKAGE NO.175: 72 PIN ZIP



PACKAGE NO. 176: 72 LEAD ANGLED SIMM



PACKAGE NO. 356: 72 PIN SIMM



ALL DIMENSIONS ARE IN INCHES