Design Idea DI-56
DPA-Switch™
19.2 W DC-DC Converter

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
Telecom	DPA425R	19.2 W	36-75 VDC	±12 V	Flyback

Design Highlights

- Low cost 400 kHz flyback design
- ±12 V outputs at ±5% accuracy
- Highly efficient diode rectification design - 80% at 48 V
- Low component count
- Accurate line OV and UV protection
- Thermal, short circuit and output overload protection
- No current sense components

Operation

DPA-Switch greatly simplifies the design compared to a discrete implementation. Resistor R1 programs the under/over voltages and linearly reduces the maximum duty cycle with input voltage to prevent core saturation during load transients. Resistor R3 programs the *DPA-Switch* current limit at 77% of nominal to minimize fault and overload power. Drain voltage clamping is provided by Zener diode VR1.

Output regulation is taken from the +12 V output. The -12 V output is magnetically coupled. Shared regulation of +12 V and -12 V may be used if better cross-regulation is required between the two outputs. Optional resistor R7, diode D3 and capacitor C16 implement a soft-finish network to slow the rise of the output voltage at start-up, preventing overshoot.

The bias winding provides operating power to the *DPA-Switch*. The regulation is fed back from the secondary through the opto-transistor of U2. The *DPA-Switch* will go into auto-restart in the event of optocoupler (U2) failure, or output short circuit. The optional resistor R5 and Zener diode VR2 provide a fail-safe output regulation path, limiting the instantaneous output overvoltage in the event of U2 failure.

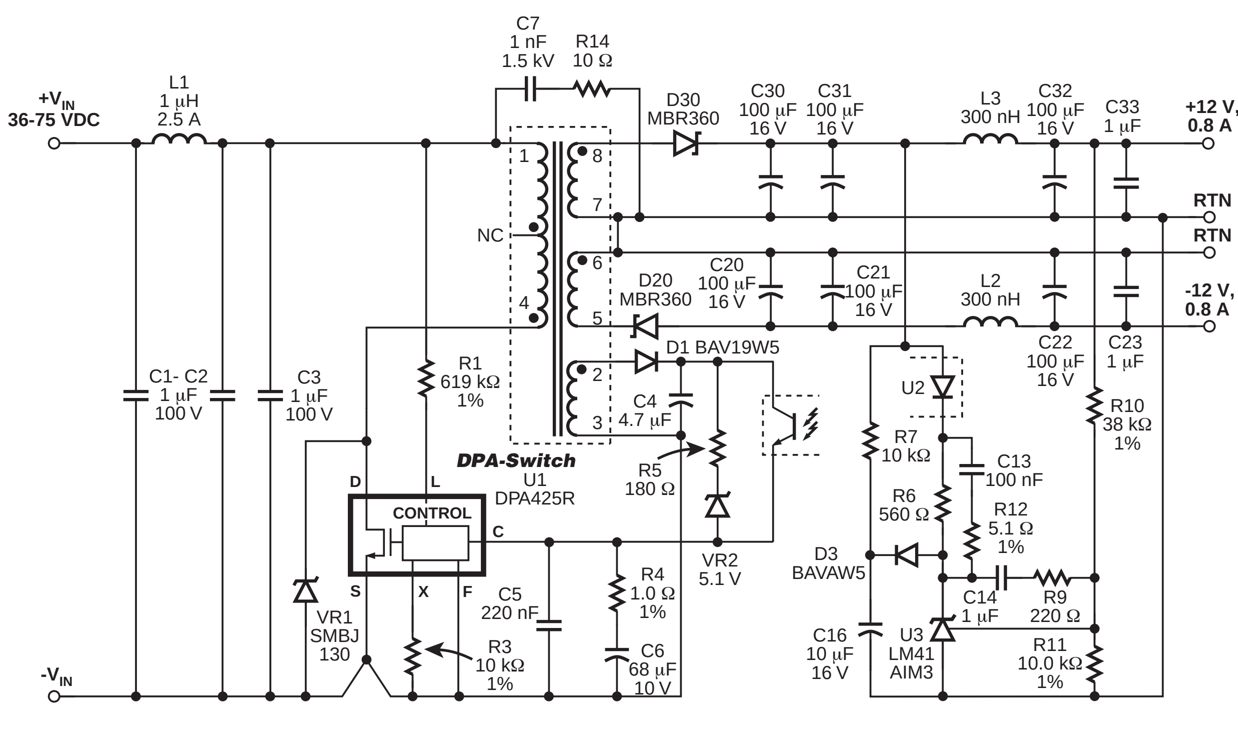

Figure 1. DPA425R - 19.2 W, ±12 V, 0.8 A, DC-DC Converter.

Key Design Points

- For the nominal under-voltage set point V_{UV}:
  $R1 = (V_{UV} – 2.35) / 50\ \mu A$
  $V_{OV} = (R1 \times 135\ \mu A) + 2.5\ V$
- For highest efficiency designs: use continuous conduction mode operation designed at approximately 0.4 KRP; minimize turns in the transformer and at this (19 W) power level keep AC flux density (BM) <1500 Gauss; fully fill a single layer for each winding to minimize leakage inductance and maximize copper fill factor; if possible use Schottky rectifying diodes (D20 and D30) with a low-forward drop.
- The transformer primary is split in order to minimize leakage inductance and thus obtain better cross-regulation. Note: minimizing primary leakage inductance will improve output cross-regulation at load extremes.
- The -12 V output is not directly sensed as part of the regulation loop. Cross-regulation may be improved by adding a second sense resistor to work in conjunction with R10. Both resistors R10 and the second sense resistor would be changed to 76 kΩ each.
- Set resonant frequency of post-filter (L2, C22 or L3, C32) beyond crossover frequency (typically 5% to 10% of switching frequency).
- Good layout practices
  - For length of +12 V secondary current loop from transformer pin 8, diode D30 and capacitors C30, C31 and back to pin 7 of the transformer: ensure identical path length for C30 and C31 to guarantee they equally share the ripple current.
  - The same is also true for the layout of the -12 V output.
- Choosing a larger *DPA-Switch* will increase efficiency at low and medium input voltages.

TRANSFORMER PARAMETERS	
Core Material	Epcos P/N: P 14x8 N87, ungapped
Bobbin	8-pin P 14x8 surface mount bobbin
Winding Details	Primary 7T + 7T, 2 x 29 AWG Bias 5T, 1 x 36 AWG +12 V 5T, 2 x 29 AWG -12 V 5T, 2 x 29 AWG
Winding Order & Pin Numbers	Primary-1 (4-NC), -12 V (6-5), Bias (2-3), +12 V (8-7), Primary-2 (NC-1)
Primary Inductance	22 µH ±25% (at 400 kHz)
Primary Resonant Frequency	3.8 MHz (minimum)
Leakage Inductance	0.75 µH (maximum)

Table 1. Transformer Design Parameters.

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