Design Idea DI-134



PeakSwitch[®] Audio Amplifier Power Supply

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
Audio	PKS606P	20 W, 43 W peak	90-265 VAC	12 V	Flyback

Design Highlights

- Delivers >2X peak power without output distortion
- Universal input voltage range operation allows a single design to be sold worldwide
- High efficiency (>79%) across entire input range
- Meets EN55022 B conducted EMI limits
- Auto-restart feature allows indefinitely shorted output
- Thermal shutdown protects supply and amplifier

Operation

The isolated flyback converter shown in Figure 1 was designed around a member of the PeakSwitch IC family, the PKS606P (U1). A device in the P package (8-pin DIP) was selected to minimize the cost and size of the heatsink required for peak power delivery.

The input circuitry consists of a fuse (F1) and EMI filter components (R6, C9, L8, L4, C12, R9, R8 and C13). The AC input is rectified (D1–D4) and filtered (C2) and connected across the primary side power components (T1 and U1).

During the flyback portion of each switching cycle, an RCD-Zener clamp circuit (L2, D5, R7, C11 and VR1) protects the MOSFET integrated within U1. Ferrite bead L2, and RC

snubber R7 and C11 reduce EMI by damping high-frequency ringing. Capacitor C4 decouples the BYPASS (BP) pin of U1, which is the IC's internally regulated supply node. An integrated, high-voltage current source provides initial operating power to U1. A bias winding on T1 (pins 4 and 5), D6, C5 and R3 provide operating current to U1, after initial startup. Output voltage feedback is coupled across the safety isolation barrier by U2. Transistor Q1, C19, R14 and D9 prevent the high-frequency gain loss that the U2 phototransistor normally experiences, which prevents groups of enabled and disabled switching cycles (pulse bunching). Using the signal on the EN/UV pin, the controller within U1 regulates the output voltage by enabling and disabling MOSFET switching cycles.

On the secondary side of the isolation barrier, D7 rectifies the output of T1 and charges C7 and C16. The snubber circuit (R5 and C10) across D7 attenuates the high frequency ring that occurs when D7 turns off.

Output voltage feedback is derived from two separate circuits. The circuit formed by VR2, the LED in U2, C19 and R16 provides the high frequency (HF) portion of the feedback



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signal. The circuit formed by R10, U3 and its associated components provides the low frequency (LF) portion of the feedback signal and determines the DC regulation set point.

The HF circuit gives the supply good transient load responsiveness. The LF circuit gives the supply good output voltage accuracy. Both circuits work by forward biasing the LED in U2 whenever the output voltage exceeds the set point value. The series voltage drops across VR2, the U2 LED and R16 determine the set point for the HF circuit. The voltage divider (R12 and R13) and U3 determine the set point for the LF circuit. Capacitor C17 is physically located near the HF circuit, and attenuates noise that could falsely trigger its set point threshold. Zener diode VR3 clamps the output voltage at 16 V, if the feedback loop becomes an open circuit, until auto-restart activates (occurs after no cycles have been skipped for 30 ms).

Key Design Points

• The values for R11 and R16 were chosen so that the voltage on the cathode of the LED in U2 is about 2.2 V.

TRANSFORMER PARAMETERS		
Core Material	EE25 NC-2H or Equivalent, gapped for A_{LG} of 105 nH/t ²	
Bobbin	EE25, 10 pin	
Winding Details	1/2 Primary: 26T, 27 AWG, 1 layer, tape Bias: 8T X2, 29 AWG, tape Secondary: 6T, X4, 23 AWG TIW, 2 layers Shield: 7T X4, 29 AWG, tape 1/2 Primary: 26T, 27 AWG, 1 layer	
Primary Inductance	370 μH ±12%	
Primary Resonant Frequency	180 kHz (minimum)	
Leakage Inductance	8 μH (maximum)	

- The core size and the winding wire diameter sizes were chosen based on the average of the peak and the continuous output power.
- The number of turns in the primary and secondary windings and the primary inductance values were chosen based on the peak output power.
- Diode D5 must be an ultrafast diode with a reverse recovery time of <75 ns.



Output Current (A)

Figure 2. Efficiency vs. Load, at Standard Line Voltages.



Figure 3. Worst Case Conducted EMI (230 VAC).

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Table 2. Transformer Parameters.