PROCESS CP311

Power Transistor

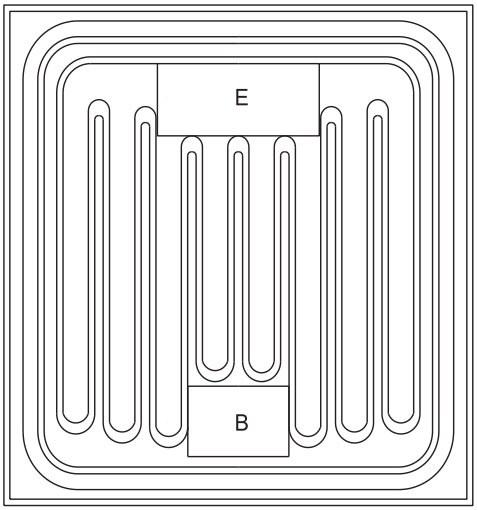
NPN High Voltage Transistor Chip

Central™ Semiconductor Corp.

PROCESS DETAILS

Process	EPITAXIAL PLANAR
Die Size	109.5 x 109.5 MILS
Die Thickness	9.0 MILS
Base Bonding Pad Area	23.6 x 15.4 MILS
Emitter Bonding Pad Area	37.8 x 15.8 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Ti / Ni / Ag - 11,300Å

GEOMETRY



BACKSIDE COLLECTOR R0

GROSS DIE PER 4 INCH WAFER

900

PRINCIPAL DEVICE TYPES

CJDD3110

145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

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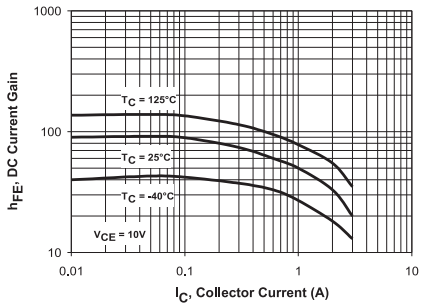
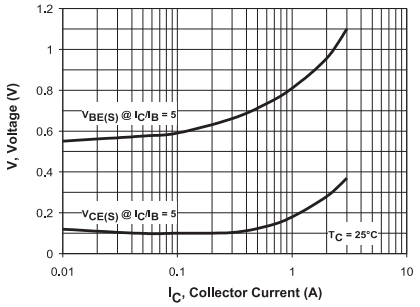
Typical Electrical Characteristics

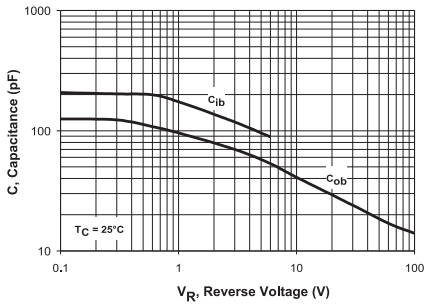
DC Current Gain



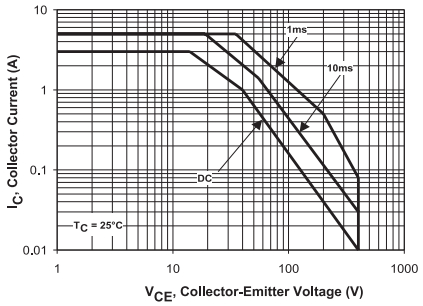
"ON" Voltage



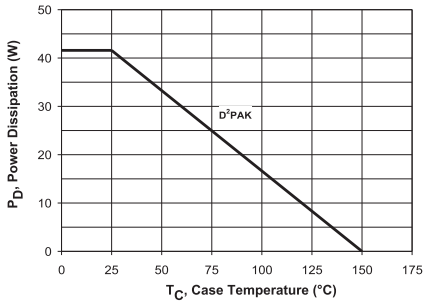
Capacitance



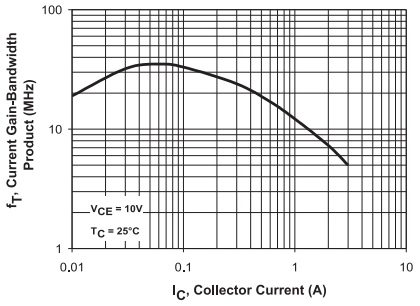
Safe Operating Area



Power Derating



Current Gain-Bandwidth Product



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