CompactPCI® Backplane Interface / Termination IC

Features

- Eleven channel termination
- Hot-swap capability
- Suitable for system slot boards
- Industrial temperature range: -40°C to +85°C
- Typical TCR of resistors: -100 ppm/°C
- Very low channel capacitance
- 28-pin TSSOP package
- Allows backplane termination with minimal PCB footprint

Applications

- Hot-swap CompactPCI® cards
- Computer Telephony
- Industrial PCs
- Telecom/Datacom equipment
- Instrumentation
- Real-time Machine Control
- Industrial Automation

Product Description

The CMCPCI100 is an 11-channel backplane interface/ termination IC specifically designed for the latest version of the CompactPCI specification. The CMCPCI100 allows CompactPCI boards to interface to the backplane. To minimize signal reflection and ringing, it provides a 10Ω resistor for each channel to terminate the transmission line stub on the board, per CompactPCI specification.

The CompactPCI standard requires system boards to be hot-swappable. To accommodate this requirement, the CMCPCI100 features a switched 10kΩ resistor connected to the 1V Precharge Supply Voltage which allows for live insertion of boards. If the precharge enable pin (P_EN) is asserted, then the 10kΩ pull-up resistors are connected to precharge the circuits.
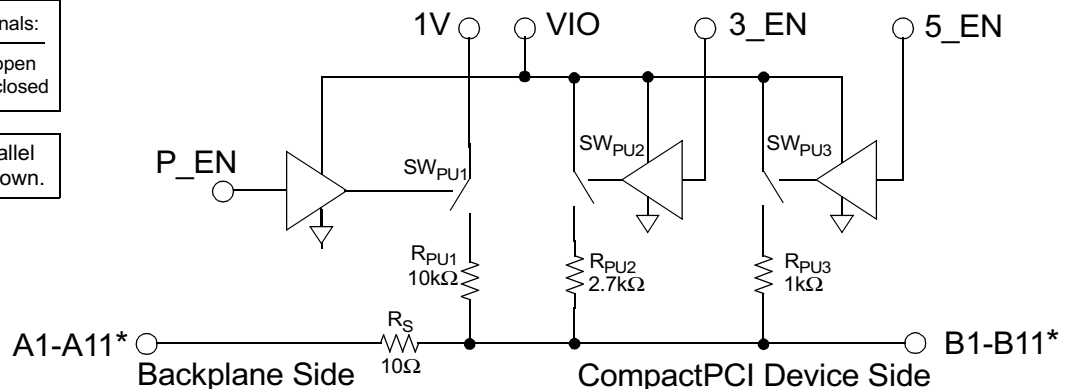
In addition, a system board requirement mandates either a 1.0kΩ pull-up resistor or a 2.7kΩ resistor connected to VIO. CompactPCI slot cards must work in either 3.3V or 5V systems, hence the need for both 2.7kΩ and 1kΩ resistors. If the 3_EN pin is logic high, the 2.7kΩ resistor is used as the pull-up. If the 5_EN pin is logic high, the 1kΩ resistor is used.
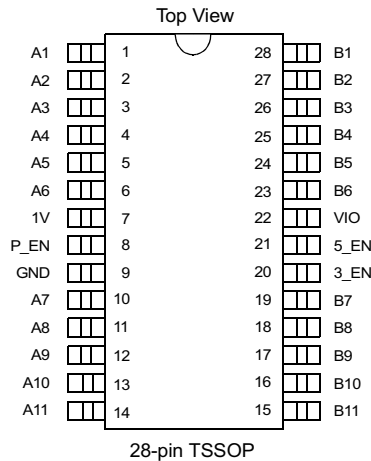
The CMCPCI100 integrates all these functions into a low-profile 28-pin TSSOP package.

Simplified Electrical Schematic

For all enable signals:
Logic 0 = switch open
Logic 1 = switch closed

*One of 11 parallel channels is shown.

PACKAGE / PINOUT DIAGRAM

Top View

A1	1	28	B1
A2	2	27	B2
A3	3	26	B3
A4	4	25	B4
A5	5	24	B5
A6	6	23	B6
1V	7	22	VIO
P_EN	8	21	5_EN
GND	9	20	3_EN
A7	10	19	B7
A8	11	18	B8
A9	12	17	B9
A10	13	16	B10
A11	14	15	B11

28-pin TSSOP

Note: This drawing is not to scale.

PIN DESCRIPTIONS

PIN(S)	NAME	DESCRIPTION
1-6	A1 - A6	The backplane-side input signals for channels 1 through 6, respectively. These pins are configured with a 10kΩ internal precharge (pull-up) resistor which is switch-controlled by P_EN (pin 8).
10-14	A7 - A11	The backplane-side input signals for channels 7 through 11, respectively. These pins are configured with a 10kΩ internal precharge (pull-up) resistor which is switch-controlled by P_EN (pin 8).
23-28	B1 - B6	The device-side connection for channels 1 through 6, respectively.
15-19	B7 - B11	The device-side connection for channels 7 through 11, respectively.
7	1V	A 1-volt precharge supply voltage input for all channels.
8	P_EN	The precharge enable input which controls the precharge pull-up resistors for all channels. When this active high control signal is set to '1', precharge of channels A1 through A11 is enabled.
9	GND	The ground voltage reference for the CMCPCI100.
20	3_EN	The enable signal for the device-side channel pull-up mechanism when 3.3V is the supply voltage. When this active high control signal is set to '1', the 2.7kΩ pull-up resistor which pulls up the channel to the supply rail is engaged.
21	5_EN	The enable signal for the device-side channel pull-up mechanism when 5V is the supply voltage. When this active high control signal is set to '1', the 1kΩ pull-up resistor which pulls up the channel to the supply rail is engaged.
22	VIO	The positive supply voltage for the CMCPCI100. Either 3.3V or 5V may be used.

Ordering Information

PART NUMBERING INFORMATION

Pins	Package	Ordering Part Number[1]	Part Marking
28	TSSOP	CMCPCI100T	CMCPCI100TS

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
VIO (supply voltage)	-0.5 to +6	V

Pin Voltages
    1V, P_EN, 3_EN, 5_EN
    A1-A11
    B1-B11
	
	-0.5 to (VIO+0.5)
	-0.5 to (VIO+0.5)
	-0.5 to (VIO+0.5)
		
		V
		V
		V

ESD Withstand Voltage (Note 1)
    Human Body Model, MIL-STD-883D, Method 3015 (Note 2)
        VIO, 1V, P_EN, 5_EN, 3_EN
        All other pins
	
	±2
	±1.25
		
		kV
		kV

Storage Temperature Range	-65 to +150	°C
Operating Temperature Range (Ambient)	-40 to +85	°C
DC Power per Resistor	62	mW
Package Power Rating	1	W

Note 1: This parameter guaranteed by design.
Note 2: ESD is applied to input / output pins with respect to GND, one at a time; unused pins are left open.

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
VIO (supply voltage)	3 to 5.5	V

Pin Voltages
    P_EN, 3_EN, 5_EN
    A1-A11
    B1-B11
	
	0 to VIO
	0 to VIO
	0 to VIO
		
		V
		V
		V

Ambient Operating Temperature Range	-40 to +85	°C

Specifications (Continued)

ELECTRICAL OPERATING CHARACTERISTICS[1]						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
R_S	Series Resistance through R_S	A to B; T_A=25°C		10		Ω
R_{PU1}	Resistance of R_{PU1} pull-up	T_A=25°C	9.5		15	kΩ
R_{PU2}	Resistance of R_{PU2} pull-up	T_A=25°C		2.7		kΩ
R_{PU3}	Resistance of R_{PU3} pull-up	T_A=25°C		1.0		kΩ
TOL_{RS} TOL_{RPU2} TOL_{RPU3}	Resistance Tolerance (R_S, R_{PU2}, R_{PU3})	T_A=25°C			±5	%
TCR_{PU}	Temperature Coefficient of Resistance (R_{PU1}, R_{PU2}, R_{PU3})			-100		ppm/°C
TCR_S	Temperature Coefficient of Resistance (R_S)			+250		ppm/°C
C_1	Capacitance on backplane side (A side) of series resistor R_S	Measured @ 66MHz; VIO=5V; 5_EN=5V; 30mV osc level; Note 2		1.4		pF
C_2	Capacitance on device side (B side) of series resistor R_S	Measured @ 66MHz; VIO=5V; 5_EN=5V; 30mV osc level; Note 2		2.6		pF
V_{IL}	Logic Low Input Voltage to P_EN, 3_EN, 5_EN		-0.5		VIO x 0.3	V
V_{IH}	Logic High Input Voltage to P_EN, 3_EN, 5_EN		VIO x 0.57		VIO + 0.5	V
I_{LEAK}	Leakage Current into P_EN, 3_EN, 5_EN	GND < V < VIO		±1	±10	μA
t_{PLH}, t_{PHL}	Switch closure delay from the low-to-high or high-to-low transition of enable signal	Note 2			10	ns

Note 1: All parameters specified at T_A= -40 to +85°C unless otherwise noted.
Note 2: This parameter is guaranteed by design; it is not tested 100%.

Performance Information

Channel Charge Characteristics

Figure 1 shows a possible power-up sequence of the CMCPCI100. The channel (in this case measured at B3) is initially at ground. When the P_EN signal is asserted, the channel is connected to the 1V Precharge Supply Voltage via R_{PU1} (10kΩ). With a 30pF load on the channel it is easy to see the channel charging up to 1V.

Then the P_EN signal deasserts to logic LOW, and the 5_EN signal becomes logic HIGH. The channel is connected to VIO (5V) via R_{PU3} (1kΩ).
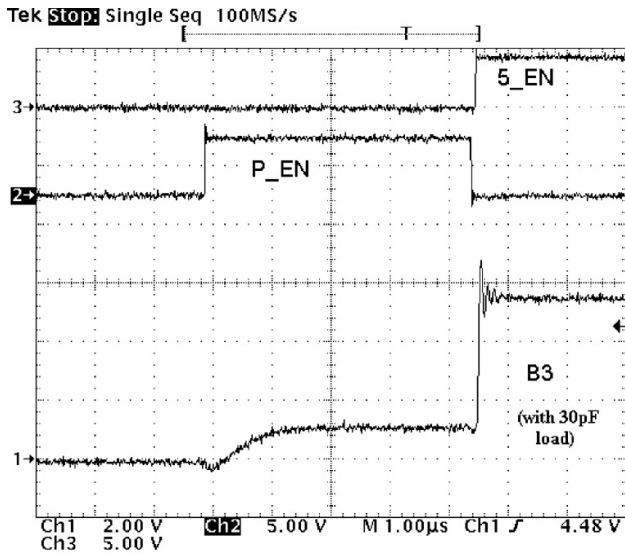
Figure 1. Example Power-Up Sequence

Capacitance Variation with Frequency

Figure 2 graphs A through D show how the capacitance varies with frequency. The capacitance of the signal channel is lower at high frequencies because the capacitance of the switches is decoupled by the pull-up resistors.
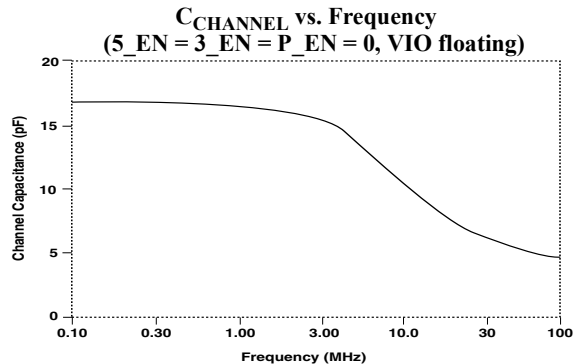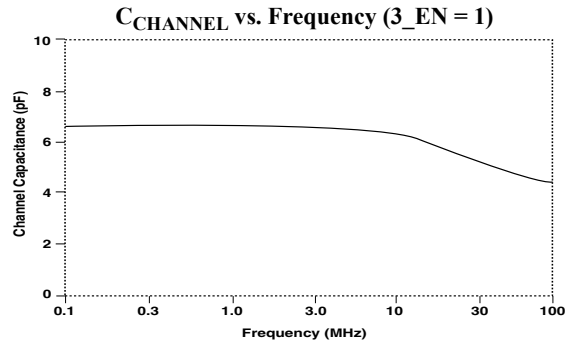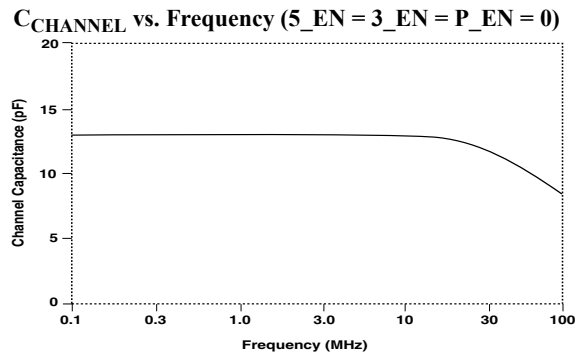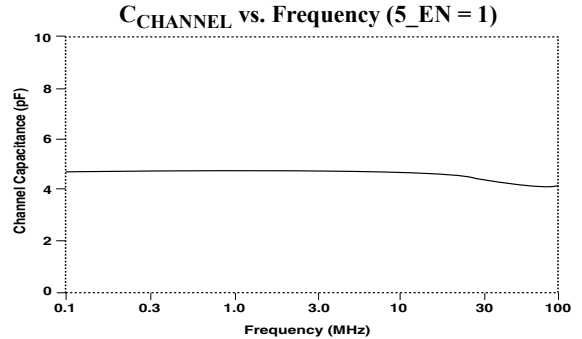

Figure 2. Capacitance Variance with Frequency

Application Information

Board Layout Recommendations

The CMCPCI100 devices should be located on the board as close as possible to the CompactPCI connector. Most of the signals do need to be terminated (with series stub and pull-up resistors), but some signals can be left out depending on the application and the type of board.

For 32-bit System slot boards, the following signals needs to be terminated:

AD0-AD31, C/BE0#-C/BE3#, PAR, FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR#, RST#, REQ64#, and ACK64#

If used on the board, the following signals should be terminated:

INTA#, INTB#, INTC# and INTD#

For 64-bit System slot boards, the following signals should also be terminated:

AD32-AD63, C/BE4#-C/BE7#, and PAR64.

Figure 3 shows a 64-bit system board connection between the CMCPCI100 termination and the CompactPCI 5-row connector (2 mm pitch) labeled A to E (row F is Ground). The System slot should have signal lengths not exceeding 63.5 mm (2.5 inches). To minimize trace length, it is recommended that the CMCPCI100s be placed on alternate sides of the PC board. The configuration shown illustrates a fully-terminated 64-bit board utilizing 10 CMCPCI100 devices. Some applications (e.g. 32-bit boards) do not require all lines to be terminated, per the above table.

The CMCPCI100 resistors have a very low TCR (typically -100ppm/°C) so that resistance will not fluctuate over temperature. Buffers are implemented on P_EN, 5_EN, and 3_EN inputs to ensure that switches turn on and off completely.

A typical system slot card may use 10 CMCPCI100 devices to replace 14 16-bit FET bus switches and 76 4-resistor packs (0805 form factor), thus providing significant reduction in both component count and assembly costs. At the same time this highly integrated solution improves reliability and manufacturing efficiency, saves board area for space-critical designs, and satisfies CompactPCI height requirements.
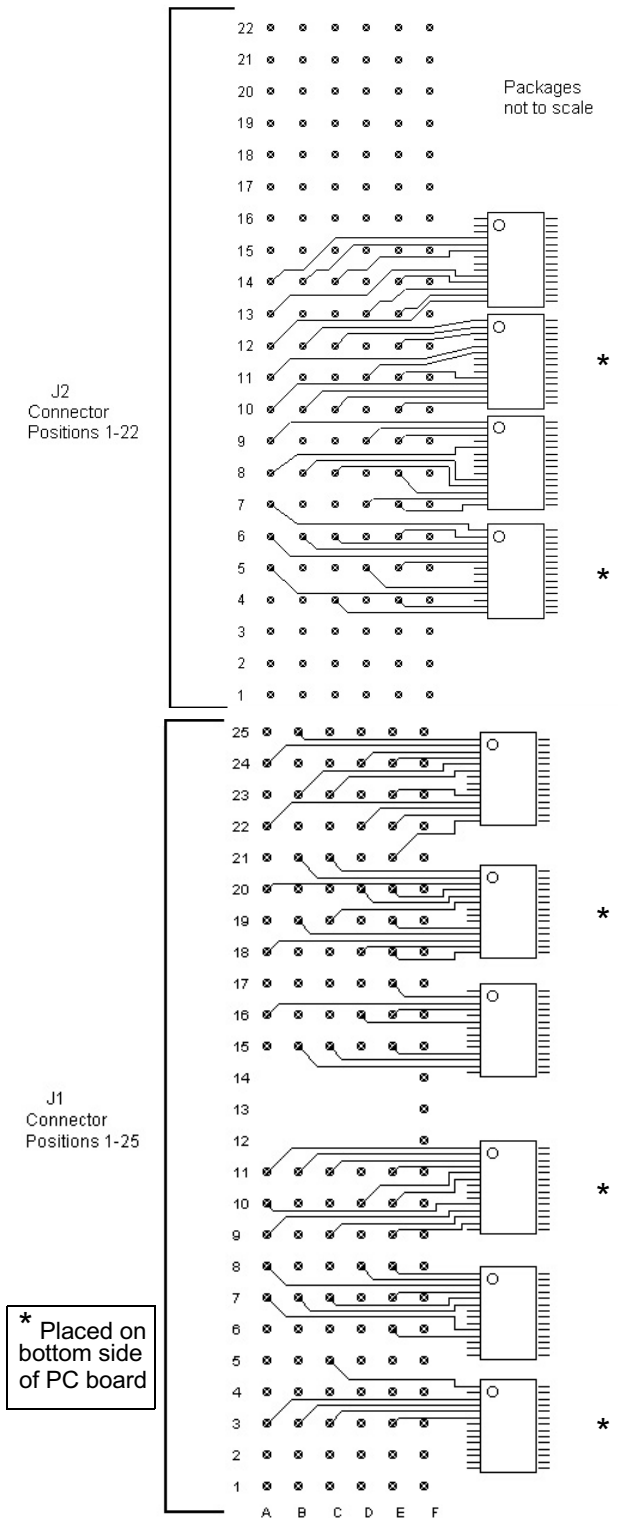
Packages not to scale

J2 Connector Positions 1-22

J1 Connector Positions 1-25

* Placed on bottom side of PC board

A B C D E F

Figure 3. Schematic for 64-bit System Board

Mechanical Details

TSSOP Mechanical Specifications

CMCPCI100 devices are packaged in 28-pin TSSOP packages. Dimensions are presented below.

For complete information on the TSSOP-28 package, see the California Micro Devices TSSOP Package Information document.

PACKAGE DIMENSIONS				
Package	TSSOP			
Pins	28			
Dimensions	Millimeters		Inches	
	Min	Max	Min	Max
A	—	1.10	—	0.0433
A1	0.05	0.15	0.002	0.006
B	0.19	0.30	0.0075	0.0118
C	0.09	0.20	0.0035	0.0079
D	9.60	9.80	0.378	0.386
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.0256 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
# per tube	50 pieces*			
# per tape and reel	2500 pieces			
Controlling dimension: millimeters				

* This is an approximate number which may vary.

Mechanical Package Diagrams

TOP VIEW

SIDE VIEW

END VIEW
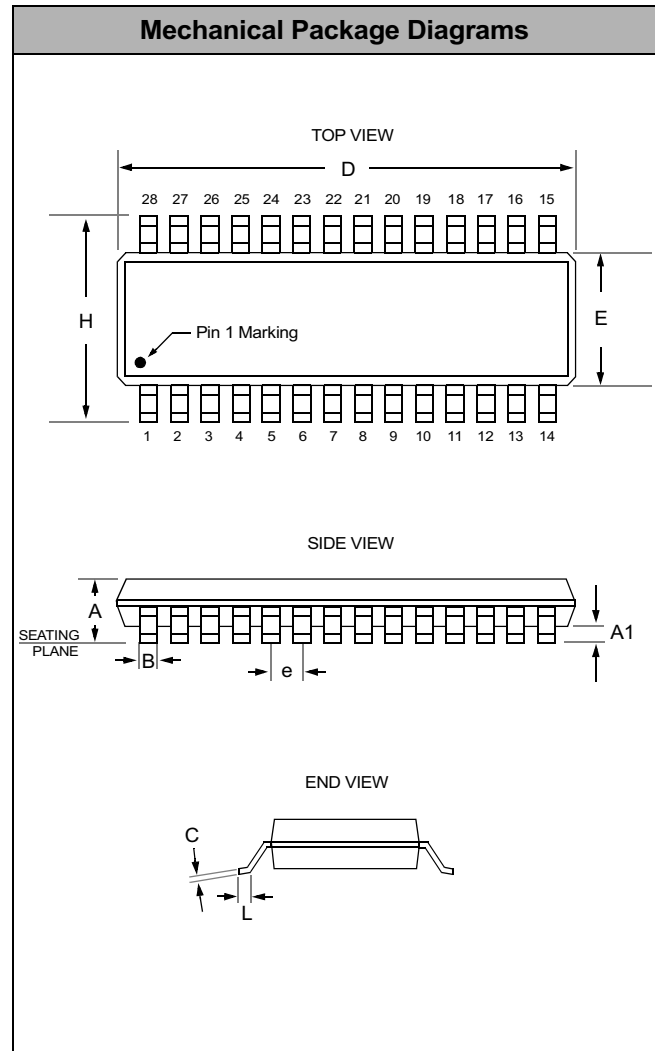
Package Dimensions for TSSOP-28