DDR V_{DDQ} and Termination Voltage Regulator

Features

- 5A continuous current from V_{DDQ}
- 1.8V to 2.6V adjustable V_{DDQ} output voltage
- 600 mV typical V_{DDQ} dropout voltage at 5A
- V_{TT} tracking at 50% of V_{DDQ}
- Source and sink up to 2A V_{TT} current
- Excellent load and line regulation, low noise
- Fast transient response
- Meets JEDEC DDR-I SDRAM power spec.
- Linear regulator design requires no inductors and has low external component count
- Integrated power MOSFETs
- Dual purpose ADJ/Shutdown pin
- Built-in over-current limit with short-circuit foldback and thermal shutdown for V_{DDQ} and V_{TT}
- 5mA quiescent current
- TO252 andTO263 packages for high performance thermal dissipation and easy PC board layout
- Optional RoHS Compliant Lead-free packaging

Product Description

The CM3205 is a dual-output, low noise linear regulator designed to meet SSTL-2 and SSTL-3 specifications for DDR-SDRAM V_{DDQ} supply and termination voltage V_{TT} supply. With integrated power MOSFET's, the CM3205 can source up to 5A of V_{DDQ} current, and source or sink up to 2A V_{TT} current. The typical dropout voltage for V_{DDQ} is 600 mV at 5A load current.

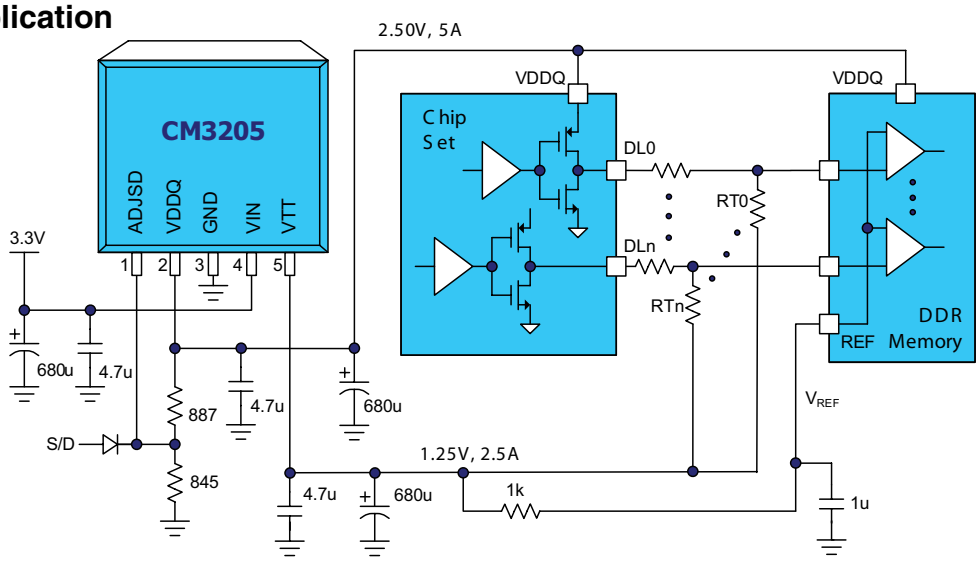
The CM3205 provides fast response to transient load changes. Load regulation is excellent, less than 1%, from no load to full load. It also has built-in over-current limits and thermal shutdown at 170°C.

The CM3205 is packaged in an easy-to-use 5-pin D^2PAK (TO263-5) and DPAK (TO252-5). Low thermal resistance (48°C/W) allows it to withstand 1.7W (1) dissipation at 85°C ambient. It can operate over the industrial ambient temperature range of –40°C to 85°C.

Applications

- DDR memory and active termination buses
- Desktop Computers, Servers
- Residential and Enterprise Gateways
- DSL Modems
- Routers and Switchers
- DVD recorders
- 3D AGP cards
- LCD TV and STB

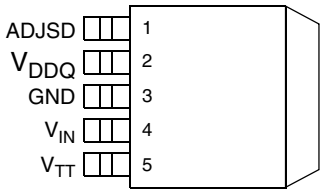
Typical Application



Package Pinout

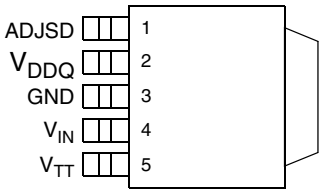
PACKAGE / PINOUT DIAGRAM

Top View



5-Lead TO-263-5 Package
CM3205-00TN

Top View



5-Lead TO-252-5 Package
CM3205-00TP

Note: This drawing is not to scale.

Ordering Information

PART NUMBERING INFORMATION

Pins	Package	Lead-free Finish	
		Ordering Part Number[1]	Part Marking
5	TO-263-5	CM3205-00TN	
5	TO-252-5	CM3205-00TP	

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS

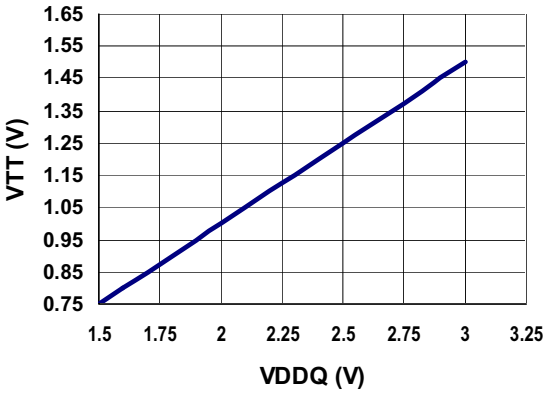
PARAMETER	RATING	UNITS
V_{IN} to GND	[GND - 0.3] to +6.0	V
Pin Voltages V_{DDQ} ,V_{TT} to GND ADJSD to GND	 [GND - 0.3] to +6.0 [GND - 0.3] to +6.0	 V V
Storage Temperature Range	-65 to +150	°C
Operating Temperature Range	-40 to +85	°C
Lead Temperature (Soldering, 10s)	300	°C

Specifications (cont'd)

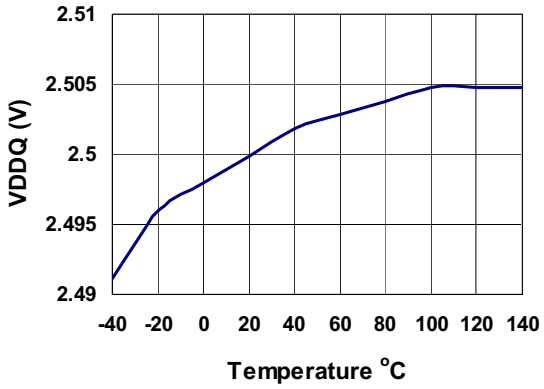
ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
V_{IN} = 3.3V, typical values are at T_A = 25°C (unless otherwise specified)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
VIN						
V_{IN}	Supply Voltage Range		3.15	3.30	3.50	V
V_{UVLO}	Under-voltage Lockout	All outputs are no load	2.4	2.7	2.9	V
	UVLO Hysterisis			100		mV
I_Q	Quiescent Current	V_{DDQ} = 0V, V_{TT} = 0V, ADJSD = 3.3V (shutdown)		3		mA
		V_{DDQ} = 2.5V, V_{TT} = 1.25V, (no load)		5		mA
V_{DDQ} Regulator						
	Output Current Limit	V_{OUT} = 2.5V	6.0	8.0		A
V_{REF}	Reference Voltage		1.203	1.215	1.227	V
I_{BIAS}	Input Bias Current (I_{ADJ})	VADJSD = V_{REF}		30	200	nA
$V_{R\ LOAD}$	Load Regulation	I_O = 10 mA to 5A		1		%
$V_{R\ LINE}$	Line Regulation	V_{IN} = 3.15V to 3.5V, I_O = 10 mA		0.5		%
$V_{DROPOUT}$	Dropout Voltage	V_{IN} = 3.15V, I_O = 5A		600		mV
V_{TT} Regulator						
	Output Current Limit (Source)	V_{OUT} = 1.25V	2	2.5		A
	Output Current Limit (Sink)	V_{OUT} = 1.25V	2	2.5		A
$V_{R\ VTTLOAD}$	Load Regulation	I_O = 0A to 2A		1		%
		I_O = 0A to -2A		1		%
Over Temperature Protection						
	Thermal Shutdown Temperature			170		°C
	Thermal Shutdown Hysteresis			50		°C

Typical Operating Curves

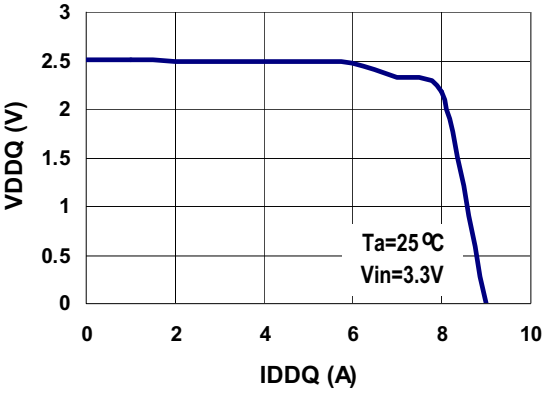
VTT vs. VDDQ



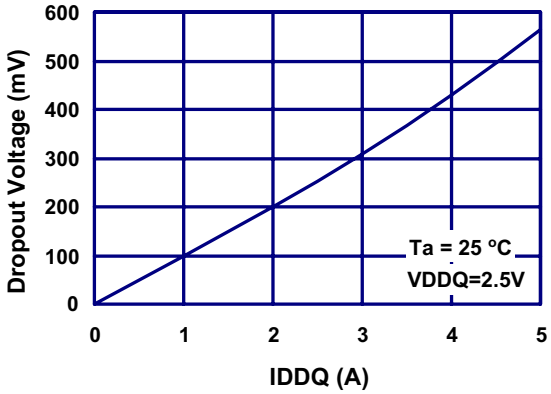
VDDQ vs. Temperature



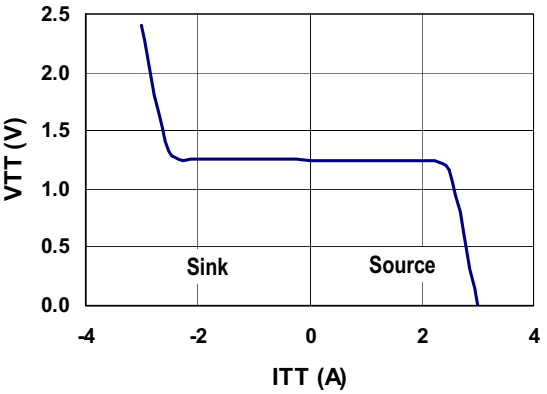
VDDQ vs. Load Current



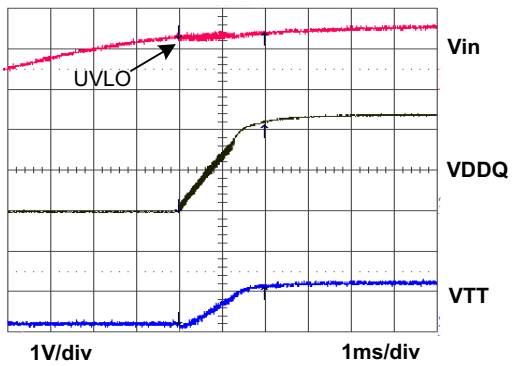
VDDQ Dropout vs. IDDQ



VTT vs. Load Current

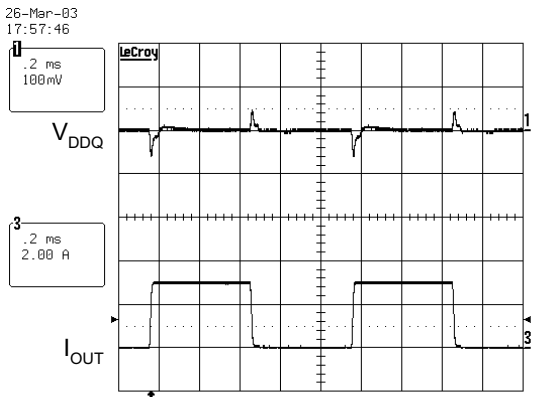


Startup into Full Load



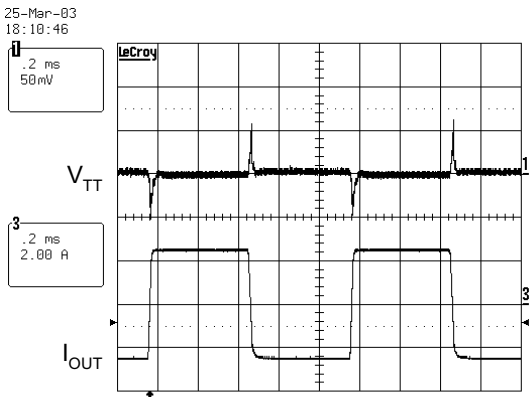
Typical Operating Characteristics

VDDQ Transient Response



V_{IN} = 3.3V
I_{OUT} Step: 10mA ~ 3A

VTT Transient Response

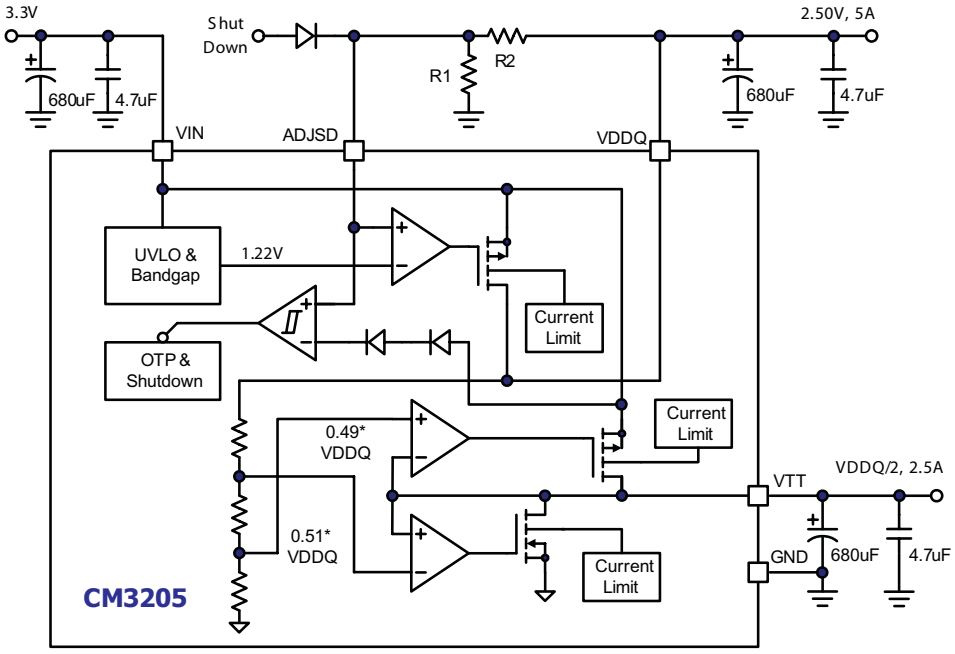


V_{IN} = 3.3V
I_{OUT} Step: -2.5A ~ +2.5A

Pin Descriptions

PIN DESCRIPTIONS		
PIN(S)	**NAME**	**DESCRIPTION**
1	ADJSD	This pin is for V_{DDQ} output voltage adjustment. The V_{DDQ} output voltage is set using an external resistor divider connected to ADJSD. The output voltage is determined by the following formula: $V_{DDQ} = 1.215V \times \frac{R1 + R2}{R1}$ where R1 is the ground-side resistor and R2 is the upper resistor of the divider. Connect these resistors to the V_{DDQ} output at the point of regulation. In addition, this input functions as a shutdown pin. Apply a voltage higher than V_{IN}-1.2V to this pin to simultaneously shutdown both V_{DDQ} and V_{TT} outputs. The outputs are restored when the voltage on this pin falls below V_{IN}-1.2V. A low-leakage diode in series with the shutdown input signal is recommended to avoid interference with the voltage adjustment setting.
2	V_{DDQ}	V_{DDQ} regulator output voltage pin.
3	GND	GROUND reference pin. The back tab is also ground and serves as the package heatsink. It should be soldered to the circuit board copper to remove excess heat from the IC.
4	V_{IN}	Input voltage pin, typically 3.3V from the power supply.
5	V_{TT}	V_{TT} regulator output voltage pin, which is preset to 50% of V_{DDQ}.

Functional Block Diagram



Application Information

Powering DDR Memory

Double-Data-Rate (DDR) memory has provided a huge step in performance for personal computers, servers and graphic systems. As is apparent in its name, DDR operates at double the data rate of earlier RAM, with two memory accesses per cycle versus one. DDR SDRAM's transmit data at both the rising falling edges of the memory bus clock.

DDR's use of Stub Series Terminated Logic (SSTL) topology improves noise immunity and power-supply rejection, while reducing power dissipation. To achieve this performance improvement, DDR requires more complex power management architecture than previous RAM technology.

Unlike the conventional DRAM technology, DDR SDRAM uses differential inputs and a reference voltage for all interface signals. This increases the data bus bandwidth, and lowers the system power consumption. Power consumption is reduced by lower operating voltage, a lower signal voltage swing associated with Stub Series Terminated Logic (SSTL_2) and by the use of a termination voltage, V_{TT}. SSTL_2 is an industry standard, defined in JEDEC document JESD8-9. SSTL_2 maintains high-speed data bus signal integrity by reducing transmission reflections. JEDEC further defines the DDR SDRAM specification in JESD79C.

DDR memory requires three tightly regulated voltages: V_{DDQ}, V_{TT}, and V_{REF} (see Figure 1). In a typical SSTL_2 receiver, the higher current V_{DDQ} supply voltage is normally 2.5V with a tolerance of ±200 mV. The active bus termination voltage, V_{TT}, is half of V_{DDQ}. V_{REF} is a reference voltage that tracks half of V_{DDQ}, ± 1%, and is compared with the V_{TT} terminated signal at the receiver. V_{TT} must be within ±40 mV of V_{REF}.

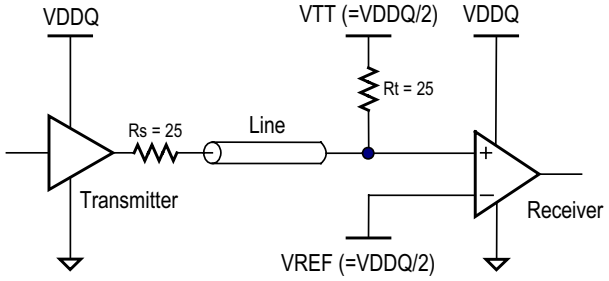


Figure 1. Typical DDR terminations, Class II

Application Information (cont'd)

The V_{TT} power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2 mA to achieve the 405 mV minimum over V_{TT} needed at the receiver:

$$I_{terminaton} = \frac{405mV}{Rt(25\Omega)} = 16.2mA$$

A typical 128 Mbyte SSTL-2 memory system, with 192 terminated lines, has a worst-case maximum V_{TT} supply current up to ±3.11A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the V_{TT} external capacitor. In a real memory system, the continuous average V_{TT} current level in normal operation is less than ±200 mA.

The V_{DDQ} power supply, in addition to supplying current to the memory banks, could also supply current to controllers and other circuitry. The current level typically stays within a range of 2.0A to 3.0A, with peaks up to 4.0A or more, depending on memory size and the computing operations being performed.

The tight tracking requirements and the need for V_{TT} to sink, as well as source, current provide unique challenges for powering DDR SDRAM.

CM3205 Regulator

The CM3205 dual output linear regulator provides all of the power requirements of DDR memory by combining two linear regulators into a single TO-263 or TO-252 5-lead package. The V_{DDQ} regulator can supply up to 5A continuous current, and the two-quadrant V_{TT} termination regulator has current sink and source capability to ±2A. The V_{DDQ} linear regulator uses a PMOS pass element for a very low dropout voltage, typically 600mV at a 5A output. The output voltage of the V_{DDQ} regulator can be set by an external voltage divider. The second output, V_{TT}, is regulated at $V_{DDQ}/2$ by an internal resistor divider. The V_{TT} regulator can source, as well as sink, up to 2A continuous current. The CM3205 is designed for optimal operation from a nominal 3.3VDC bus, but can work with V_{IN} as high as 5V. When operating at higher V_{IN} voltages, attention must be given to the increased package power dissipation and proportionally increased heat generation.

V_{REF} is typically routed to inputs with high impedance, such as a comparator, with little current draw. An adequate V_{REF} can be created with a simple voltage divider of precision, matched resistors from V_{DDQ} to ground. A small ceramic bypass capacitor can also be added for improved noise performance.

Input and Output Capacitors

The CM3205 requires that at least a 680µF electrolytic capacitor be located near the V_{IN} pin for stability and to maintain the input bus voltage during load transients. An additional 4.7µF ceramic capacitor between the V_{IN} (pin 4) and the GND (pin 5), located as close as possible to those pins, is recommended to ensure stability.

A minimum of a 680µF electrolytic capacitor is recommended for the V_{DDQ} output. An additional 4.7µF ceramic capacitor between the V_{DDQ} (pin 2) and GND, located very close to those pins, is recommended.

A minimum of a 680µF, electrolytic capacitor is recommended for the V_{TT} output. This capacitor should have low ESR to achieve best output transient response. SP or OSCON capacitors provide low ESR at high frequency, and thus are a good choice. In addition, place a 4.7µF ceramic capacitor between the V_{TT} pin (pin 5) and GND, located very close to those pins. The total ESR must be low enough to keep the transient within the V_{TT} window of 40 mV during the transition for source to sink. An average current step of ±0.5A requires:

$$ESR < \frac{40mV}{1A} = 40m\Omega$$

Both outputs will remain stable and in regulation even during light or no load conditions.

Adjusting V_{DDQ} Output Voltage

The CM3205 internal bandgap reference is set at 1.215V. The V_{DDQ} voltage is adjustable by using a resistor divider, R1 and R2:

$$V_{OUT} = V_{ADJ} \times \left(1 + \frac{R2}{R1}\right)$$

Application Information (cont'd)

where V_{ADJ} = 1.215V (± 1%). For best regulator stability, we recommend that R1 and R2 not exceed 10 kΩ each.

Shutdown

Pin 1 (ADJSD) also serves as a shutdown pin. When pin 1 is pulled high, > (V_{IN} - 1.2V), the V_{DDQ} output is turned off and both source and sink MOSFET's of the V_{TT} regulator are set to a high impedance state. During shutdown, the quiescent current is reduced to less than 3mA, independent of output load.

It is recommended that a 1N914 or equivalent low leakage diode be placed between Pin 1 and an external shutdown signal to prevent interference with the ADJ pin's normal operation. When the diode anode is pulled low, or left open, the CM3205 is again enabled.

Current Limit, Foldback and Over-temperature Protection

The CM3205 features internal current limiting with thermal protection. During normal operation, V_{DDQ} limits the output current to approximately 8A and V_{TT} limits the output current to approximately ±2A. When V_{TT} is current limiting into a hard short circuit, the output current folds back to a lower level, about 1.5A, until the over-current condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the junction temperature of the device exceeds 170 °C (typical), the thermal protection circuitry triggers and shuts down both outputs. Once the junction temperature has cooled to below about 120 °C, the CM3205 returns to normal operation.

Thermal Considerations

Both the TO-252 and the TO-263 packages provide a very effective thermal conduction path from the silicon junction into the PC board to which it is mounted. See Figure 2 below. These surface mount packages have a large metal tab that solders to the PC board, where the ground plane can serve as heatsink. This metal tab connects internally to GND (pin 3). A top-layer ground plane is the best in terms of convection air-cooling, a bottom-layer ground plane is less effective, and a middle layer ground plane of a multiple-layer PC board is the least effective.

We recommend the metal tab of CM3205 be soldered to a minimum of 3 square inches of ground plane on the top side of the PC board. Use 20 or more plate-through vias to connect the top layer ground plane to ground planes on other layers.

When measured in accordance to JEDEC JESD51-3, under natural convection without forced airflow, the Theta junction-to-air (θja) resistance is approximately 48 °C/watt for the CM3205-00TN (TO-263-5), and 55 °C/watt for the CM3205-00TP (TO-252-5).

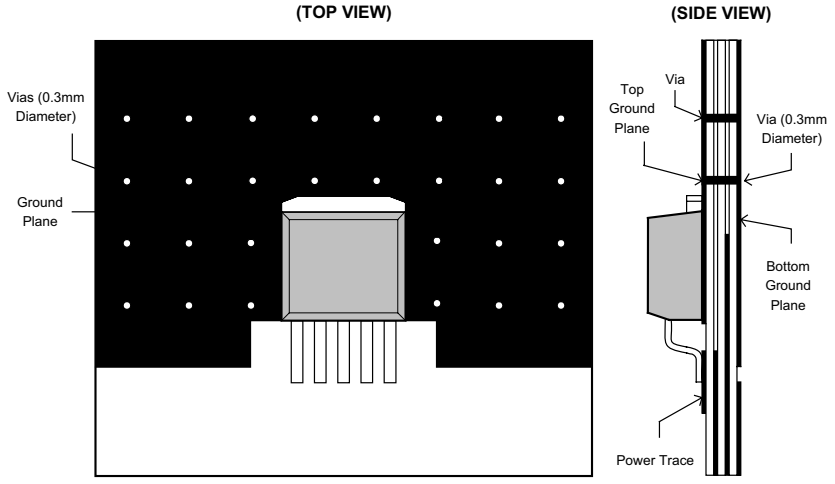


Figure 2. Thermal Layout

Mechanical Details

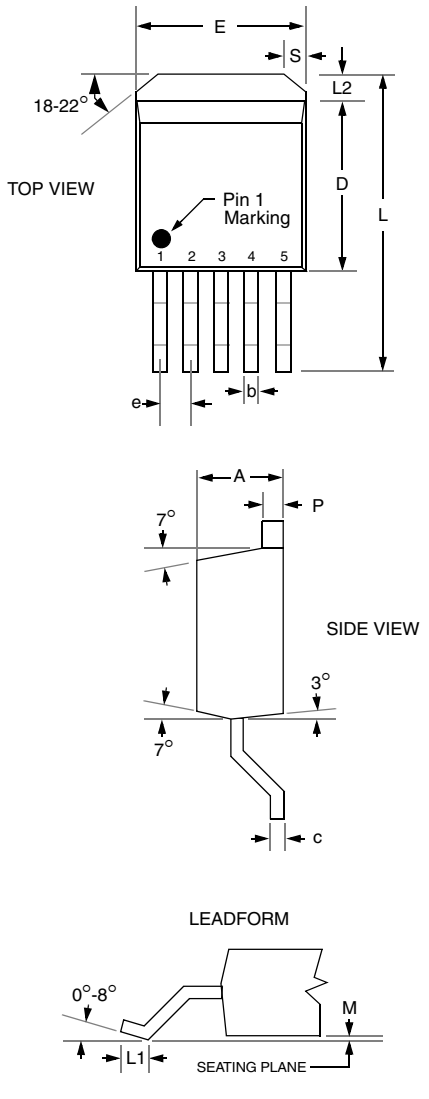
TO-263-5 Mechanical Specifications

Dimensions for CM3205-00TN devices packaged in 5-lead, standard TO-263 packages are presented below.

PACKAGE DIMENSIONS				
Package	TO-263			
Pins	5			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	4.34	4.60	0.171	0.181
b	0.74	0.89	0.029	0.035
c	0.33	0.43	0.013	0.017
D	8.92	9.17	0.351	0.361
E	10.16	10.67	0.400	0.420
e	1.70 REF		0.067 REF	
L	14.61	15.88	0.575	0.625
L1	2.29	2.79	0.090	0.110
L2	1.14	1.40	0.045	0.055
M	0.23	0.30	0.009	0.012
P	1.14	1.40	0.045	0.055
S	1.40	1.91	0.055	0.075
# per tape and reel	750 pieces			
Controlling dimension: inches				

* This is an approximate amount which may vary.

Mechanical Package Diagrams



Package Dimensions for Standard TO-263

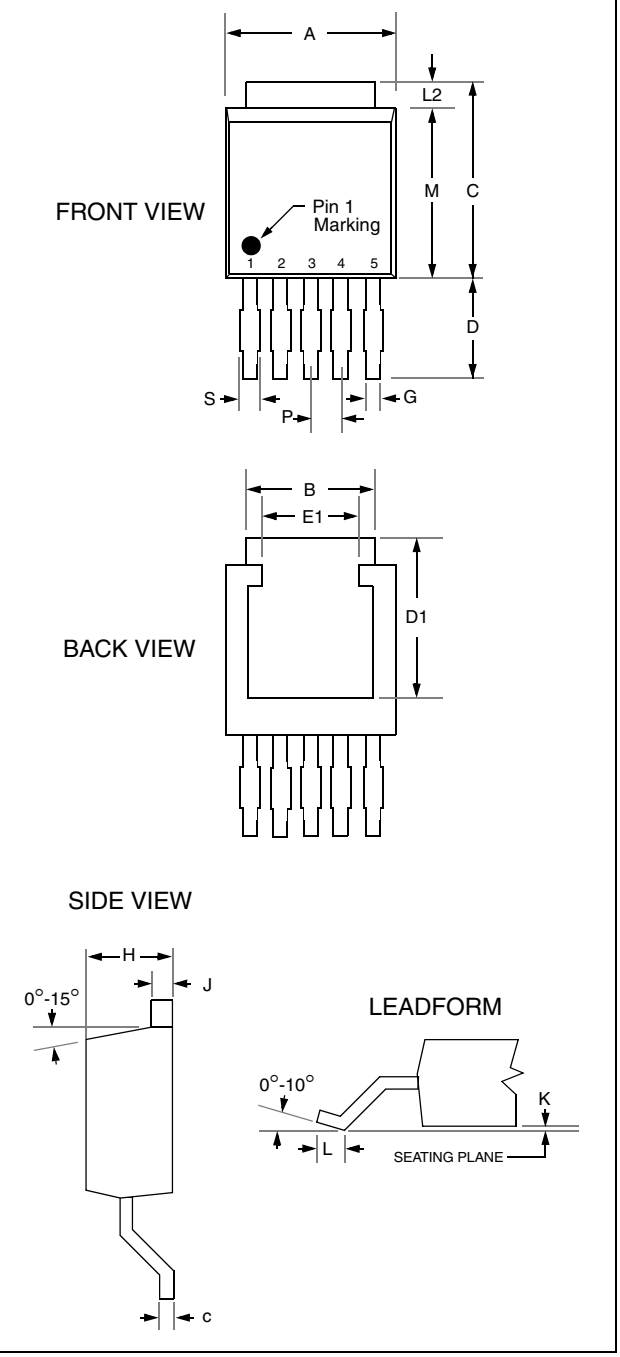
Mechanical Details (cont'd)

TO-252-5 Mechanical Specifications

Dimensions for CM3205-00TP devices packaged in 5-pin TO-252 packages are presented below.

PACKAGE DIMENSIONS				
Package	TO-252			
Pins	5			
Dimensions	**Millimeters**		**Inches**	
	Min	**Max**	**Min**	**Max**
A	6.40	6.80	0.252	0.268
B	5.20	5.50	0.205	0.217
C	6.80	7.20	0.268	0.283
D	2.20	2.80	0.087	0.110
G	0.40	0.60	0.016	0.024
H	2.20	2.40	0.087	0.094
J	0.45	0.55	0.018	0.022
K	0	0.15	0	0.006
L	0.90	1.50	0.035	0.059
M	5.40	5.80	0.213	0.228
P	1.27 REF		0.05 REF	
S	0.50	0.80	0.020	0.031
# per tape and reel	750 pieces			
Controlling dimension: inches				

Mechanical Package Diagrams



Package Dimensions for TO252-5