

16 Volt Digitally Programmable Potentiometer (DPP™) with 128 Taps and 2-wire Interface



FEATURES

- Single linear DPP with 128 taps
- End-to-end resistance of 10kΩ, 50kΩ or 100kΩ
- 2-wire (I²C-like) interface
- Fast Up/Down wiper control mode
- Non-volatile wiper setting storage
- Automatic wiper setting recall at power-up
- Digital Supply range (V_{CC}): 2.7V to 5.5V
- Analog Supply range (V₊): +8V to +16V
- Low Standby Current: 15μA
- 100 Year wiper setting memory
- Industrial Temperature range: -40°C to +85°C
- RoHS-compliant 10-pin MSOP package

APPLICATIONS

- LCD screen adjustment
- Volume control
- Mechanical potentiometer replacement
- Gain adjustment
- Line impedance matching
- VCOM setting adjustments

For Ordering Information details, see page 13.

DESCRIPTION

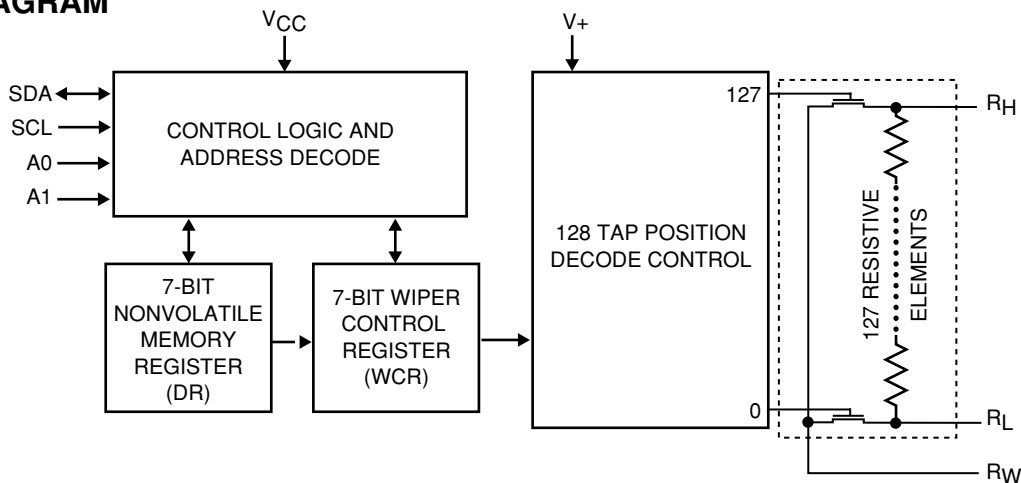
The CAT5132 is a high voltage Digitally Programmable Potentiometer (DPP) with non-volatile wiper setting memory, operating like a mechanical potentiometer. The tap points between the 127 equal resistive elements are connected to the wiper output via CMOS switches. The switches are controlled by a 7-bit Wiper Control Register (WCR). The wiper setting can be stored in a 7-bit non-volatile Data Register (DR). The WCR is accessed via the 2-wire serial bus.

Upon power-up, the WCR is set to mid-scale (1000000). After the power supply is stable, the contents of the DR are transferred to the WCR and the wiper is returned to the memorized setting.

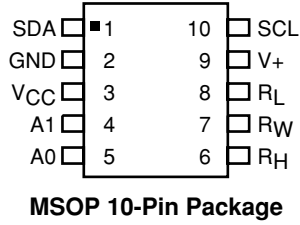
The CAT5132 has two voltage supplies: V_{CC}, the digital supply and V₊, the analog supply. V₊ can be much higher than V_{CC}, allowing for 16V analog operations.

The CAT5132 can be used as a potentiometer or as a two-terminal variable resistor.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

| Pin Number | Name | Description |
|------------|-----------------|--|
| 1 | SDA | Serial Data Input/Output - Bidirectional Serial Data pin used to transfer data into and out of the CAT5132. This is an Open-Drain I/O and can be wire OR'd with other Open-Drain (or Open Collector) I/Os. |
| 2 | GND | Ground |
| 3 | V _{CC} | Digital Supply Voltage (2.7V to 5.5V) |
| 4 | A1 | Address Select Input to select slave address for 2-wire bus. |
| 5 | A0 | Address Select Input to select slave address for 2-wire bus. |
| 6 | R _H | High Reference Terminal for the potentiometer |
| 7 | R _W | Wiper Terminal for the potentiometer |
| 8 | R _L | Low Reference Terminal for the potentiometer |
| 9 | V+ | Analog Supply Voltage for the potentiometer (+8.0V to 16.0V) |
| 10 | SCL | Serial Bus Clock input for the 2-wire Serial Bus. This clock is used to clock all data transfers into and out of the CAT5132 |

ABSOLUTE MAXIMUM RATINGS

| | |
|---|---------------------------------|
| Temperature Under Bias..... | -55 °C to +125 °C |
| Storage Temperature | -65 °C to +150 °C |
| Voltage on any SDA, SCL, A0 & A1 pins with respect to Ground ⁽¹⁾ | -0.3V to V _{CC} + 0.3V |
| Voltage on R _H , R _L & R _W pins with respect to Ground | V+ |
| V _{CC} with respect to Ground | -0.3V to +6V |
| V+ with respect to Ground | -0.3V to +16.5V |
| Wiper Current (10 sec) | ±6mA |
| Lead Soldering temperature (10 sec) | +300 °C |

RECOMMENDED OPERATING CONDITIONS

| |
|---|
| V _{CC} = +2.7V to +5.5V |
| V+ = +8.0V to +16V |
| Operating Temperature Range: -40 °C to +85 °C |

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

Notes:

1. Latch-up protection is provided for stresses up to 100mA on address and data pins from -0.3V to V_{CC} +0.3V.

POTENTIOMETER CHARACTERISTICS

(Over recommended operating conditions unless otherwise stated.)

| Symbol | Parameter | Test Conditions | Limits | | | Units |
|--|--|---|--------|----------|------|--------------------|
| | | | Min | Typ | Max | |
| R _{POT} | Potentiometer Resistance (100kΩ) | | | 100 | | kΩ |
| R _{POT} | Potentiometer Resistance (50kΩ) | | | 50 | | kΩ |
| R _{POT} | Potentiometer Resistance (10kΩ) | | | 10 | | kΩ |
| R _{TOL} | Potentiometer Resistance Tolerance | | | | ±20 | % |
| | Power Rating | 25° C | | | 50 | mW |
| I _W | Wiper Current | | | | ±3 | mA |
| R _W | Wiper Resistance | I _W = ±1mA @ V+ = 12V | | 70 | 150 | Ω |
| | | I _W = ±1mA @ V+ = 8V | | 110 | 200 | Ω |
| V _{TERM} | Voltage on R _W , R _H or R _L | GND = 0V; V+ = 8V to 16V | GND | | V+ | V |
| RES | Resolution | | | 0.78 | | % |
| A _{LIN} | Absolute Linearity ⁽²⁾ | V _{W(n)(actual)} - V _{W(n)(expected)} ^{(5), (6)} | | | ±1 | LSB ⁽⁴⁾ |
| R _{LIN} | Relative Linearity ⁽³⁾ | V _{W(n+1)} - [V _{W(n)} + LSB] ^{(5), (6)} | | | ±0.5 | LSB ⁽⁴⁾ |
| TC _{R_{POT}} | Temperature Coefficient of R _{POT} | ⁽¹⁾ | | ±300 | | ppm/° C |
| TC _{Ratio} | Ratiometric Temperature Coefficient | ⁽¹⁾ | | | 30 | ppm/° C |
| C _H /C _L /C _W | Potentiometer Capacitances | ⁽¹⁾ | | 10/10/25 | | pF |
| fc | Frequency Response | R _{POT} = 50kΩ | | 0.4 | | MHz |

Notes:

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
3. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer.
4. LSB = (R_{HM} - R_{LM})/127; where R_{HM} and R_{LM} are the highest and lowest measured values on the wiper terminal.
5. n = 1, 2, ..., 127
6. V+ @ R_H; 0V @ R_L; V_W measured @ R_W with no load.

D.C. ELECTRICAL CHARACTERISTICS

(Over recommended operating conditions unless otherwise stated.)

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---------------|--|---|---------------------|---------------------|---------------|
| I_{CC1} | Power Supply Current (Volatile Write/Read) | $F_{SCL} = 400\text{kHz}$, SDA Open, $V_{CC} = 5.5\text{V}$, Input = GND | | 1 | mA |
| I_{CC2} | Power Supply Current (Nonvolatile WRITE) | $F_{SCL} = 400\text{kHz}$, SDA Open, $V_{CC} = 5.5\text{V}$, Input = GND | | 3.0 | mA |
| $I_{SB(VCC)}$ | Standby Current ($V_{CC} = 5\text{V}$) | $V_{IN} = \text{GND}$ or V_{CC} , SDA = V_{CC} | | 5 | μA |
| $I_{SB(V+)}$ | V+ Standby Current | $V_{CC} = 5\text{V}$, $V+ = 16\text{V}$ | | 10 | μA |
| I_{LI} | Input Leakage Current | $V_{IN} = \text{GND}$ to V_{CC} | | 10 | μA |
| I_{LO} | Output Leakage Current | $V_{OUT} = \text{GND}$ to V_{CC} | | 10 | μA |
| V_{IL} | Input Low Voltage | | -1 | $V_{CC} \times 0.3$ | V |
| V_{IH} | Input High Voltage | | $V_{CC} \times 0.7$ | $V_{CC} + 1.0$ | V |
| V_{OL1} | Output Low Voltage ($V_{CC} = 3.0$) | $I_{OL} = 3\text{mA}$ | | 0.4 | V |

CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$, $V_{CC} = 5.0\text{V}$

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|-----------|---------------------------------|-----------------------------|-----|-----|-------|
| $C_{I/O}$ | Input/Output Capacitance (SDA) | $V_{I/O} = 0\text{V}^{(1)}$ | | 8 | pF |
| C_{IN} | Input Capacitance (A0, A1, SCL) | $V_{IN} = 0\text{V}^{(1)}$ | | 6 | pF |

A.C. CHARACTERISTICS

| Symbol | Parameter (see Fig. 1) | $V_{CC} = 2.7 - 5.5\text{V}$ | | Units |
|-----------------|---|------------------------------|-----|---------------|
| | | Min | Max | |
| F_{SCL} | Clock Frequency | | 400 | kHz |
| $T_I^{(1)}$ | Noise Suppression Time Constant at SCL & SDA Inputs | | 50 | ns |
| t_{AA} | SLC Low to SDA Data Out and ACK Out | | 1 | μs |
| $t_{BUF}^{(1)}$ | Time the bus must be free before a new transmission can start | 1.2 | | μs |
| $t_{HD:STA}$ | Start Condition Hold Time | 0.6 | | μs |
| t_{LOW} | Clock Low Period | 1.2 | | μs |
| t_{HIGH} | Clock High Period | 0.6 | | μs |
| $t_{SU:STA}$ | Start Condition Setup Time (for a Repeated Start Condition) | 0.6 | | μs |
| $t_{HD:DAT}$ | Data in Hold Time | 0 | | ns |
| $t_R^{(1)}$ | SDA and SCL Rise Time | | 0.3 | μs |
| $t_F^{(1)}$ | SDA and SCL Fall Time | | 300 | ns |
| $t_{SU:STO}$ | Stop Conditions Setup Time | 0.6 | | μs |
| t_{DH} | Data Out Hold Time | 100 | | ns |

Notes:

1. This parameter is tested initially and after a design or process change that affects the parameter.

POWER UP TIMING ⁽¹⁾⁽²⁾

| Symbol | Parameter | Min | Max | Units |
|------------------|-----------------------------|-----|-----|-------|
| t _{PUR} | Power-up to Read Operation | | 1 | ms |
| t _{PUW} | Power-up to Write Operation | | 1 | ms |

XDCP TIMING

| Symbol | Parameter | Min | Max | Units |
|-------------------|---|-----|-----|-------|
| t _{WRPO} | Wiper Response Time After Power Supply Stable | 5 | 10 | μs |
| t _{WRL} | Wiper Response Time After Instruction Issued | 5 | 10 | μs |

WRITE CYCLE LIMITS

| Symbol | Parameter | Min | Max | Units |
|-----------------|-------------------------------|-----|-----|-------|
| t _{WR} | Write Cycle Time (see Fig. 2) | | 5 | ms |

The write cycle is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

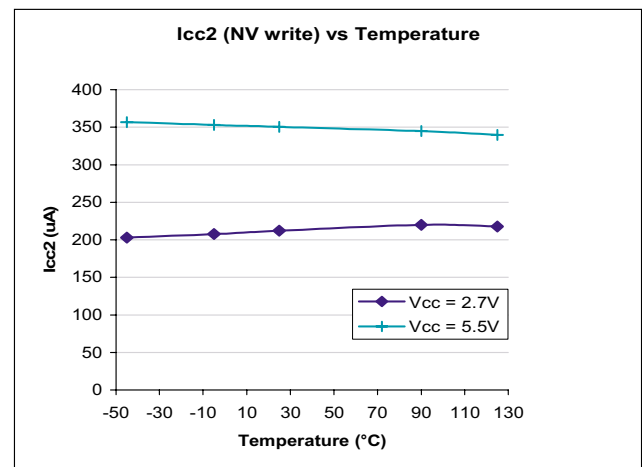
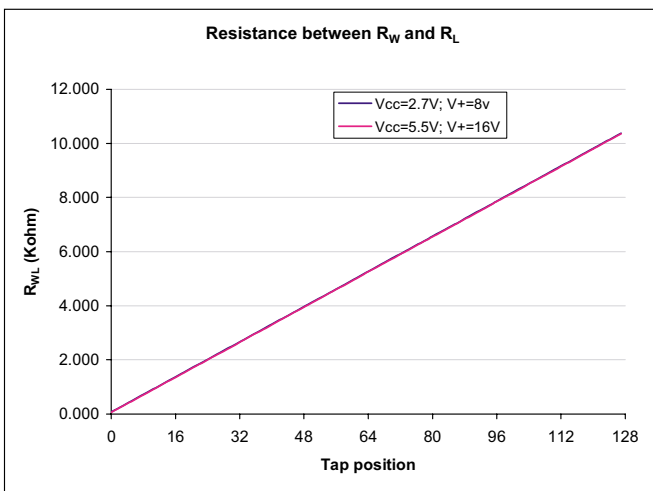
RELIABILITY CHARACTERISTICS

| Symbol | Parameter | Reference Test Method | Min | Max | Units |
|---------------------------------|----------------|-------------------------------|---------|-----|--------|
| N _{END} ⁽¹⁾ | Endurance | MIL-STD-883, Test Method 1033 | 100,000 | | Cycles |
| T _{DR} ⁽¹⁾ | Data Retention | MIL-STD-883, Test Method 1008 | 100 | | Years |

Notes:

1. This parameter is tested initially and after a design or process change that affects the parameter.
2. t_{PUR} and t_{PUW} are the delays required from the time VCC is stable until the specified operation can be initiated.

TYPICAL PERFORMANCE CHARACTERISTICS



TYPICAL PERFORMANCE CHARACTERISTICS (CONT)

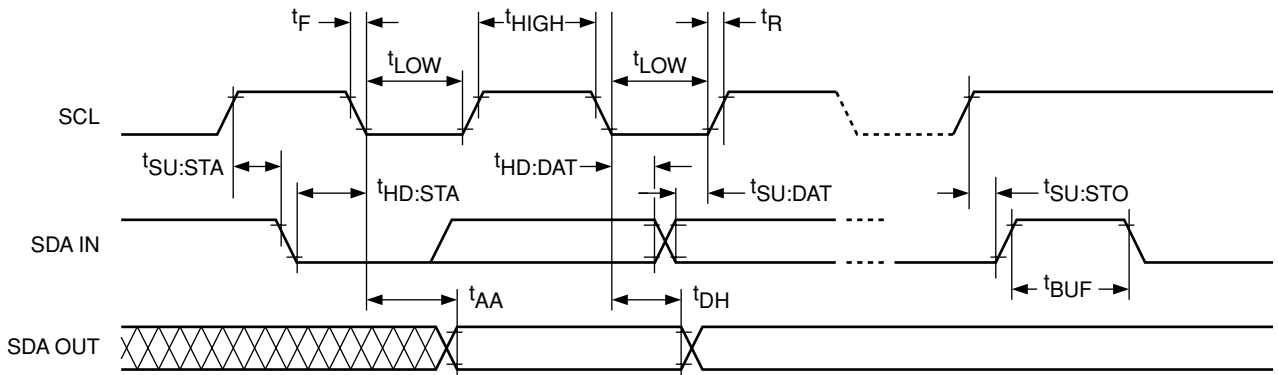
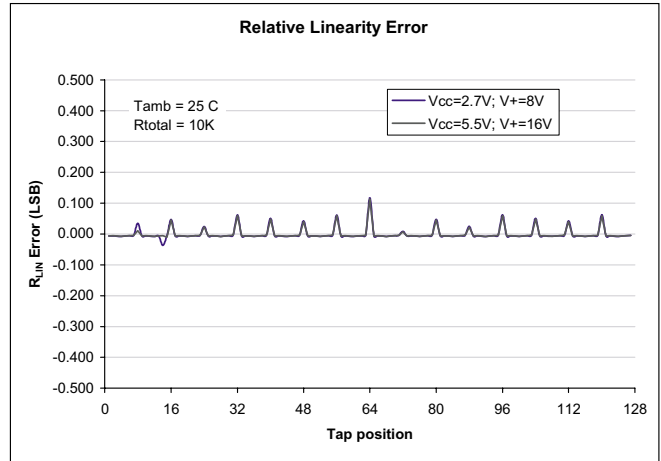
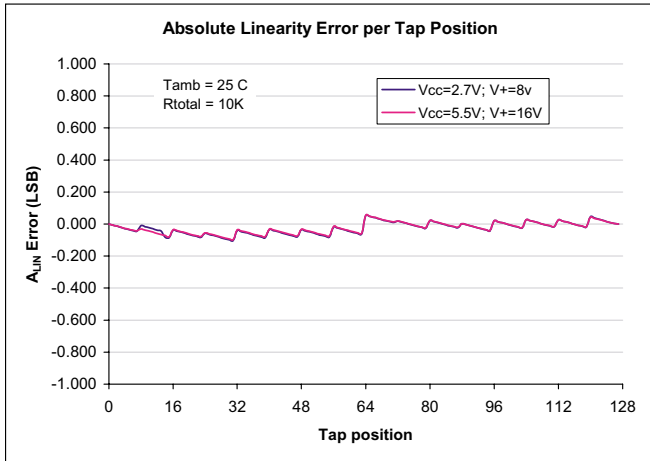


Figure 1. Bus Timing

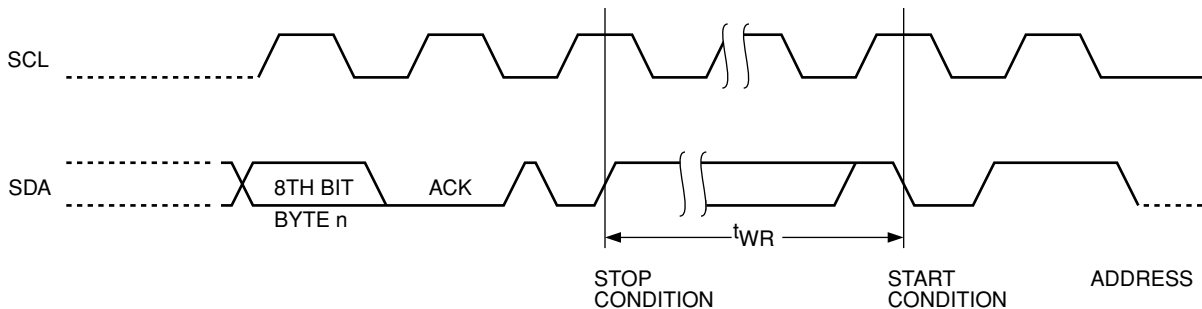


Figure 2. Write Cycle Timing

SERIAL BUS PROTOCOL

The following defines the features of the 2-wire bus protocol:

- (1) Data transfer may be initiated only when the bus is not busy.
- (2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT5132 will be considered a slave device in all applications.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT5132 monitors the SDA and SCL lines and will not respond until this condition is met (see Fig. 3).

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition (see Fig. 3).

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data (see Fig. 4).

The CAT5132 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT5132 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5132 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the STOP condition is issued to indicate the end of the write operation, the CAT5132 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the START condition followed by the slave address. If the CAT5132 is still busy with the write operation, no ACK will be returned. If the CAT5132 has completed the write operation, an ACK will be returned and the host can then proceed with the next instruction operation.

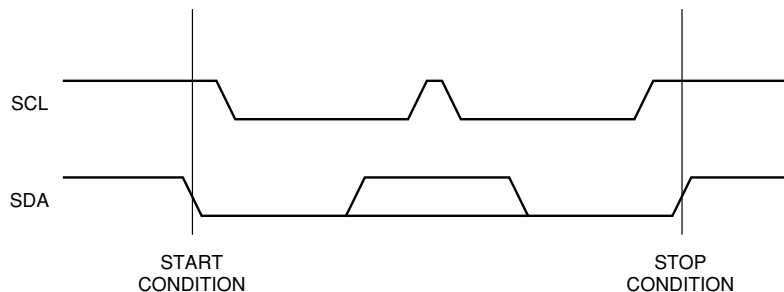


Figure 3. Start/Stop Condition

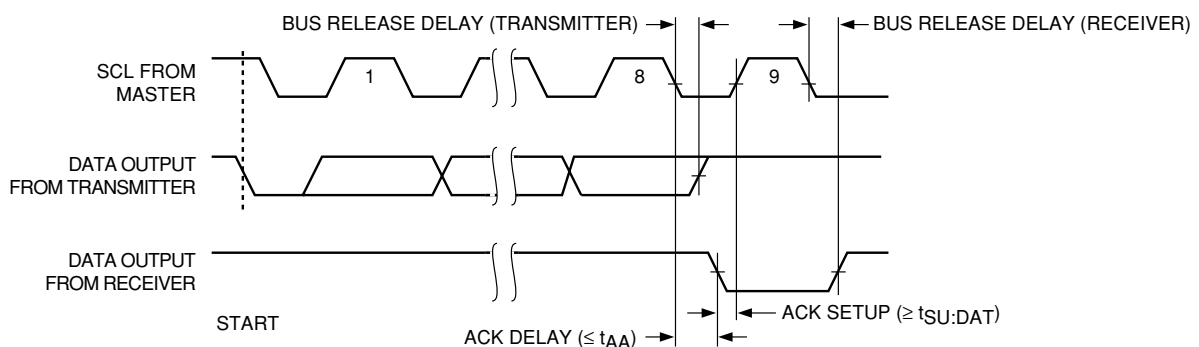


Figure 4. Acknowledge Condition

DEVICE DESCRIPTION

Access Control Register

The volatile register WCR and the non-volatile register DR are accessed only by addressing the volatile Access Register AR first, using the 3 byte I²C protocol for all read and write operations (see Table 1). The first byte is the slave address/instruction byte (see details below). The second byte contains the address (02h) of the AR register. The data in the third byte controls which register WCR (80h) or DR (00h) is being addressed (see Figure 5).

Slave Address Instruction Byte Description

The first byte sent to the CAT5132 from the master processor is called the Slave/DPP Address Byte. The most significant five bits of the slave address are a device type identifier. For the CAT5132 these bits are fixed at 01010 (refer to Table 2).

The next two bits, A1 and A0, are the internal slave address and must match the physical device address which is defined by the state of the A1 and A0 input pins. Only the device with slave address matching the input byte will be accessed by the master. This allows up to 4 devices to reside on the same bus. The A1 and A0 inputs can be actively driven by CMOS input signals or tied to Vcc or Ground.

The last bit is the READ/WRITE bit and determines the function to be performed. If it is a “1” a read command is initiated and if it is a “0” a write is initiated. For the AR register only write is allowed.

After the Master sends a START condition and the slave address byte, the CAT5132 monitors the bus and responds with an acknowledge when its address matches the transmitted slave address.

Table 1. Access Control Register

| START | 1st byte | | | | | | | | | ACK | 2nd byte | | | | | | | ACK | 3rd byte | | | | | | | | ACK | STOP | | | |
|-------|----------|-----|-----|-----|-----|----|----|----|------------------|-----|----------|---|---|---|---|------------------------------|---|-----|----------|---|---|---|---|---|---|---|-----|------|---|----|----|
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | AR address - 02h | | | | | | | WCR(80h) / DR(00h) selection | | | | | | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | SP |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | SP | |

Table 2. Byte 1 Slave Address and Instruction Byte

| Device Type Identifier | | | | | Slave Address | | Read/Write |
|------------------------|-----|-----|-----|-----|---------------|----|------------|
| ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | R/W |
| 0 | 1 | 0 | 1 | 0 | X | X | X |

(MSB) (LSB)

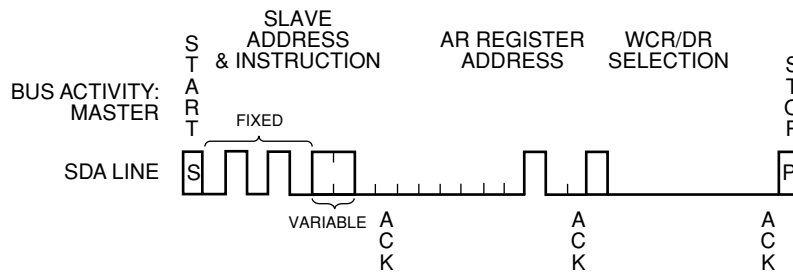


Figure 5. Access Register Addressing Using 3 Bytes

Wiper Control Register (WCR) Description

The CAT5132 contains a 7-bit Wiper Control Register which is decoded to select one of the 128 switches along its resistor array. The WCR is a volatile register and is written with the contents of the nonvolatile Data Register (DR) on power-up. The Wiper Control Register loses its contents when the CAT5132 is powered-down. The

contents of the WCR may be read or changed directly by the host using a READ/WRITE command after addressing the WCR (see Table 1 to access WCR). Since the CAT5132 will only make use of the 7 LSB bits (The first data bit, or MSB, is ignored) on write instructions and will always come back as a “0” on read commands.

A write operation (see Table 3) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a data byte and a STOP condition. After each of the three bytes the CAT5132 responds with an acknowledge. At this time the data is written only to volatile registers, then the device enters its standby state.

Table 3. WCR Write Operation

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----------|-----|-----|-----|-----|----|----|----|-----|------------------|---|---|---|---|---|---|---|-----|--------------------|---|---|---|---|---|---|---|-----|------|---|----|
| START | 1st byte | | | | | | | | ACK | 2nd byte | | | | | | | | ACK | 3rd byte | | | | | | | | ACK | STOP | | |
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | | AR address - 02h | | | | | | | | | WCR(80h) selection | | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | SP |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|--------------------|-----|-----|-----|-----|----|----|----|-----|-------------------|---|---|---|---|---|---|---|-----|--------------------|---|---|---|---|---|---|---|-----|------|---|----|
| START | slave address byte | | | | | | | | ACK | WCR address - 00h | | | | | | | | ACK | data byte | | | | | | | | ACK | STOP | | |
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | | AR address - 02h | | | | | | | | | WCR(80h) selection | | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | X | X | X | X | X | X | X | X | X | X | A | SP |

An increment operation (see Table 4) requires a Start condition, followed by a valid increment address byte (01011), a valid address byte 00h. After each of the two bytes, the CAT5132 responds with an acknowledge. At this time if the data is high then the wiper is incremented or if the data is low the wiper is decremented at each clock. Once the stop is issued then the device enters its standby state with the WCR data as being the last inc/dec position. Also, the wiper position does not roll over but is limited to min and max positions.

Table 4. WCR Increment/Decrement Operation

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----------|-----|-----|-----|-----|----|----|----|-----|------------------|---|---|---|---|---|---|---|-----|--------------------|---|---|---|---|---|---|---|-----|------|---|----|
| START | 1st byte | | | | | | | | ACK | 2nd byte | | | | | | | | ACK | 3rd byte | | | | | | | | ACK | STOP | | |
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | | AR address - 02h | | | | | | | | | WCR(80h) selection | | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | SP |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|--------------------|-----|-----|-----|-----|----|----|----|-----|-------------------|---|---|---|---|---|---|---|-----|------------------------------------|---|---|---|---|---|---|---|------|--|----|
| START | slave address byte | | | | | | | | ACK | WCR address - 00h | | | | | | | | ACK | increment (1) / decrement (0) bits | | | | | | | | STOP | | |
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | | AR address - 02h | | | | | | | | | WCR(80h) selection | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | | | SP |

A read operation (see Table 5) requires a Start condition, followed by a valid slave address byte for write, a valid address byte 00h, a second START and a second slave address byte for read. After each of the three bytes, the CAT5132 responds with an acknowledge and then the device transmits the data byte. The master terminates the read operation by issuing a STOP condition following the last bit of Data byte.

Table 5. WCR Read Operation

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----------|-----|-----|-----|-----|----|----|----|-----|------------------|---|---|---|---|---|---|---|-----|--------------------|---|---|---|---|---|---|---|-----|------|---|----|
| START | 1st byte | | | | | | | | ACK | 2nd byte | | | | | | | | ACK | 3rd byte | | | | | | | | ACK | STOP | | |
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | | AR address - 02h | | | | | | | | | WCR(80h) selection | | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | SP |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|--------------------|-----|-----|-----|-----|----|----|----|-----|-------------------|---|---|---|---|---|---|---|-----|--------------------|---|---|---|---|---|---|---|------|---|----|
| START | slave address byte | | | | | | | | ACK | WCR address - 00h | | | | | | | | ACK | data byte | | | | | | | | STOP | | |
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | | AR address - 02h | | | | | | | | | WCR(80h) selection | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | 0 | X | X | X | X | X | X | X | X | X | SP |

Data Register (DR)

The Data Register (DR) is a nonvolatile register and its contents are automatically written to the Wiper Control Register (WCR) on power-up. It can be read at any time without effecting the value of the WCR. The DR, like the WCR, only stores the 7 LSB bits and will report the MSB bit as a “0”. Writing to the DR is performed in the same fashion as the WCR except that a time delay of up to 5ms is experienced while the nonvolatile store operation is

being performed. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. The WCR is also written during a write to DR. After a DR WRITE is complete the DR and WCR will contain the same wiper position.

To write or read to the DR, first the access to DR is selected, see table 1 then the data is written or read using the following sequences.

A write operation (see Table 6) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a data byte and a STOP condition. After each of the three bytes the CAT5132 responds with an acknowledge. At this time the data is written both to volatile and non-volatile registers, then the device enters its standby state.

Table 6. DR Write Operation

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----------|-----|-----|-----|-----|----|----|----|-----|------------------|---|---|---|---|---|---|---|-----|-------------------|---|---|---|---|---|---|---|-----|------|----|
| START | 1st byte | | | | | | | | ACK | 2nd byte | | | | | | | | ACK | 3rd byte | | | | | | | | ACK | STOP | |
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | | AR address - 02h | | | | | | | | | DR(00h) selection | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | SP |

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|--------------------|---|---|---|---|---|---|---|-----|------------------|---|---|---|---|---|---|---|-----|-----------|---|---|---|---|---|---|---|-----|------|----|
| START | slave address byte | | | | | | | | ACK | DR address - 00h | | | | | | | | ACK | data byte | | | | | | | | ACK | STOP | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | X | X | X | X | X | X | X | X | X | A | SP |

A read operation (see Table 7) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a second Start and a second slave address byte for read. After each of the three bytes the CAT5132 responds with an acknowledge and then the device transmits the data byte. The master terminates the read operation by issuing a STOP condition following the last bit of Data byte.

Table 7. DR Read Operation

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------|----------|-----|-----|-----|-----|----|----|----|-----|------------------|---|---|---|---|---|---|---|-----|-------------------|---|---|---|---|---|---|---|-----|------|----|
| START | 1st byte | | | | | | | | ACK | 2nd byte | | | | | | | | ACK | 3rd byte | | | | | | | | ACK | STOP | |
| | ID4 | ID3 | ID2 | ID1 | ID0 | A1 | A0 | Wb | | AR address - 02h | | | | | | | | | DR(00h) selection | | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A | SP |

| | | | | | | | | | | | | | | | | | | | |
|-------|--------------------|---|---|---|---|---|---|---|-----|------------------|---|---|---|---|---|---|---|--|------|
| START | slave address byte | | | | | | | | ACK | DR address - 00h | | | | | | | | | |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| START | slave address byte | | | | | | | | | data byte | | | | | | | | | STOP |
| ST | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | A | 0 | X | X | X | X | X | X | X | | SP |

POTENTIOMETER OPERATION

Power-On

The CAT5132 is a 128-position, digital controlled potentiometer. When applying power to the CAT5132, V_{CC} must be supplied prior to or simultaneously with $V+$. At the same time, the signals on R_H , R_W and R_L terminals should not exceed $V+$. If $V+$ is applied before V_{CC} , the electronic switches of the DPP are powered in the absence of the switch control signals, that could result in multiple switches being turned on. This causes unexpected wiper settings and possible current overload of the potentiometer. When V_{CC} is applied the device turns on at the mid-point wiper location (64) until the wiper register can be loaded with the nonvolatile memory location previously stored in the device. After the nonvolatile memory data is loaded into the wiper register the wiper location will change to the previously stored wiper position.

At power-down, it is recommended to turn-off first the signals on R_H , R_W and R_L , followed by $V+$ and, after that, V_{CC} , in order to avoid unexpected transmissions of the wiper and uncontrolled current overload of the potentiometer.

The end-to-end nominal resistance of the potentiometer has 128 contact points linearly distributed across the total resistor. Each of these contact points is addressed by the 7 bit wiper register which is decoded to select one of these 128 contact points.

Each contact point generates a linear resistive value between the 0 position and the 127 position. These values can be determined by dividing the end-to-end value of the potentiometer by 127. In the case of the

10k Ω potentiometer $\sim 79\Omega$ is the resistance between each wiper position. However in addition to the $\sim 79\Omega$ for each resistive segment of the potentiometer, a wiper resistance offset must be considered. Table 8 shows the effect of this value and how it would appear on the wiper terminal.

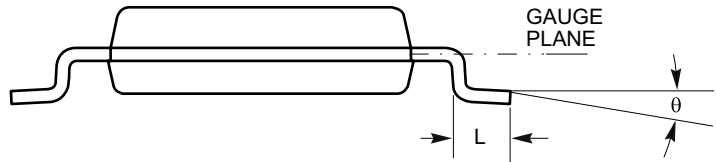
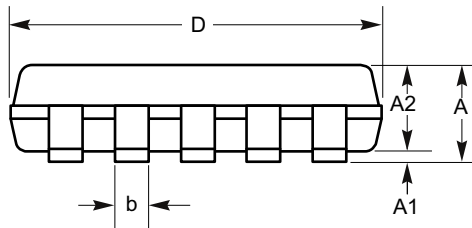
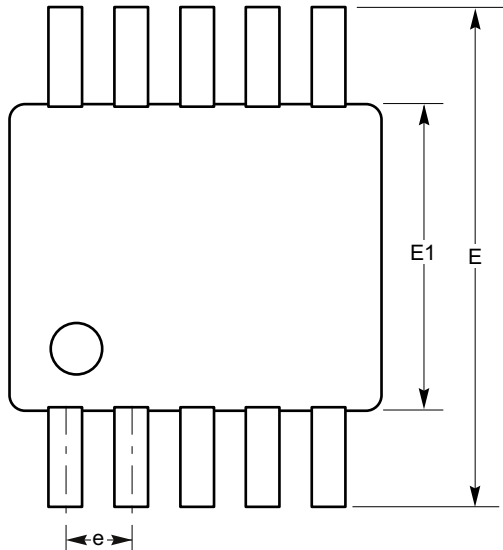
This offset will appear in each of the CAT5132 end-to-end resistance values in the same way as the 10k Ω example. However resistance between each wiper position for the 50k Ω version will be $\sim 395\Omega$ and for the 100k Ω version will be $\sim 790\Omega$.

Table 8. Potentiometer Resistance and Wiper Resistance Offset Effects

| Position | Typical R_w to R_L Resistance for 10k Ω DPP | |
|----------|--|-------------------------------|
| 00 | 70 Ω or | 0 Ω + 70 Ω |
| 01 | 149 Ω or | 79 Ω + 70 Ω |
| 63 | 5,047 Ω or | 4,977 Ω + 70 Ω |
| 127 | 10,070 Ω or | 10,000 Ω + 70 Ω |
| | | |
| Position | Typical R_w to R_H Resistance for 10k Ω DPP | |
| 00 | 10,070 Ω or | 10,000 Ω + 70 Ω |
| 64 | 5,047 Ω or | 4,977 Ω + 70 Ω |
| 126 | 149 Ω or | 79 Ω + 70 Ω |
| 127 | 70 Ω or | 0 Ω + 70 Ω |

PACKAGE OUTLINES

10-LEAD MSOP



| SYMBOL | MIN | NOM | MAX |
|--------|----------|------|------|
| A | | | 1.10 |
| A1 | 0.00 | 0.05 | 0.15 |
| A2 | 0.75 | 0.85 | 0.95 |
| b | 0.17 | | 0.27 |
| D | 2.90 | 3.00 | 3.10 |
| E | 4.75 | 4.90 | 5.05 |
| E1 | 2.90 | 3.00 | 3.10 |
| e | 0.50 BSC | | |
| L | 0.40 | | 0.8 |
| θ | 0° | | 8° |

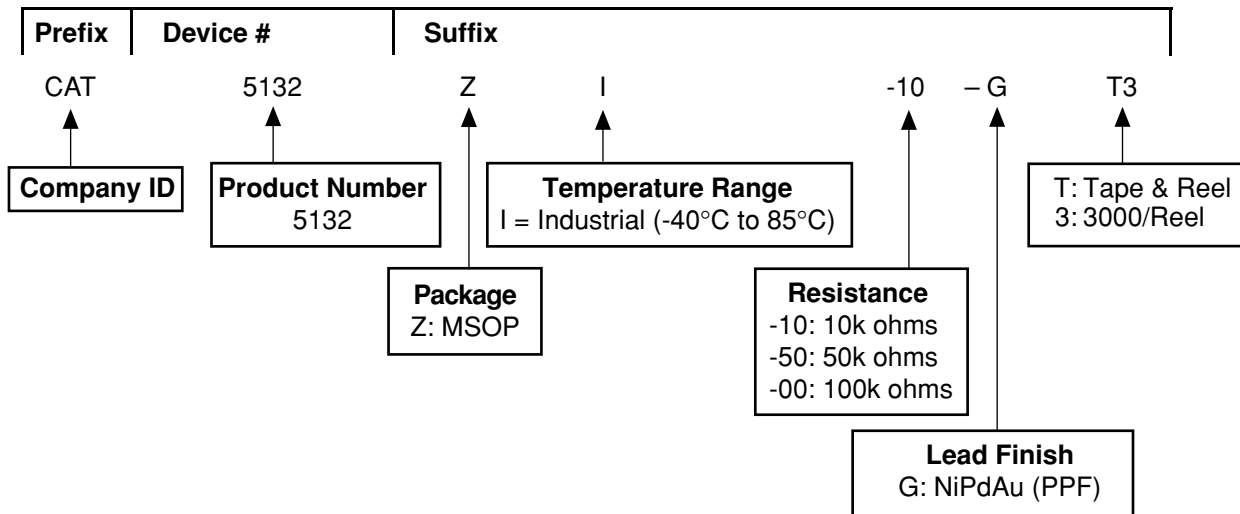
10-lead_MSOP.eps

**For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.**

Notes:

1. All dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC Specification MO-187.
3. Stand off height/coplanarity are considered as special characteristics.

EXAMPLE OF ORDERING INFORMATION



Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a CAT5132ZI-10-GT3 (MSOP, Industrial Temperature range, 10k ohms, NiPdAu, Tape & Reel).
- (4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

| Ordering Part Number |
|----------------------|
| CAT5132ZI-10-GT3 |
| CAT5132ZI-50-GT3 |
| CAT5132ZI-00-GT3 |

REVISION HISTORY

| Date | Rev. | Reason |
|------------|------|---|
| 09/12/2005 | 00 | Initial Issue |
| 01/18/2006 | 01 | Update Ordering Information |
| 03/24/2006 | 02 | Update Features Update Description Update Pin Description Update Absolute Maximum Ratings Update Recommended Operating Conditions Update Ordering Information Update Absolute Maximum Ratings Update Reliability Characteristics Update Potentiometer Operation |
| 08/11/06 | 03 | Update Title Update Potentiometer Characteristics Update D. C. Electrical Characteristics Update Typical Performance Characteristics Update Package Outline Update Example of Ordering Information |
| 11/01/06 | 04 | Update Potentiometer Operation Update Example of Ordering Information |

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