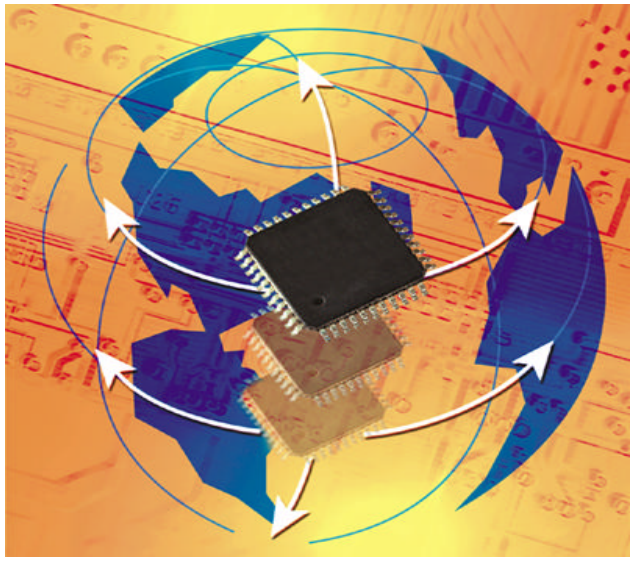
Qualification Package

AT89C51ED2

FLASH 8-bit C51 Microcontroller

64 Kbytes FLASH, 2 Kbytes EEPROM



AT89C51RD2 / AT89C51ED2

JULY 2003

1 Table of contents

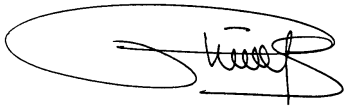
2 General Information

Product Name:	AT89C51RD2
Function:	8-bit Microcontroller with 64 Kbytes FLASH SPI Interface
Product Name:	AT89C51E2
Function:	8-bit Microcontroller with 64 Kbytes FLASH, 2 Kbytes EEPROM SPI Interface
Wafer Process:	Logic CMOS 0.35 um with embedded FLASH
Available Package Types	PLCC 44, VQFP 44, PLCC 68, VQFP 68 ,PDIL 40
Other Forms:	Die, Wafer

Locations:

Process Development,	Atmel Colorado Springs, USA
Product Development	Atmel Nantes, France
Wafer Plant	Atmel Colorado Springs, USA
QC Responsibility	Atmel Nantes, France
Probe Test	Atmel Colorado Springs, USA
Assembly	Depending on package
Final Test	Atmel TSTI Manila, Philippines
Lot Release	Atmel Nantes, France
Shipment Control	Global Logistic Center, Philippines
Quality Assurance	Atmel Nantes, France
Reliability Testing	Atmel Nantes, France
Failure Analysis	Atmel Nantes, France

Quality Management
Atmel Nantes, France



Signed: Pascal LECUYER

3 Technology Information

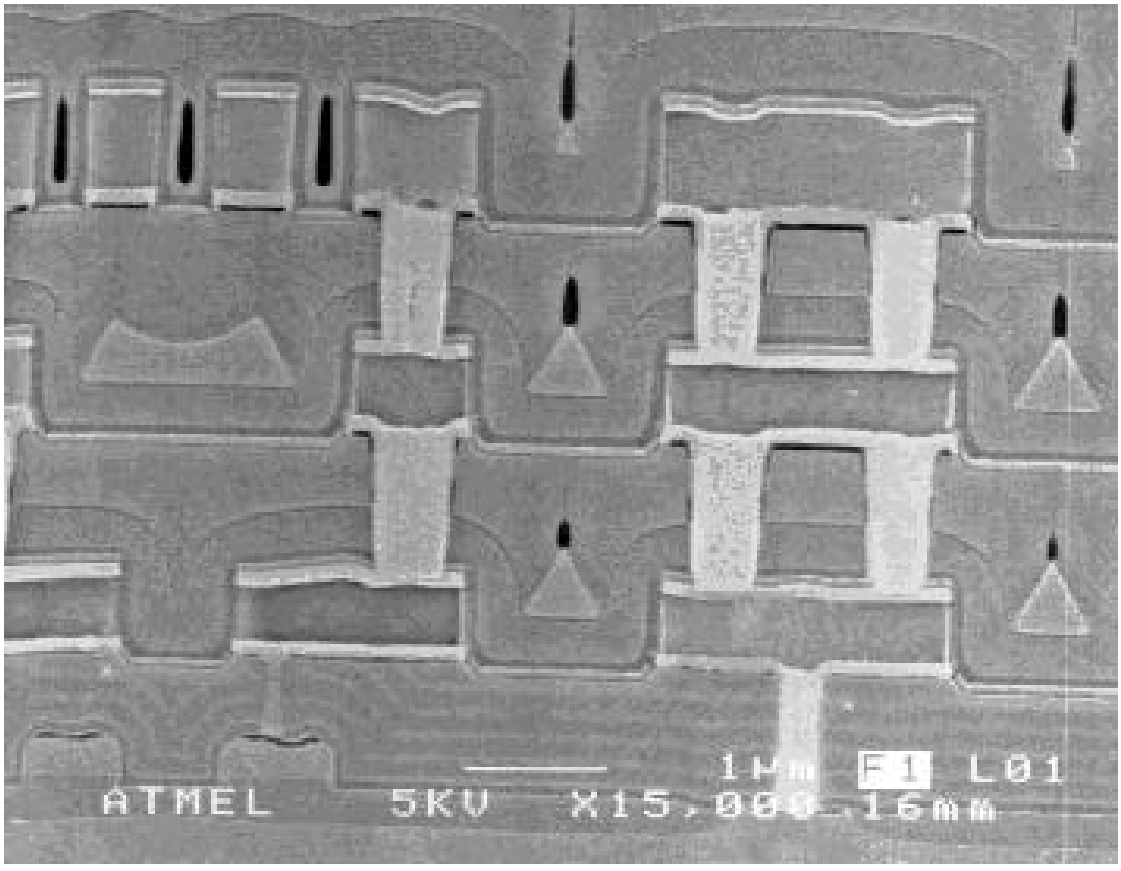
3.1 Wafer Process Technology

Process Type (Name):	Logic 0.35um with embedded FLASH (AT56800)
Base Material:	Epitaxied Silicon
Wafer Thickness (final)	475 um
Wafer Diameter	150 mm
Number Of Masks	27
Gate Oxide (Logic transistors)	
Material	Silicon Dioxide
Thickness	68A
Gate Oxide (EPROM cell)	
Material	Silicon Dioxide
Thickness	390A
Polysilicon	
Number of Layers	2
Thickness Poly 1	1400A Amorphous
Thickness Poly 2	3200A
Metal	
Number of Layers	3
Material:	Aluminum Copper
Layer 1 Thickness	5000A
Layer 2 Thickness	5000A
Layer 3 Thickness	8000A
Passivation	
Material	Oxide HDP/ Oxy-nitride
Thickness	21000A

3.2 Product Design

Die Size	17,9 mm^2
Pad Size Opening / Pitch	66 um * 66 um / 111 um
Logic Effective Channel Length	0.35 µm
Gate Poly Width (min.)	0.35 µm
Gate Poly Spacing (min.)	0.42 µm
Metal 1 Width	0.42 µm
Metal 1 Spacing	0.49 µm
Metal 2 Width	0.56 µm
Metal 2 Spacing	0.49 µm
Metal 3 Width	0.56 µm
Metal 3 Spacing	0.49 µm
Contact Size	0.35 µm
Contact Spacing	0.42 µm
Via 1 Size	0.42 µm
Via 2 Size	0.42 µm

3.3 Device cross section



AT56Kxx cross section

4 Qualification

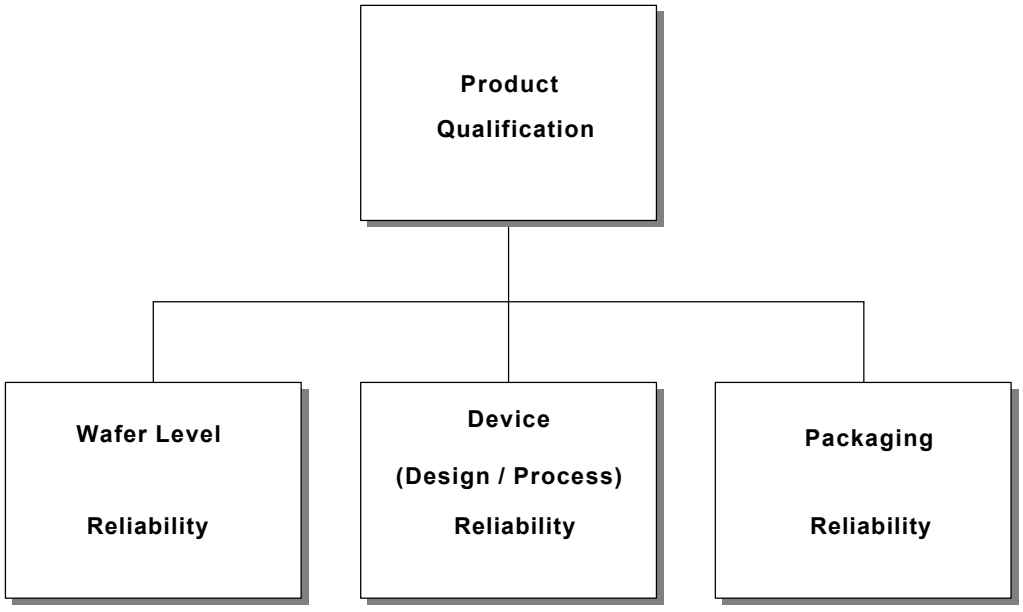
4.1 Qualification Methodology

All product qualifications are split into three distinct steps as shown below. Before a product is released for use, successful qualification testing are required at wafer, device and package level.

- Wafer Level Reliability consists in testing individually basic process modules regarding their well known potential limitations (Electro-migration, Hot Carriers Injection, Oxide Breakdown, NVM Data Retention). Each test is performed using wafer process specific structures.

- Device reliability is covering either dice design and processing aspects. The tests are performed on device under qualification, but generic data may also be considered for reliability calculation.

- For each package type proposed in the Datasheet, it is verified that qualification data are available. If not qualification tests are carried out for the new package types. In addition, one package type is selected to verify packaging reliability of the device under qualification.



4.2 Qualification Test Methods

General Requirements for Plastic packaged CMOS ICs:

Standard	Test Description	Acceptance
MIL-STD 883 Method 1005	**Electrical Life Test (Early Failure Rate)** 48 hours 140°C	0/300 - 48h
MIL-STD 883 Method 1005	**Electrical Life Test (Latent Failure Rate)** 1000 hours 140°C Dynamic or Static	0/100 - 500h
MIL-STD 883 Method 3015.7	**Electrostatic Discharge HBM** +/-2000v 1.5kOhm/100pF/3 pulses	0/3 per level
JEDEC 78	**Latch up** 50mW power injection, 50% overvoltage @125°C	0/5 per stress
AEC Q100 Method 005	**NVM Endurance** Program Erase Cycles 25°C	0/50 - 10kc
AEC Q100 Method 005	**NVM Data Retention** High Temperature Storage 165°C	0/50 - 500h
MIL-STD 883 Method 1010	**Temperature Cycling** 1000 cycles –65°C/150°C air/air	0/50 - 500c
Atmel PAQA0184	**HAST after Preconditioning** 144 hours 130°C/85%RH	0/50 – 96h
EIA JESD22-A101	**85/85 Humidity Test** 1000 hours 85°C/85%RH	0/50 - 500h
EIA JESD22-A110	**HAST** 336 hours 130°C/85%RH	0/50 - 168h
EIA JEDEC 20-STD	**Preconditioning** Soldering Stress 220°C/235°c/3 times	0/11 per class
MIL-STD 883 Method 2003	**Solderability**	0/3
MIL-STD 883 Method 2015	**Marking Permanency**	0/5

4.3 Wafer Level Reliability

4.3.1 Electromigration

Purpose:

To evaluate the AT56800, AT35500, and AT37000 processes for Metal 1, Metal 3 & Via Electromigration Reliability. These 3 processes have the same steps for interconnect levels.

Test Parameters:

Metal 1 & Metal 3:
Sample Size = 15
Temp = 250C with Joule heating .
J = 3.5E06 A/cm2.

Via:
Sample Size = 15
Temp = 200C with Joule heating.
J = 2.5E06 A/cm2.

Black's Equation Parameters:

Failure Criteria - 10% increase in resistance. Data taken every 1% change.
n = 2
Ea = 0.6eV

Lifetime Predictions:

Metal 1 :
Split 1 - $Tf_{.1\%\ exp}$ = ~ 28 hrs $Tf_{.01\%\ op}$ = ~ 28 hrs x 39706 accel = **127 years**.
(Sigma = 2.7118 hours, $Accel_{temp}$ = 130, $Accel_{current}$ = 306)

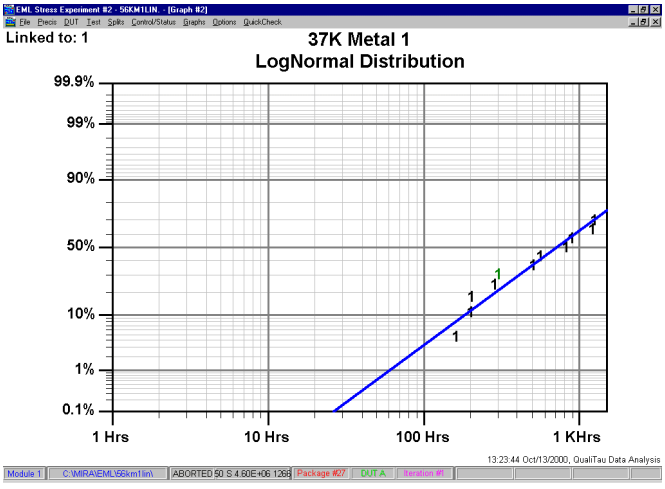
Metal 3 :
Split 3 - $Tf_{.1\%\ exp}$ = ~ 140 hrs $Tf_{.01\%\ op}$ = ~ 140 hrs x 39706 accel = **634 years**.
(Sigma = 1.8782 hours, $Accel_{temp}$ = 130, $Accel_{current}$ = 306)

VIA :
Split 4 - $Tf_{.1\%\ exp}$ = ~ 22 hrs $Tf_{.1\%\ op}$ = ~ 22 hrs x 7144 accel = **18 years**.
(Sigma = 2.59 hours, $Accel_{temp}$ = 31.75, $Accel_{current}$ = 225) (9/15 fails)

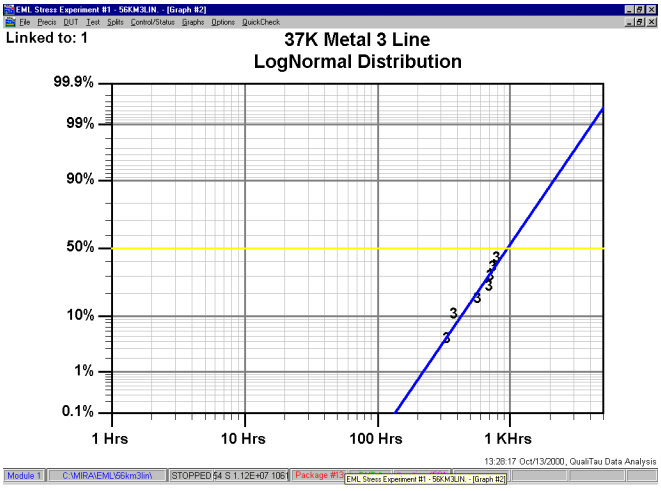
Conclusion:

All splits pass the minimum 10 years lifetime.

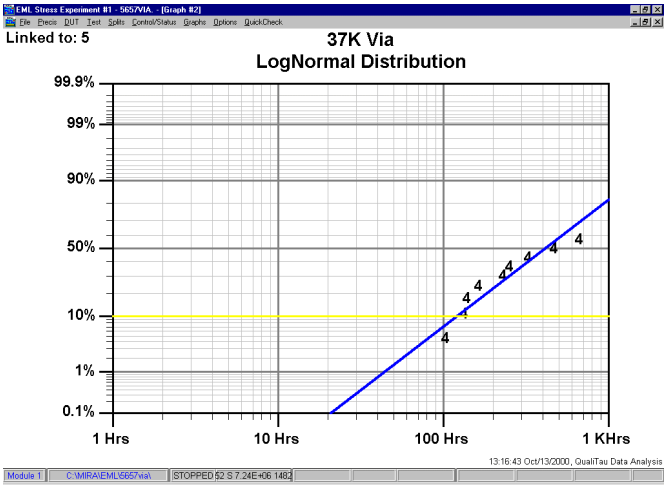
Test results :



AT56800 metal 1 results



AT56800 metal 3 results



AT56800 VIA results

Electromigration summary table:

Level	Sample Size	Fails @ 10%	Tf.1% Lifetime (yrs)
M1	15	9	140
M3	15	7	1088
Via	15	9	19

4.3.2 Hot Carriers Injection

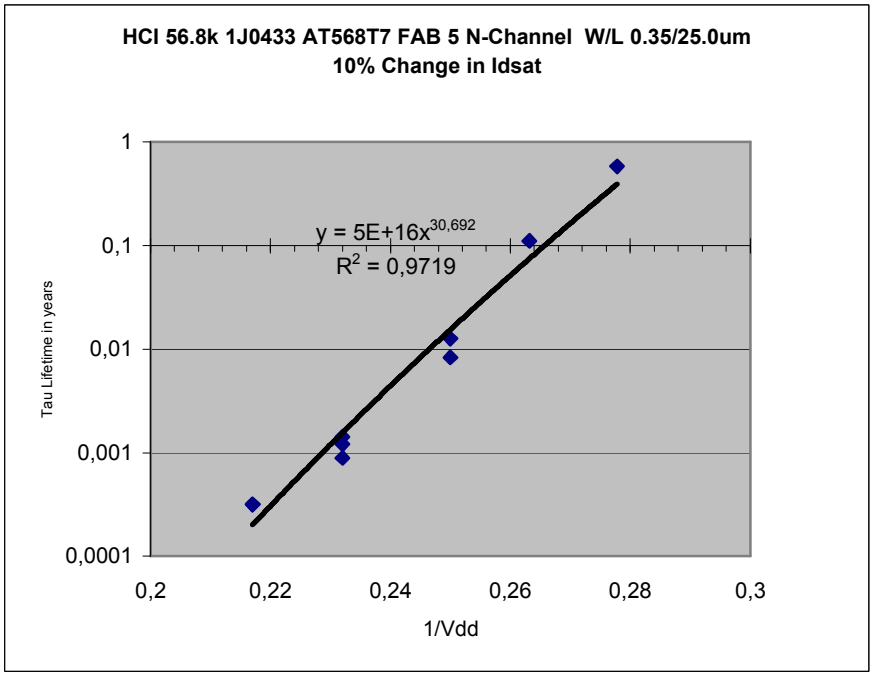
Test conditions

The test is performed by forcing a high drain bias on the test device (Vds>Vddmax) to accelerate the carriers to the maximum. At the same time the gate bias (Vgs) is chosen in order to maximize the injection of carriers into the gate oxide and also the substrate. WLR_B n-channel W/L 0.35um/25um the stress is performed on a number of transistors, each at a different stress condition Vds,stress and Vgs,stress. For each transistor, the time to reach the failure criteria (dIdsat/Idsat=10%) is obtained. NMOS is more sensitive to hot carriers compared to PMOS. Consequently NMOS is the only structure tested.

Measurement

AT568T7 lot 1J0433 has been measured using the WLR_B hot electron structure with standard drain.
NMOS W/L = 25/0.35 um.

Results



Conclusion

The extrapolated life time in the worst case conditions (@Vds=Vdd max & Vgs set to maximize substrate current) is much greater than 0.2 years in DC mode (qualification requirement) which is equivalent to more than 10 years in AC mode.

4.3.3 Time Dependent Dielectric Breakdown

Purpose:

To evaluate the AT56800 thin gate oxide TDDB performance as follows:

a) To determine the activation energy of gate oxide failures on STI active edge capacitors
b) To determine the field acceleration factor for intrinsic gate oxide failures
c) To determine the sigma the lognormal standard deviation of the time to breakdown distribution of the intrinsic gate oxide

Test Parameters:

Lot 9G3470 (wafers 4, 5, 18)
Min thickness: 72.9A
Max thickness: 74.7A
Capacitor size: 6.267 um^2

The stress conditions used are shown below:

Temperature/Field	9.5MV/cm	10.0MV/cm	10.5MV/cm
225C	N=5	N=5	N=5
200C	N=5	N=5	N=5
175C	N=5	N=5	N=6

Accumulated total stress time: 132 hours / 46 capacitors

Calculation Parameters:

Failure Criteria: 0.01% failures
Temp/Voltage use: 105°C / 3.3V
Oxide thickness: 63A (target –10%)

Lifetime Prediction:

The equation used to describe the breakdown of gate oxides is:

$Tbd(i) = \exp(SIGMA*Z(i) + GAMMA*Eox + Ea/kT + T0)$

Where
Tbd(i) is the time to breakdown of the i^{th} capacitor,
SIGMA is the lognormal standard deviation of the breakdown distribution,
Z(i) is the Z-score of the i^{th} capacitor (essentially the difference between its breakdown time and the mean measured in standard deviations),
GAMMA is the Field acceleration constant,
Eox is the oxide field,
Ea is the activation energy of this failure mechanism,
K is Boltzmann's constant,
T is the Kelvin Temperature, and
T0 is a fitting constant.

The best fit coefficients in the regression analysis are:

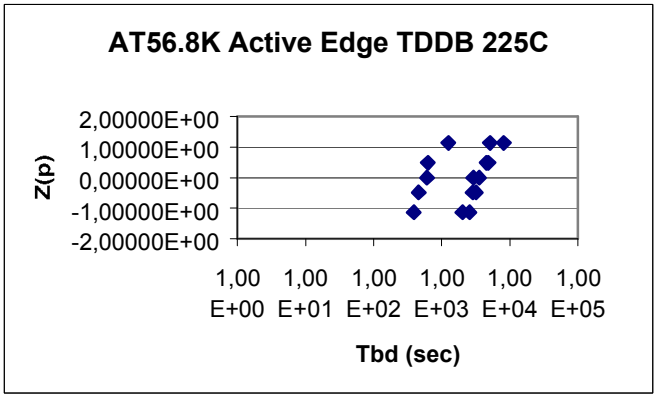
T0= 14.25034317 LN-sec
Ea= 1.060043152 eV
GAMMA= -3.2454227 LN-sec-cm/MV
SIGMA= 0.414655753 LN-sec

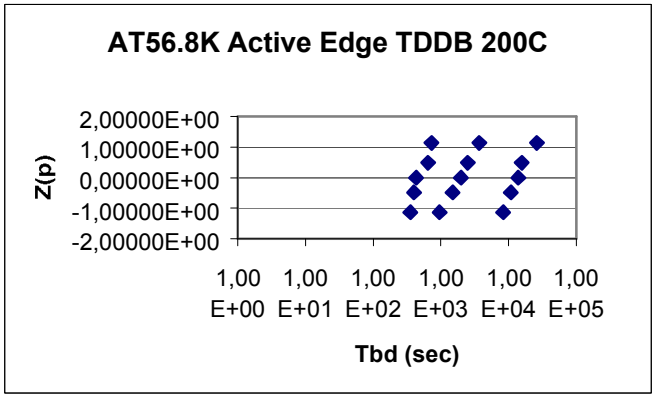
with an adjusted r-squared of 97.99%. The intrinsic lifetime at use conditions calculated from this regression is 56174 years.

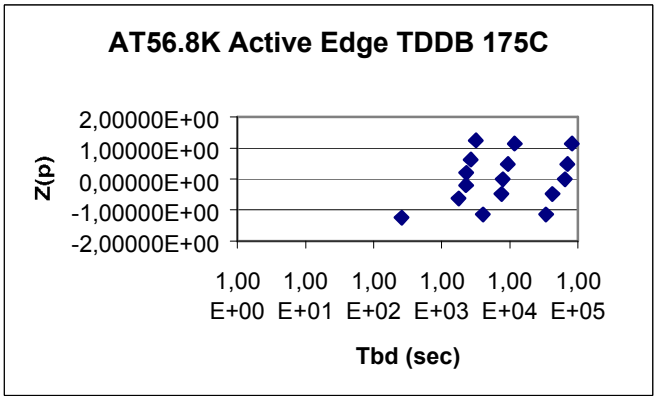
Conclusion:

Using the coefficients determined above, the time to reach any cumulative percent failure level can be estimated given the stress conditions. Using 105C and 3.3 volts on 63 Angstrom N-Channel gate2 oxide, we may expect 0.01% of capacitors having 6,267 square microns area with 6,174 microns of active edge to fail in about 613 years, exceeding the technology requirement of ten years.

Test results :







4.3.4 FLASH Characteristics

4.3.4.1 Cell endurance

Purpose:

To evaluate the ability of memory cell to withstand high number of program/erase cycles without change of electrical characteristics.

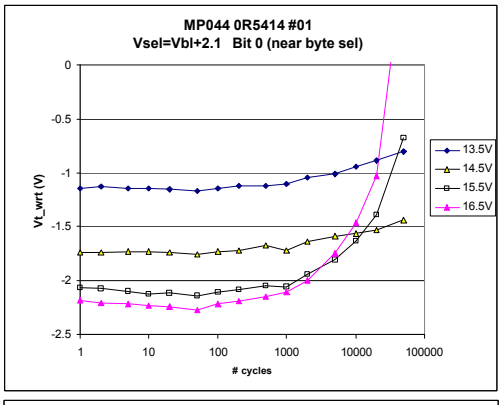
Test Parameters:

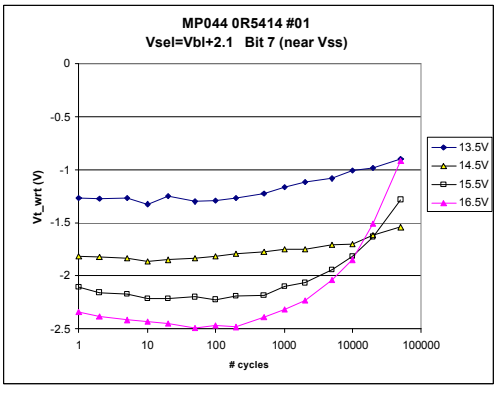
Measurements have been done on lot 0R5414.
Test done on 2 cells in a byte :

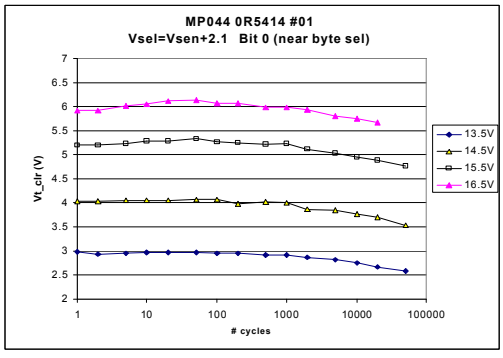
- cell near byte select transistor, called bit0 (1st column)
- cell near Vss contact, called bit 7 (8th column).

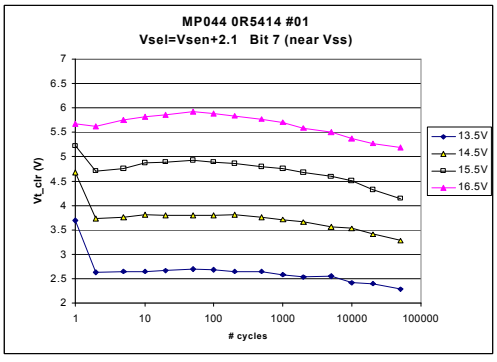
Cycling is done for various programming voltages :

- write :	13.5V on BL / 15.6V on select	- clear :	13.5V on sense / 15.6V on select
@5ms	14.5V on BL / 16.6V on select	@5ms	14.5V on sense / 16.6V on select
	15.5V on BL / 17.6V on select		15.5V on sense / 17.6V on select
	16.5V on BL / 17.6V on select		16.5V on sense / 17.6V on select









Conclusions:

- Vt_wrt shift of 200 mV after 10k cycles
- I_read decrease of 2.5 uA after 10kcycles (- 7 to 9 %)
- No big difference between bit0 and bit 7 in terms of Vt or current variations Using the coefficients

4.3.4.2 Cell retention

Purpose:

To extrapolate cell life duration at 125°C from bake measurements at high temperature.

Test parameters:

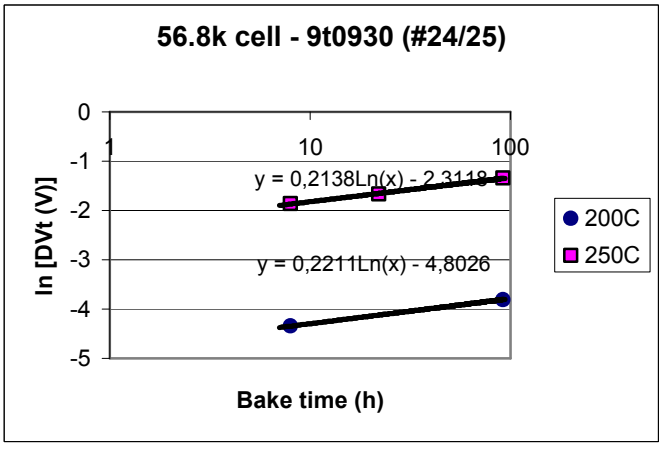
Lot: 9T0930
Temperature: 250°C and 200°C
Duration: 92 hours

Lifetime Prediction:

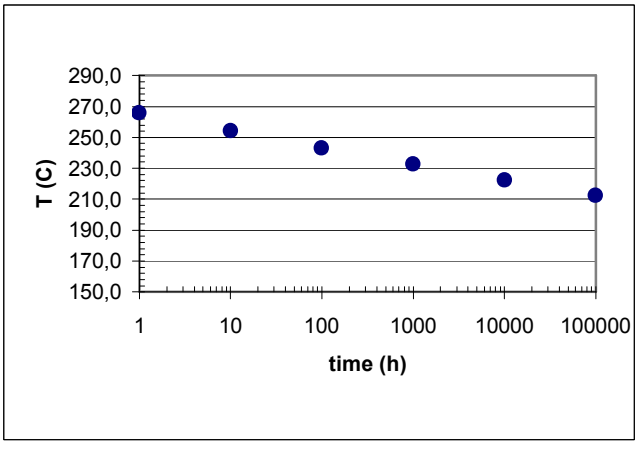
The equation used to describe memory cell retention is:

DVt (V) = A * (t[h])^m * exp (-1.05eV/kT[K])

Results :



Test measurements



Extrapolated Life Time

Conclusions :

Extrapolation to 125°C - 10years = Vt loss is less than 0.8 mV

4.3.4.3 Cell Read Disturb

Purpose:

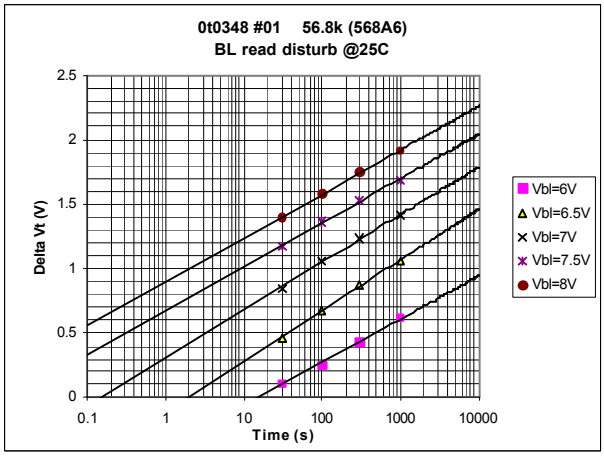
To measure read disturb influence on 56k8 memory cell.

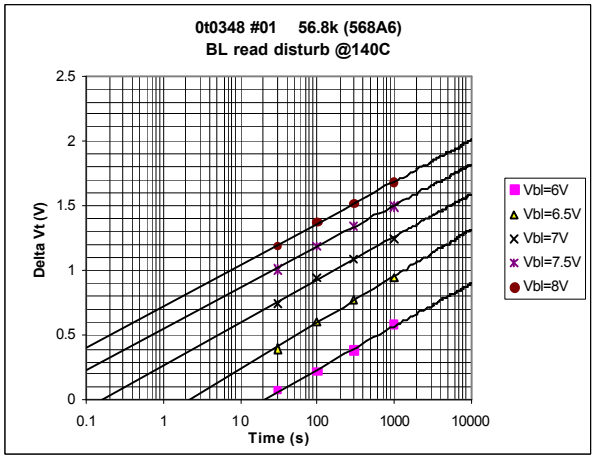
Test parameters:

Lot: 0t0348
Programming: 14V on WL and sensegate @5ms
Temperature: 25°C and 140°C

The cell is stressed with BL voltage much higher than standard read conditions (around 6V) to accelerate disturb phenomenon : electrons from the Floating gate can move through the tunnel oxide. This charge loss is measured after stress by a Vt measurement.

Test results:





Conclusion:

Extrapolation to 10 years lifetime give a maximum BL voltage of around 4V in read operation, which is much higher than nominal BL read voltage (~1V). So there is no sensitivity to read disturb either at room temperature or high temperature.

4.3.4.4 Wafer probe Data retention measurement

Data retention has been verified after bake for 168 hours at 250°C on 3 wafers of a standard production lot. The results are summarized in the table below:

Lot	Wafer	% Retention loss	Failure rate extrapolation at 55°C	Time to failure
1G4448	6	0%	3.91fit	>> 10 years
1G4448	8	0%	4.19fit	>> 10 years
1G4448	12	0%	3..96fit	>> 10 years
Total		0%	1.34fit	>> 10 years

Conclusion:

Data Retention measurements at wafer probe stand out high data retention capability of AT56800 products, exceeding the technology requirement of ten years.

4.4 Device Reliability

4.4.1 Operating Life Testing

AT89C51ED2 test results are summarized in the table below.

Lot	Device Type	Test Description	Step	Result	Comment
A01948K	AT89C51ED2 PLCC 44	EFR Dynamic Life Test	12h 48h	0/300 0/300	
		LFR Dynamic Life Test	500h 1000h	0/100 0/100	

4.4.2 ESD / Latch-up

AT89C51ED2 test results are summarized in the table below.

Lot	Device Type	Test Description	Step	Result	Comment
A01948	AT89C51ED2 PLCC 44	ESD-HBM Model	2000V 3000V 4000V 5000V	0/3 1/3 1/3 1/3	Class 2 of MIL STD 883
		LATCH-UP Over-Voltage Power Injection	5.5v 50mW	0/5 0/5	Test done at 125°C Classified latch-up free

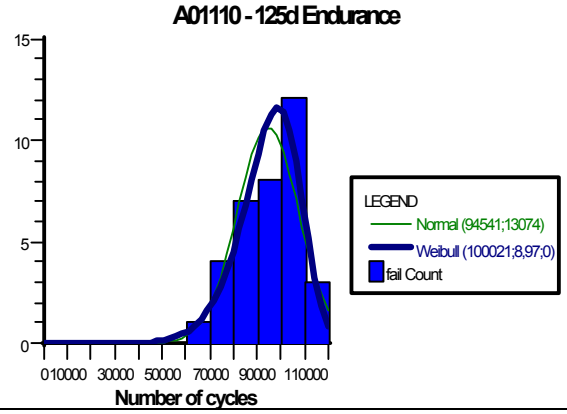
4.4.3 FLASH and EEPROM Data Retention and Endurance Cycling

AT89C51ED2 test results are summarized in the table below.

Lot	Device Type	Test Description	Step	Result	Comment
A01948K	AT89C51ED2 PLCC 44	Data Retention	500h 1000h	0/50 0/50	
		Program / Erase Endurance Cycling	100kc	0/30	32k USER memory
		Program / Erase Endurance Cycling	100kc	0/30	2k DATA memory

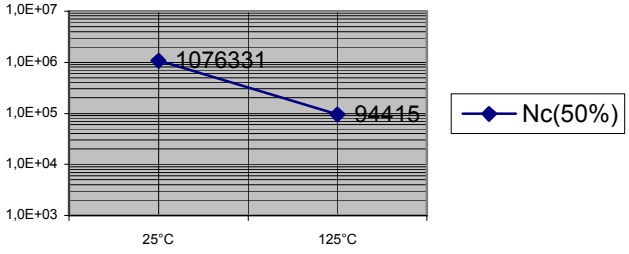
AT56800 Program / Erase Endurance:

Temperature acceleration factor calculation:



16K FLASH Program Erase Endurance: Typical 125d distribution

Endurance Temperature Acceleration
T89C51CC02 - A01013L



Temperature effect on 16K FLASH Program / Erase

$A_{T(125d/25d)}$ = 11.8 - Ea = 0.25eV

AT56800 FLASH / EEPROM Reliability Calculation:

Global Calculation	AT56800 Microcontrollers	Data-Retention Test	165°c 250°c	0/1101000 0/251496	For current sample size expressed in device*hours, Ea = 0.7eV, CL = 60%, T = 55°: ?$_{DR}$ = 0.29 fit
		Endurance Cycling	55°c	1/109850k	Failure : 1 bit charge loss For sample size expressed in equivalent cycles at 55°c, and assuming one cycle per day, Ea = 0.25eV, CL = 60%: ?$_{EC}$ = 0.76 fit

4.4.4 AT89C51ED2 Operating Reliability Calculation

In the next table, it is proposed a AT89C51ED2 reliability prediction calculated at 55°c for 60% confidence level from generic test data collected over the 12 last months process monitor.

Lots	Device Type	Test Description	Step	Result	Comment
A00648 P01709 A00988B A01459A A01460E A01615B	T89C51CC01 VQFP 44	EFR Dynamic Life Test	48h	0/3787	
		LFR Dynamic Life Test	1000h	0/266	
A01110C A01110D A01185F A01366E	T89C51CC02 SOIC28	EFR Dynamic Life Test	48h	1/1260	1 Ipd drift caused by scratch on metal 1
		LFR Dynamic Life Test	1000h	0/280	
A01679A A01679B	T89C51RC2 PLCC 44	EFR Dynamic Life Test	48h	0/1856	
		LFR Dynamic Life Test	1000h	0/100	
A00808A A00943E	T89C51RB2 PLCC 44	EFR Dynamic Life Test	48h	0/300	
		LFR Dynamic Life Test	1000h	0/100	
A01487Q A02179	T85C5121 T89C5121 SSOP24	EFR Dynamic Life Test	48h	0/684	
		LFR Dynamic Life Test	1000h	0/100	
A01435H A01435K A02293C	AT89C5114 SOIC20	EFR Dynamic Life Test	48h	0/1887	
		LFR Dynamic Life Test	1000h	0/200	
A00960C A01808A A01914J	AT89C51SND1 AT83C51SND1 VQFP 80	EFR Dynamic Life Test	48h	1/550	Consumption hot spot in DCLK input buffer
		LFR Dynamic Life Test	1000h	0/170	
A01584A	AT89C5131 VQFP64	EFR Dynamic Life Test	48h	0/350	
		LFR Dynamic Life Test	1000h	0/100	

Global		EFR Dynamic Life Test	48h	2/10674	187 ppm
		LFR Dynamic Life Test	-	0/1316	4.4 fit

4.5 AT89C51ED2 Packaging reliability

In this section are presented the packaging qualification measurements carried out in PLCC 44.

Lots	Device Type	Test Description	Step	Result	Comment
A01948K	AT89C51ED2 PLCC 44	Humidity 85/85 post Preconditioning level 1	500h	0/50 0/50	
		Thermal Cycles post Preconditioning L1	500c 1000c	0/50 0/50	
		Autoclave post thermal shocks and Precond. L1	96h	0/50	
A01679C	AT89C51RC2 PLCC44	Preconditioning level 1	SAM Visual Elect.	0/11 0/50 0/50	
		Thermal Cycles post Preconditioning L1	500c 1000c	0/50 0/50	
		Humidity 85/85 post Preconditioning level 1	500h	0/50 0/50	
		Autoclave post thermal shocks and Precond. L1	96h	0/50	
		High Temperature Storage	500h 1000h	0/50 0/50	
		Marking permanency	Visual	0/5	

4.6 AT89C51ED2 Qualification status

Atmel digital 0.35 um wafer process is qualified since 1999, October.

Derived from this technology, AT89C51RD2 / AT89C51ED2 have passed successfully Reliability Testing. Full qualification has been pronounced in June 2003.

All package pass Level 1 of Moisture Sensitivity Ranking as per JESD 20B. Therefore, Dry Packing is not mandatory.

5 Environmental Information

Atmel Nantes Environmental Policy aims are :

- Reducing the use of harmful chemicals in its processes
- Reducing the content of harmful materials in its products
- Using re-usable materials wherever possible
- Reducing the energy content of its products

As part of that plan, Ozone Depleting Chemicals are being replaced either by Atmel Nantes or its sub-contractors.

Atmel Nantes site is ISO14001 certified since May 2000.

6 Other Data

6.1 ISO / TS16949 : 2002 Certificate

CERTIFICAT AFAQ CERTIFICATE

N° TS/2003/20127

N° IATF : 0012697

AFAQ certifie que le système qualité adopté par :
AFAQ certifies that the quality system developed by:

ATMEL NANTES SA

pour les activités suivantes :
for the following activities:

CONCEPTION ET PRODUCTION DE CIRCUITS INTEGRES ET ASICS.

DESIGN AND PRODUCTION OF INTEGRATED CIRCUITS AND ASICS.

exercées sur le(s) site(s) suivant(s) :
carried out in the following location(s):

La Chantrerie BP 70602 F-44306 NANTES CEDEX 3

a été audité selon les "Règles pour les certificateurs tierce partie pour la certification automobile à l'ISO/TS 16949 :2002 - Première édition"
has been assessed in accordance with "the rules for the certification bodies for the automotive certification from ISO/TS 16949 :2002 - First edition"

ISO/TS 16949 : 2002

Chapitre de l'ISO/TS 16949 :2002 éventuellement non applicables 7.3 (l'exclusion de la conception des processus de fabrication n'est pas autorisée) :
The ISO/TS 16949 :2002 chapters which are not applicable 7.3 (permitted exclusions do not include manufacturing process design):

Néant

Le présent certificat, délivré dans les conditions fixées par AFAQ, est valable à dater du :
This certificate, delivered under AFAQ rules, is valid as from:

2003-04-20

(année-mois-jour) *jusqu'au / until :* **2006-04-19** (year-month-day)

LE PRÉSIDENT DU COMITÉ DE CERTIFICATION / THE PRESIDENT OF THE CERTIFICATION COMMITTEE — A. PIGEONNIER

LE DIRECTEUR GÉNÉRAL D'AFAQ / THE MANAGING DIRECTOR OF AFAQ — O. PEYRAT

LE REPRÉSENTANT DE L'ENTREPRISE / ON BEHALF OF THE FIRM — F. FAES

"Sauf suspension notifiée entre temps par AFAQ à l'entreprise désignée ci-dessus, qui s'est engagée à observer les règles définies par AFAQ. Le présent document ne peut se substituer en aucune manière au contrat signé entre l'entreprise et AFAQ, qui seul fait foi.

AFAQ - 116, AVENUE ARISTIDE BRIAND - BP 40 / F-92224 BAGNEUX CEDEX FRANCE

6.2 Data Book Reference

The data sheet is available upon request to sales representative or upon direct access on Atmel web site:

http://www.atmel.com/

Address References
All inquiries relating to this document should be addressed to the following:

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6.3 Revision History

Issue	Modification Notice	Application Date
0	Initial Product Evaluation	2003 July

Remarks: