AT1511

Preliminary product Information

FET BIAS CONTROLLER AND TONE DETECTION

Features

- Provides bias for GaAs and HEMT FETs
- Drives up to three FETs
- Dynamic FET protection
- Drain current set by external resistor
- Regulated negative rail generator requires only 2 external capacitors
- Choice in drain voltage
- Wide supply voltage range
- Polarisation switch for LNBs - supporting zero volt gate switching topology.
- 22kHz tone detection for band switching
- Compliant with ASTRA control specifications
- SSOP surface mount package

Applications

- Satellite receiver LNBs
- Private mobile radio (PMR)
- Cellular telephones

Description

The AT1511 includes bias circuits to drive up to three external FETs. A control input to the device selects either one of two FETs as operational using 0V gate switching methodology, the third FET is permanently active. This feature is particularly used as an LNB polarisation switch. Also specific to LNB applications is the enhanced 22kHz tone detection and logic output feature which is used

to enable high and low band frequency switching. The detector has been specifically designed to reject inerference such as low frequency signals and DiSEqC™ tone bursts - without the use of additional external components.

Drain current setting of the AT1511 is user selectable over the range 0 to 15mA, this is achieved with the addition of a single resistor. The series also offers the choice of FET drain voltage, the AT1511 gives 2 volts.

These devices are unconditionally stable over the full working temperature with the FETs in place, subject to the inclusion of the recommended gate and drain capacitors. These ensure RF stability and minimal injected noise.

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

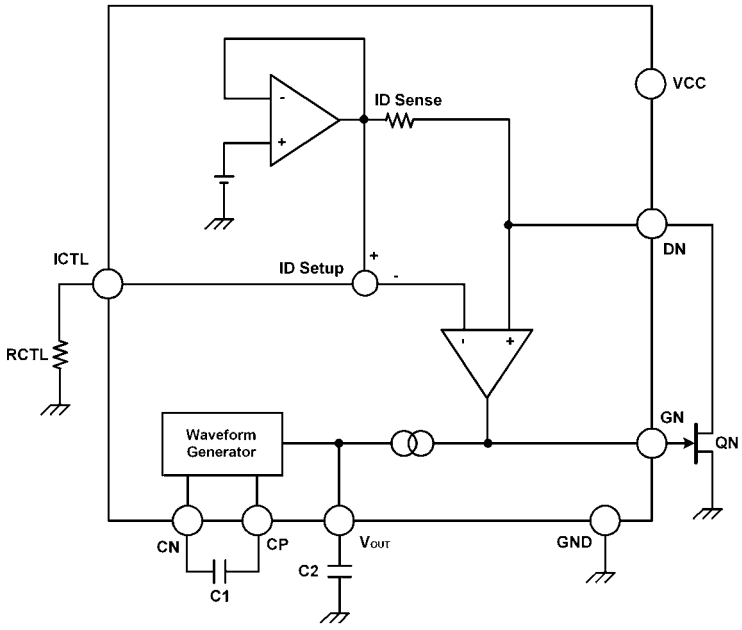
In order to protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed the range -3.5V to 1V. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

The AT1511 are available in SSOP20 for the minimum in device size. Device operating temperature is -40 to 70°C to suit a wide range of environmental conditions.

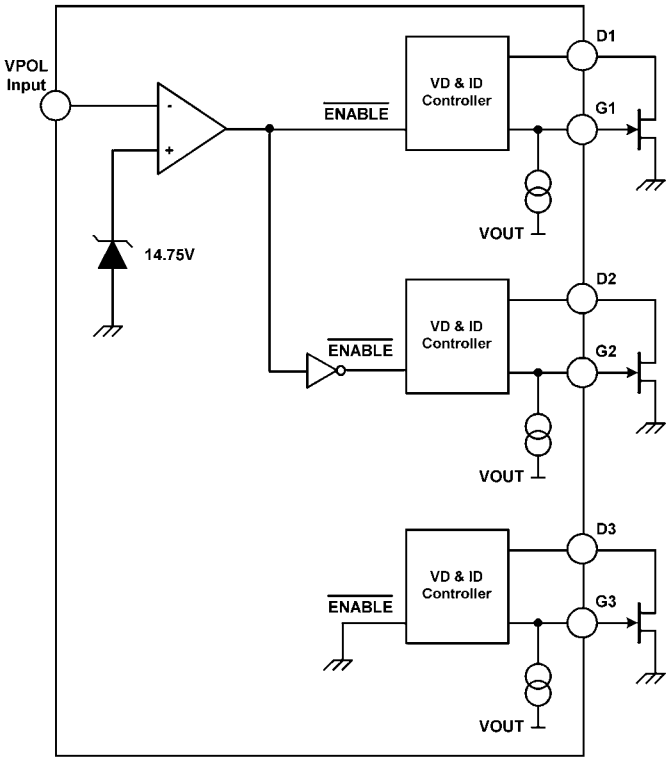
2F, No.10, Prosperity RD. II, Science-Based Industrial Park, Hsinchu 300,Taiwan, R.O.C.
Tel: 886-3-563-0878 http://www.aimtron.com.tw
Fax: 886-3-563-0879 Email: service@aimtron.com.tw

Block Diagram

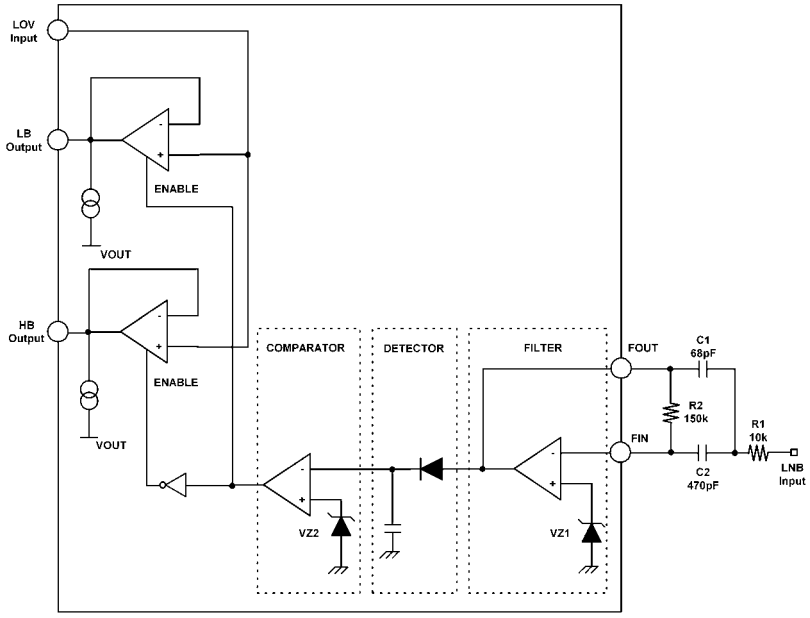
(a) Drain Voltage & Current Controller



(b)Polarisation Switch



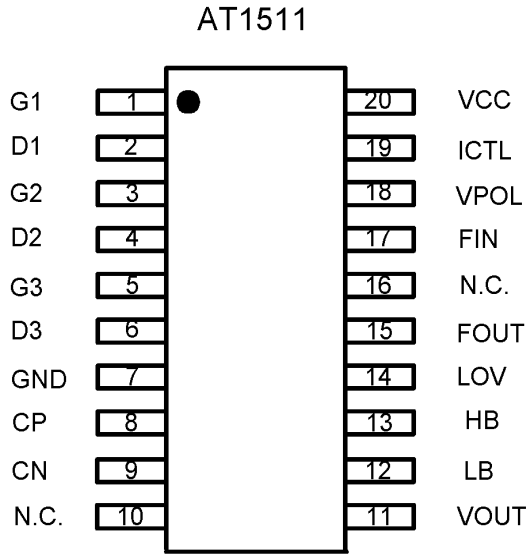
(c)Tone Detection



Pin Descriptions

Pin No.	Pin name	Function
1	G1	1st Gate output voltage Pin
2	D1	1st Drain output voltage Pin
3	G2	2nd Gate output voltage Pin
4	D2	2nd Drain output voltage Pin
5	G3	3rd Gate output voltage Pin
6	D3	3rd Drain output voltage Pin
7	GND	Ground Pin
8	CP	Positive OSC output Pin
9	CN	Negative OSC output Pin
10	N.C.	No connect Pin
11	VOUT	Negative voltage output Pin
12	LB	Error Amplifier output Pin
13	HB	Error Amplifier inverted output Pin
14	LOV	Error Amplifier input Pin
15	FOUT	Filter input Pin
16	N.C.	No connect Pin
17	FIN	Filter output Pin
18	VPOL	Polarisation switch controller Pin
19	ICTL	Drain Current set Resistor connect Pin
20	VCC	Supply voltage Pin

Pin Configuration



Ordering Information

Part number	Package	Marking
AT1511R	**SSOP20**	**AT1511R**
AT1511R_GRE	**SSOP20,Green**	**AT1511R, date code with one bottom line**

Absolute maximum ratings (Ta = 25ºC)

Parameter	Symbol	Limits	unit
Power supply voltage	V_{CC}	-0.6~12	V
Supply Current	I_{CC}	100	mA
Input Voltage	V_{POL}	25	V
Drain Current	V_D	0~15	mA
Operating temperature	T_{opr}	-40~+70	ºC
Storage temperature	T_{stg}	-50~+85	ºC
Power dissipation	P_d	500	mW

Recommended operating conditions (Ta = 25ºC)

Parameter	Symbol	Limits	unit
Power supply voltage	V_{CC}	5~10	V

Electrical characteristics

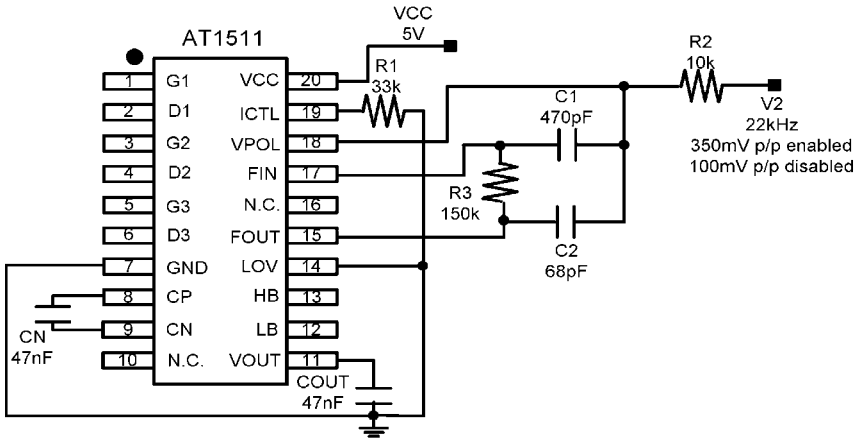
(Unless otherwise stated, Ta=25°C, V_{CC}=5V, I_D=10mA, R_{CTL}=33kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	5	--	10	V	
Supply Current	I_{CC}	--	6	10	mA	I_{D1} to I_{D3}=0
		--	25	35	mA	I_{D1}=0,I_{D2} to I_{D3}=10mA, V_{POL}=14V
		--	25	35	mA	I_{D2}=0,I_{D1} to I_{D3}=10mA, V_{POL}=15.5V
		--	16	25		I_{D1} to I_{D3}=0, I_{LB}=10mA
		--	16	25	mA	I_{D1} to I_{D3}=0, I_{HB}=10mA
Negative Voltage	V_{OUT}	-3.5	-3.0	-2.5	V	I_{OUT}= 0
		--	--	-2.4	V	I_{OUT}= -200μA
Drain Output Noise Voltage	E_{ND}	--	--	0.02	V_{PP}	C_G=4.7nF, C_D=10nF
Gate Output Noise Voltage	E_{NG}	--	--	0.005	V_{PP}	C_G=4.7nF, C_D=10nF
Oscillator Freq.	fo	200	350	800	kHz	
DRAIN						
Drain Current	I_D	8	10	12	mA	
Drain Current Charge with V_{CC}	ΔI_{DV}	--	0.5	--	%/V	V_{CC}=5 to 10V
Drain Current Charge with T_i	ΔI_{DT}	--	0.05	--	%/℃	T_j=-40 to +70°C
Drain Voltage	V_{D1}	1.8	2.0	2.2	V	I_{D1}=10mA, V_{POL}=15.5V
	V_{D2}	1.8	2.0	2.2	V	I_{D2}=10mA, V_{POL}=14V
	V_{D3}	1.8	2.0	2.2	V	I_{D3}=10mA
Drain Voltage Charge with V_{CC}	ΔV_{DV}	--	0.5	--	%/V	V_{CC}=5 to 12V
Drain Voltage Charge with T_i	ΔV_{DT}	--	50	--	ppm	T_j=-40 to +70°C
Leakage Current	I_{L1}	--	--	10	μA	V_{D1}=0.5V, V_{POL}=14V
	I_{L2}	--	--	10	μA	V_{D2}=0.5V, V_{POL}=15.5V
GATE						
Gate Output Current Range	I_{GO}	-30	--	2000	μA	
Gate1 Output Voltage	V_{G10}	-0.05	0	0.05	V	I_{D1}=0, V_{POL}=14V, I_{GO1}=0
	V_{G1L}	-3.5	-2.9	-2.0	V	I_{D1}=12mA, V_{POL}=15.5V, I_{GO1}=-10μA
	V_{G1H}	0.4	0.75	1.0	V	I_{D1}=8mA, V_{POL}=15.5V, I_{GO1}=0
Gate2 Output Voltage	V_{G20}	-0.05	0	0.05	V	I_{D2}=0, V_{POL}=15.5V, I_{GO2}=0
	V_{G2L}	-3.5	-2.9	-2.0	V	I_{D2}=12mA, V_{POL}=14V, I_{GO2}=-10μA
	V_{G2H}	0.4	0.75	1.0	V	I_{D2}=8mA, V_{POL}=14V, I_{GO2}=0
Gate3 Output Voltage	V_{G3L}	-3.5	-2.9	-2.0	V	I_{D3}=12mA, I_{GO3}=-10μA
	V_{G3H}	0.4	0.75	1.0	V	I_{D3}=8mA, I_{GO3}=0
TONE DETECTION						
Input Bias Current	I_B	0.02	0.07	0.25	μA	R_{F1}=150kΩ
Output Voltage	V_{OUT}	1.75	1.95	2.05	V	R_{F1}=150kΩ
Output Current	I_{OUT}	400	520	650	μA	V_{OUT}=1.96V, V_{FIN}=2.1V
Voltage Gain	G_V	--	46	--	dB	f=22kHz,V_{IN}=1mV
Rejection Frequency	f_R	1.0	7.5	--	kHz	$V_{(AC)in}$=1V p/p sq.w
LOV Volt. Range	V_{LOV}	-0.5	--	V_{CC}-1.8	V	I_L=50mA(LB or HB)
LOV Bias Current	I_{LOV}	0.02	0.15	1.0	μA	V_{LOV}=0
LB Output Low	V_{LBL}	-3.5	-2.75	-2.5	V	V_{LOV}=0, I_L=-10μA, Enabled
		-0.01	0	0.01	V	V_{LOV}=3V, I_L=0, Enabled

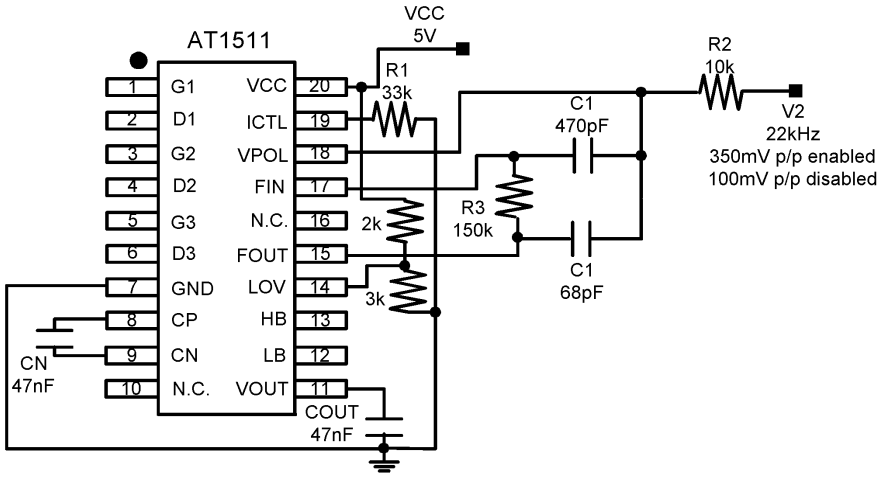
LB Output High	V_{LBH}	-0.025	0	0.025	V	V_{LOV}=0, I_L=10mA, Disabled
		2.9	3.0	3.1	V	V_{LOV}=3V,I_L=50mA,Disabled
HB Output Low	V_{HBL}	-3.5	-2.75	-2.5	V	V_{LOV}=0, I_L=-10μA,Disabled
		-0.01	0	0.01	V	V_{LOV}=3V, I_L=0, Disabled
HB Output High	V_{HBH}	-0.025	0	0.025	V	V_{LOV}=0, I_L=10mA, Enabled
		2.9	3.0	3.1	V	V_{LOV}=3V, I_L=50mA,Enabled
POLARITY SWITCH						
Input Current	I_{POL}	10	20	40	μA	V_{POL}=25V(Applied via R_{POL}=10kΩ)
Threshold Voltage	V_{TPOL}	14	14.75	15.5	V	V_{POL}=25V(Applied via R_{POL}=10kΩ)
Switching Speed	T_{SPOL}	--	--	100	ms	V_{POL}=25V(Applied via R_{POL}=10kΩ)

Test Circuit

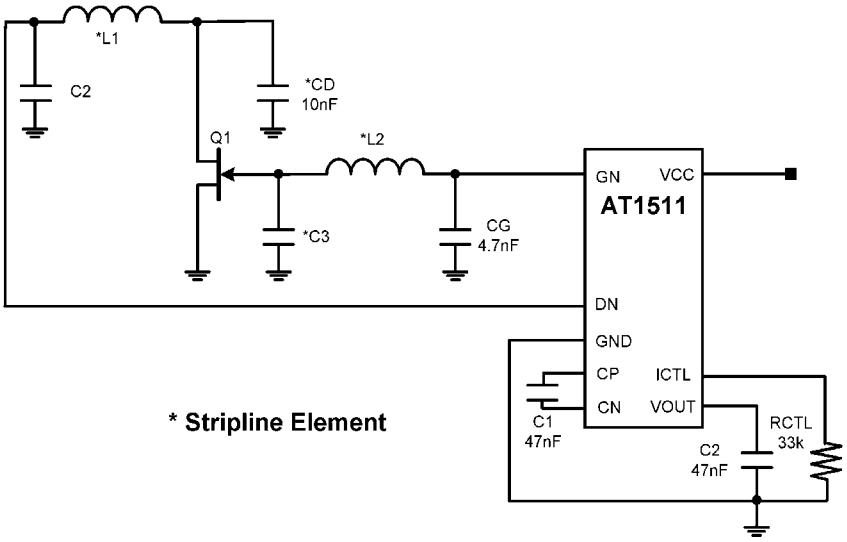
(a) L_{OV} Connected to ground



(b) L_{OV} Connected to V_{OSC}

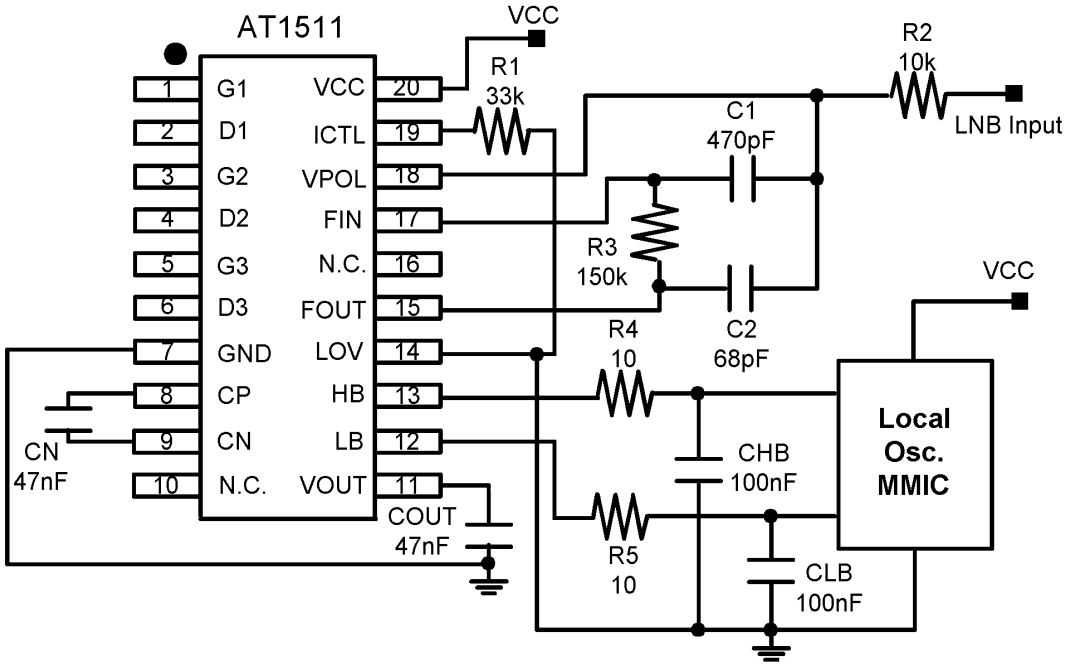


Application Circuit

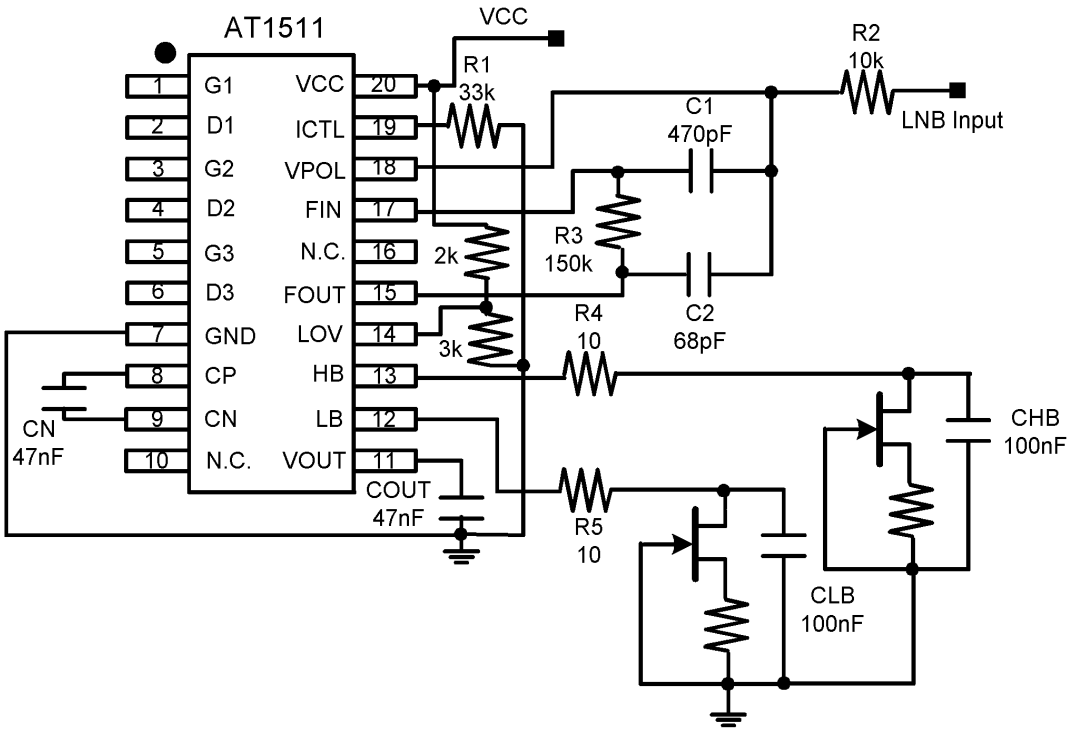


Application Information

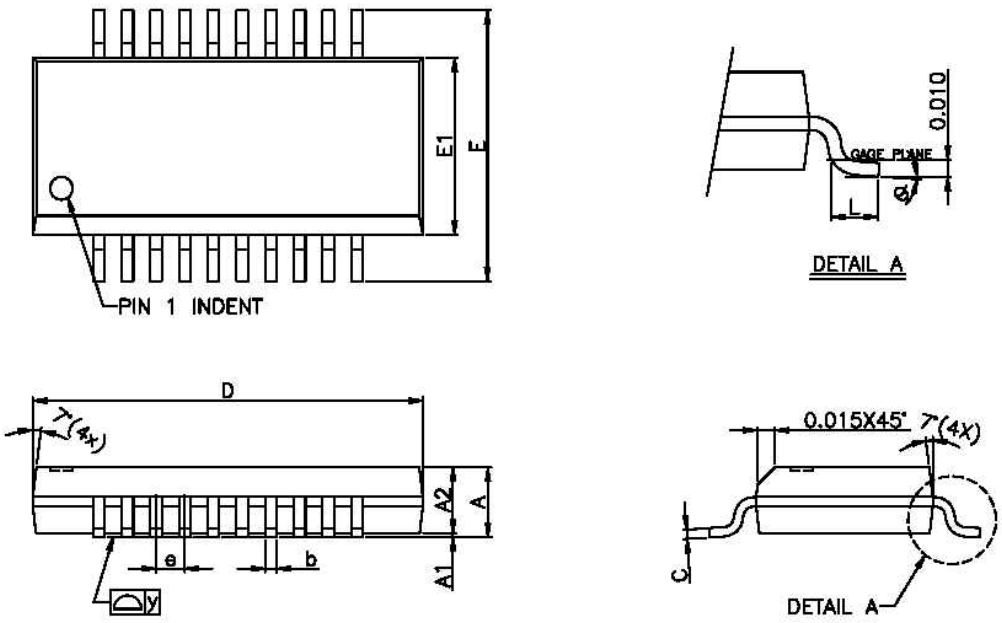
(a) L_{OV} Connected to ground



(b) L_{OV} Connected to V_{OSC}



Package Outlines : 20-pin SSOP



SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	-	0.25	0.004	-	0.010
A2	1.37	1.45	1.52	0.054	0.057	0.060
b	0.23	0.25	0.36	0.009	0.010	0.014
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	8.53	8.64	8.74	0.336	0.340	0.344
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.38	0.71	1.27	0.015	0.028	0.050
e	-	0.64	-	-	0.025	-
y	-	-	0.076	-	-	0.003
θ	0°		8°	0°		8°