DDR 14-Bit Registered Buffer

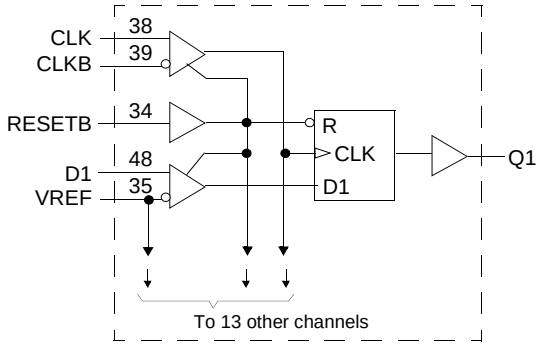
Features

- Differential clock signals
- Meets SSTL_2 class II specifications on outputs
- Supports SSTL_2 Class I and II specifications
- Low voltage operation – V_{DD} = 2.3V to 2.7V
- Available in 48-pin TSSOP and TVSOP package
- Operates at 2.3V to 2.7V for PC1600, PC2100, and PC2700; 2.5V to 2.7V for PC3200
- Pinout and Functionality Compatible with JEDEC Standard SSTV16857

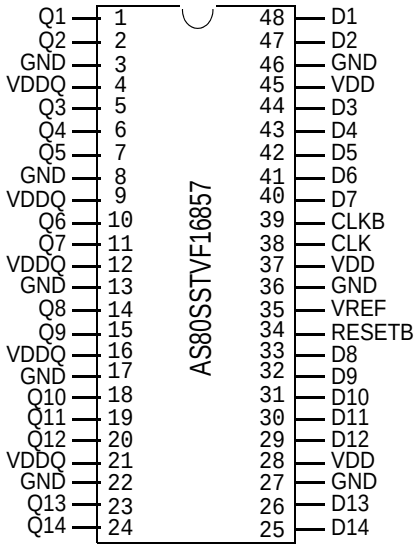
Recommended Applications

- DDR memory modules
- Provides complete DDR DIMM logic solution with PCV857
- SSTL_2-compatible data registers

Block Diagram



Pin Configuration



48-Pin TSSOP & TVSOP
6.10 mm body, 0.50 mm pitch = TSSOP
4.40 mm body, 0.40 mm pitch = TSSOP (TVSOP)

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Truth Table[1]

Inputs				Q outputs
RESETB	CLK	CLKB	D	Q
L	X or floating	X or floating	X or floating	L
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q_0[2]

1 H = high signal level, L = low signal level, ↑ = transition low to high, ↓ = transition high to low, X = don't care.
2 Output level before the indicated steady state input conditions were established.

Description

The 14-bit PC16857 is a universal bus driver designed for 2.3 V to 2.7 V V_{DD} operation and SSTL_2 I/O levels, except for the LVCMOS RESETB input.

Data flow from D to Q is controlled by the differential clock (CLK/CLKB) and a control signal (RESETB). The positive edge of CLK is used to trigger the data flow, and CLKB is used to maintain sufficient noise margins, whereas RESETB, an LVCMOS asynchronous signal, is intended for use only at power-up. PC16857 supports low-power standby operation. A logic level low at RESETB assures that all internal registers and outputs (Q) are reset to the logic low state, and that all input receivers, data (D), and clock (CLK/CLKB) are switched off. Note that RESETB must always be supported with LVCMOS levels at a valid logic state because VREF may not be stable during power-up.

To ensure that outputs are at a defined logic state before a stable clock has been supplied, RESETB must be held at a logic low level during power-up.

In the DDR DIMM application, RESETB is specified to be completely asynchronous with respect to CLK and CLKB, therefore, no timing relationship can be guaranteed between the two signals. When entering a low-power standby state, the register will be cleared and the outputs will be driven to a logic low level quickly relative to the time to disable the differential input receivers. This ensures there are no glitches on the output. When coming out of low power standby state, however, the register will become active quickly relative to the time to enable the differential input receivers. When the data inputs are at a logic level low and the clock is stable during the low-to-high transition of RESETB until the input receivers are fully enabled, the design ensures that the outputs will remain at a logic low level.

Pin Configuration

Pin number	Pin name	Type	Description
1, 2, 5, 6, 7, 10, 11, 14, 15, 18, 19, 20, 23, 24	Q(14:1)	Output	Data output
3, 8, 13, 22, 27, 36, 46	GND	PWR	Ground
4, 9, 12, 16, 21	VDDQ	PWR	Output supply voltage
25, 26, 29, 30, 31, 32, 33, 40, 41, 42, 43, 44, 47,48	D(14:1)	Input	Data input
38	CLK	Input	Positive clock input
39	CLKB	Input	Negative clock input
28, 37, 45	VDD	PWR	Core supply voltage
34	RESETB	Input	Reset (active low)
35	VREF	Input	Input reference voltage

Absolute Maximum Ratings

Storage temperature	- 65° C to +150° C
Supply voltage	-0.5 to 3.6 V
Input voltage[1]	-0.5 to V_{DD} + 0.5
Output voltage[1,2]	-0.5 to V_{DDQ} + 0.5
Input clamp current	± 50 mA
Output clamp current	± 50 mA
Continuous output current	± 50 mA
V_{DD}, V_{DDQ}, or GND current/pin	± 100 mA
Package thermal impedance[3]	55° C/W

1 The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.

2 This current will flow only when the output is in the high state level $V_O > V_{DDQ}$.

3 The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only, and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

Guaranteed by design. Not 100% tested in production.

Parameter	Description		Min	Typ	Max	Units
V_{DD}	Supply voltage		V_{DDQ}		2.7	V
V_{DDQ}	Output supply voltage	PC1600, PC2100, PC2700	2.3		2.7	V
		PC3200	2.5		2.7	V
V_{REF}	Reference voltage (V_{REF}=V_{DDQ}/2)	PC1600, PC2100, PC2700	1.15	1.25	1.35	V
		PC3200	1.25	1.3	1.35	V
V_{TT}	Termination voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	V
V_I	Input voltage		0		V_{DD}	V
$V_{IH(DC)}$	DC input high voltage	Data inputs	V_{REF} + 0.15			V
$V_{IH(AC)}$	AC input high voltage		V_{REF} + 0.31			V
$V_{IL(DC)}$	DC input low voltage				V_{REF} - 0.15	V
$V_{IL(AC)}$	AC input low voltage				V_{REF} - 0.31	V
V_{IH}	Input high voltage level	RESETB	1.7			V
V_{IL}	Input low voltage level				0.7	V
V_{ICR}	Common mode input range	CLK,CLKB	0.97		1.53	V
V_{ID}	Differential input voltage		0.36			V
V_{IX}	Cross-point voltage of differential clock pair		(V_{DDQ}/2) - 0.2		(V_{DDQ}/2) + 0.2	V
I_{OH}	High-level output current				-20	mA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature		0		70	° C

DC Electrical Characteristics for PC1600, PC2100, and PC2700

TA = 0° C to 70° C, V_{DD} = 2.5 ± 0.2 V, and V_{DDQ} = 2.5 ± 0.2 V (unless otherwise stated)

Guaranteed by design. Not 100% tested in production.

Symbol	Parameters	Test conditions		VDD	Min	Typ	Max	Units
V_{IK}		I_I = -18 mA		2.3 V			-1.2	V
V_{OH}		I_{OH} = -100 µA		2.3 V to 2.7 V	V_{DD} - 0.2			V
		I_{OH} = -16 mA		2.3 V	1.95			V
V_{OL}		I_{OL} = 100 µA		2.3 V to 2.7 V			0.2	V
		I_{OL} = 16 mA		2.3 V			0.35	V
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			± 5	µA
I_{DD}	Standby (static)	RESETB = GND	I_O = 0	2.7 V			0.01	µA
	Operating (static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}		2.7 V			25	mA
I_{DDD}	Dynamic operating (clock only)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB = switching 50% duty cycle		2.7 V		28		µA/ clock MHz
	Dynamic operating (per each data input)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB switching 50% duty cycle One data input switching at half clock frequency, 50% duty cycle		2.7 V		15		µA/ clock MHz/ data input
r_{OH}	Output high	I_{OH} = -20 mA		2.3 V to 2.7 V	7	13.5	20	Ω
r_{OL}	Output low	I_{OL} = 20 mA		2.3 V to 2.7 V	7	13	20	Ω
$r_{O(D)}$	$\lvert r_{OH} - r_{OL} \rvert$ each separate bit	I_O = 20 mA, T_A = 25° C		2.5 V			4	Ω
C_I	Data inputs	$V_I = V_{REF}$ ± 310 mV,		2.5 V	2.5		3.5	pF
	CLK and CLKB	V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360 mV		2.5 V	2.5		3.5	pF
	RESETB	$V_I = V_{DD}$ or GND		2.5V	2.5		3.5	pF

DC Electrical Characteristics for PC3200

TA = 0° C to 70° C, V_{DD} = 2.6 ± 0.1 V, and V_{DDQ} = 2.6 ± 0.1 V (unless otherwise stated)

Guaranteed by design. Not 100% tested in production.

Symbol	Parameters	Test conditions		VDD	Min	Typ	Max	Units
V_{IK}		I_I = -18 mA		2.5 V			-1.2	V
V_{OH}		I_{OH} = -100 µA		2.5 V to 2.7 V	V_{DD} - 0.2			V
		I_{OH} = -16 mA		2.5 V	1.95			V
V_{OL}		I_{OL} = 100 µA		2.5 V to 2.7 V			0.2	V
		I_{OL} = 16 mA		2.5 V			0.35	V
I_I	All inputs	$V_I = V_{DD}$ or GND		2.7 V			± 5	µA
I_{DD}	Standby (static)	RESETB = GND	I_O = 0	2.7 V			0.01	µA
	Operating (static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESETB = V_{DD}		2.7 V			25	mA
I_{DDD}	Dynamic operating (clock only)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB = switching 50% duty cycle		2.7 V		28		µA/ clock MHz
	Dynamic operating (per each data input)	RESETB = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLKB switching 50% duty cycle One data input switching at half clock frequency, 50% duty cycle		2.7 V		15		µA/ clock MHz/ data input
r_{OH}	Output high	I_{OH} = -20 mA		2.5 V to 2.7 V	7	13.5	20	Ω
r_{OL}	Output low	I_{OL} = 20 mA		2.5 V to 2.7 V	7	13	20	Ω
$r_{O(D)}$	$\lvert r_{OH} - r_{OL} \rvert$ each separate bit	I_O = 20 mA, T_A = 25° C		2.6 V			4	Ω
C_i	Data inputs	$V_I = V_{REF}$ ± 310 mV,		2.6 V	2.5		3.5	pF
	CLK and CLKB	V_{ICR} = 1.25 V, $V_{I(PP)}$ = 360 mV		2.6 V	2.5		3.5	pF
	RESETB	$V_I = V_{DD}$ or GND		2.6V	2.5		3.5	pF

Timing Requirements

(Over recommended operating free-air temperature range, unless otherwise noted.)

Guaranteed by design. Not 100% tested in production.

Symbol	Parameters		V_{DD} = 2.5 V ± 0.2 V		V_{DD} = 2.6 V ± 0.1 V		Units
			Min	Max	Min	Max	
f_{clock}	Clock frequency			200		280	MHz
t_w	Pulse duration, CLK, CLKB high or low		2.5		2.5		ns
t_{act}	Differential inputs inactive time[1]			22		22	ns
t_{inact}	Differential inputs inactive time[2]			22		22	ns
t_{Su}	Setup time, fast slew rate[3,5]	Data before CLK↑, CLKB↓	0.75		0.4		ns
	Setup time, slow slew rate[4,5]		0.9		0.5		ns
t_h	Hold time, fast slew rate[3,5]	Data after CLK↑, CLKB↓	0.75		0.4		ns
	Hold time, slow slew rate[4,5]		0.9		0.5		ns
t_{SL}	Output slew rate, measurement point at 20% and 80%		1	4	1	4	V/ns

1 Data inputes must be low a minimum time of t_{act} max, after RESETB is taken high.

2 Data and clock inputs must be held at valid levels (not floating) a minimum time of t_{inact} max, after RESETB is taken low.

3 For data signal input slew rate $\geq$ 1V/ns.

4 For data signal input slew rate $\geq$ 0.5 V/ns and < 1 V/ns.

5 CLK, CLKB signals input slew rates are $\geq$ 1 V/ns.

Switching Characteristics for PC1600, PC2100, and PC2700

(Over recommended operating free-air temperature range unless otherwise noted)

(See test circuits and switching waveforms)

Symbol	From (input)	To (output)	VDD = 2.5 V ± 0.2 V			Units
			Min	Typ	Max	
f_{max}			200			MHz
t_{pd}	CLK, CLKB	Q	1.1		2.8	ns
t_{phl}	RESETB	Q			5.0	ns

Switching Characteristics for PC3200

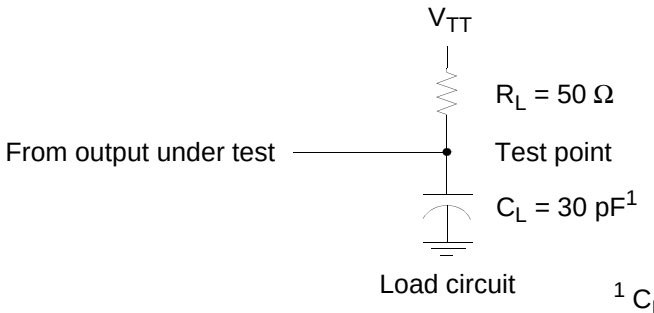
(Over recommended operating free-air temperature range unless otherwise noted)

(See test circuits and switching waveforms)

Symbol	From (input)	To (output)	VDD = 2.6 V ± 0.1 V			Units
			Min	Typ	Max	
f_{max}			280			MHz
t_{pd}	CLK, CLKB	Q	1.1		2.2	ns
t_{phl}	RESETB	Q			5.0	ns

Parameter Measurement Information:

V_{DD} = 2.5 V ± 0.2 V for PC1600, PC2100,& PC2700 and V_{DD}= 2.6 V ± 0.1V for PC3200



[1] C_L includes probe and jig capacitance.

Voltage and Current Waveforms

In the following waveforms, note that all input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, input slew rate = 1 V/ns ± 20% (unless otherwise specified).

The outputs are measured one at a time with one transition per measurement.

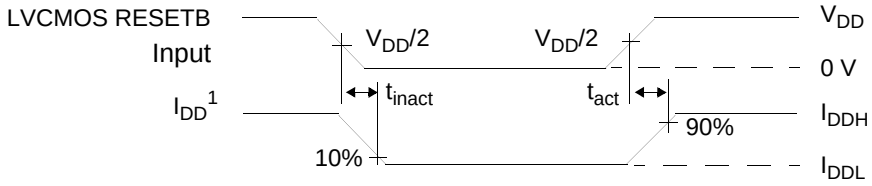
$V_{TT} = V_{REF} = V_{DDQ}/2$.

$V_{IH} = V_{REF}$ + 310 mV (AC voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.

$V_{IL} = V_{REF}$ - 310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.

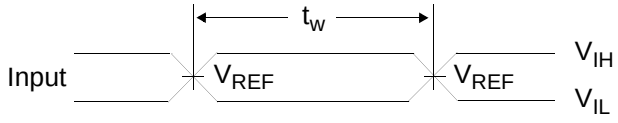
t_{PLH} and t_{PHL} are the same as t_{pd}.

Input active and inactive times

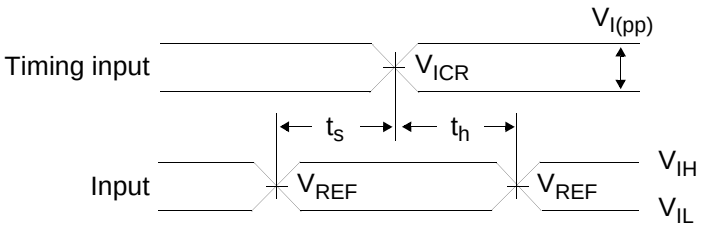


[1] I_{DD} tested with clock and data inputs held at V_{DD} or GND, and I_O = 0 mA.

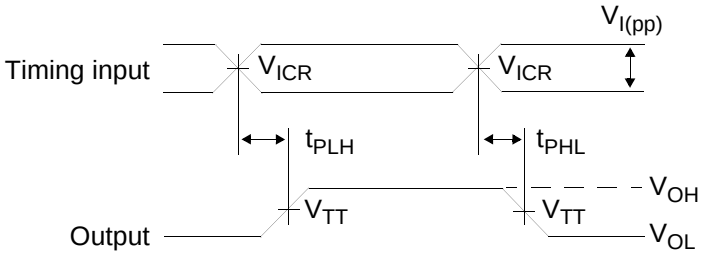
Pulse duration

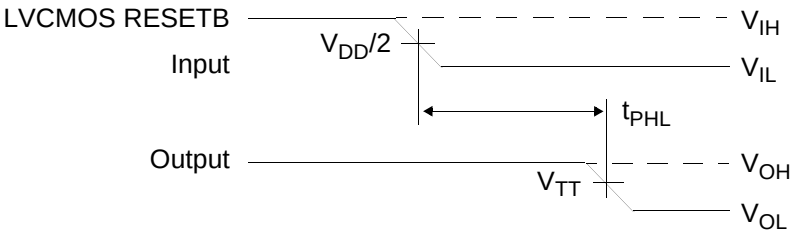


Setup and hold times

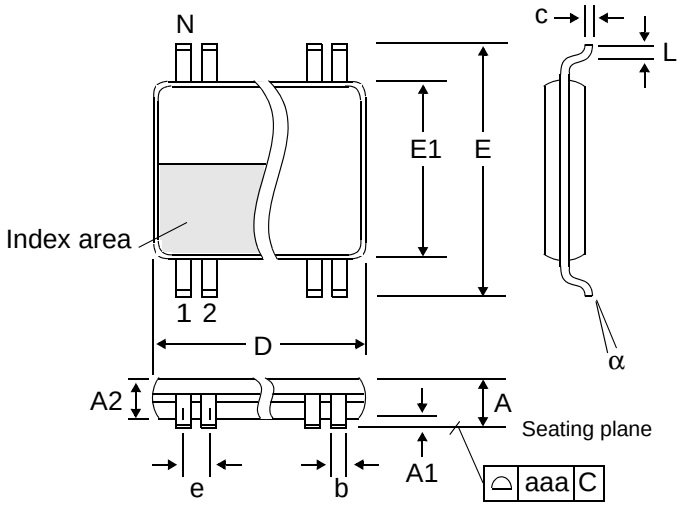


Propagation delay times





Package Dimensions (48- Pin TSSOP)



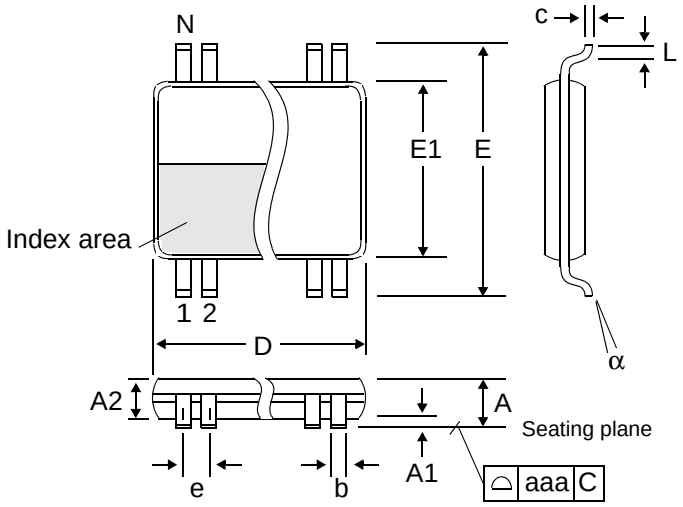
6.10 mm (240 mil) body,
0.50 mm (0.020 mil) pitch TSSOP

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	–	1.20	–	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.32	0.041
b	0.17	0.27	0,007	0.011
c	0.09	0.20	0.0035	0.008
D	See variations below			
E	8.10 basic		0.319 basic	
E1	6.00	6.20	0.236	0.244
e	0.50 basic		0.020 basic	
L	0.45	0.75	0.018	0.030
N	See variations below			
a	0°	8°	0°	8°
aaa	–	0.10	–	0.004

Variations:

N	D (mm)		D (inch)	
	Min	Max	Min	Max
48	12.40	12.60	0.488	0.496

Package Dimensions (Alternate Size)



4.40 mm (173 mil) body,
0.40 mm (16 mil) pitch TVSOP

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	–	1.20	–	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.32	0.041
b	0.13	0.23	0,005	0.009
c	0.09	0.20	0.0035	0.008
D	See variations below			
E	6.40 basic		0.252 basic	
E1	4.30	4.50	0.169	0.177
e	0.40 basic		0.016 basic	
L	0.45	0.75	0.018	0.030
N	See variations below			
a	0°	8°	0°	8°
aaa	–	0.08	–	0.003

Variations:

N	D (mm)		D (inch)	
	Min	Max	Min	Max
48	9.60	9.80	0.378	0.386

Ordering Information

Ordering Number	Marking	Package Type	Quantity per reel	Temperature
AS80SSTVF16857-48TT	AS80SSTVF16857T	48-pin TSSOP, tube		0°C to 70°C
AS80SSTVF16857-48TR	AS80SSTVF16857T	48-pin TSSOP, tape and reel	2500	0°C to 70°C
AS80SSTVF16857-48VT	AS80SSTVF16857V	48-pin TVSOP, tube		0°C to 70°C
AS80SSTVF16857-48VR	AS80SSTVF16857V	48-pin TVSOP, tape and reel	2500	0°C to 70°C